IEEE 802.3dg – Need for a new MII?

Piergiorgio Beruto

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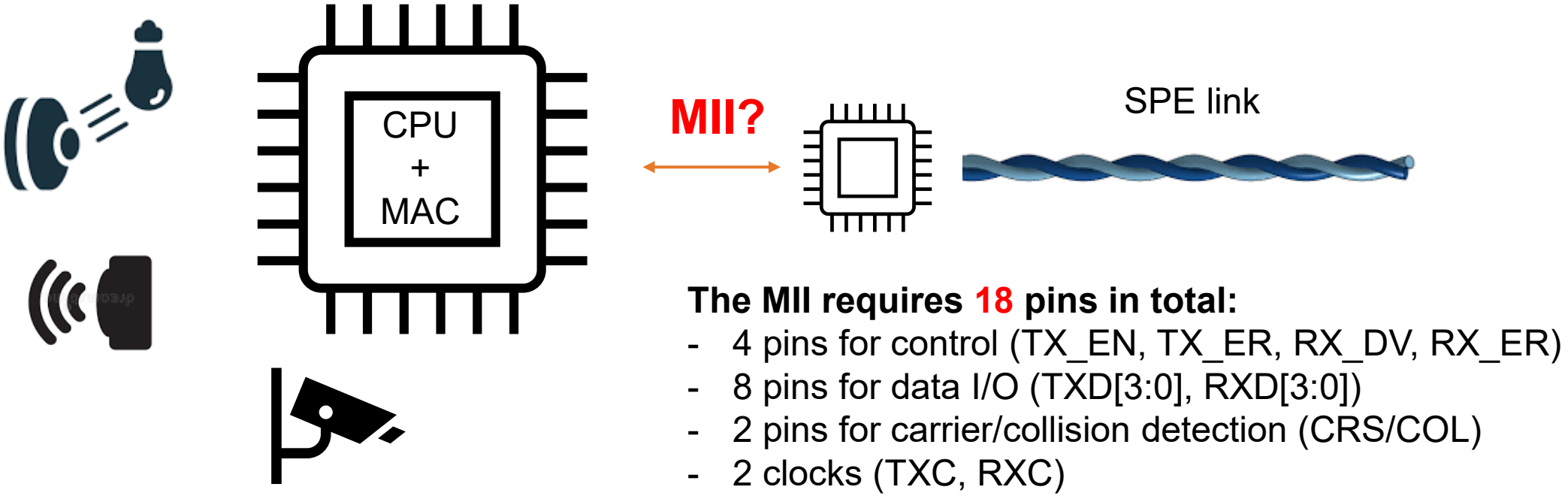
Outline

- In the last decades, Ethernet was pushed to evolve towards higher and higher speeds, leaving 10/100 Mb/s MAC/PHY interfaces to become “legacy”
  - This applies to the MII, which is the only sub-1 Gb/s interface maintained in 802.3
  - But it also applies to industry de-facto standards like RMII
- With the advent of SPE, the need for low-speed interfaces upraised again, although in a very different market and technological scenario
- At the present time, SPE comprises several 10/100 Mb/s PHYs intended to be used in strong embedded systems, especially for industrial and automotive use
  - e.g., 100BASE-T1, 10BASE-T1L, 10BASE-T1S, and ofc the upcoming 10BASE-T1M and *100BASE-T1L.*
- This presentation explores the problems and opportunities in today’s applications for SPE integration and raises the question of whether it is time to define a new MAC/PHY interface

Problem Statement

Overview

- Just a quick look at what the market looks like for low-speed SPE
- SPE applications provide Ethernet connectivity down to the network's edge.
  - e.g., Sensors, actuators, small controller units, etc.
- Typically, such applications require an MCU/CPU with an embedded MAC

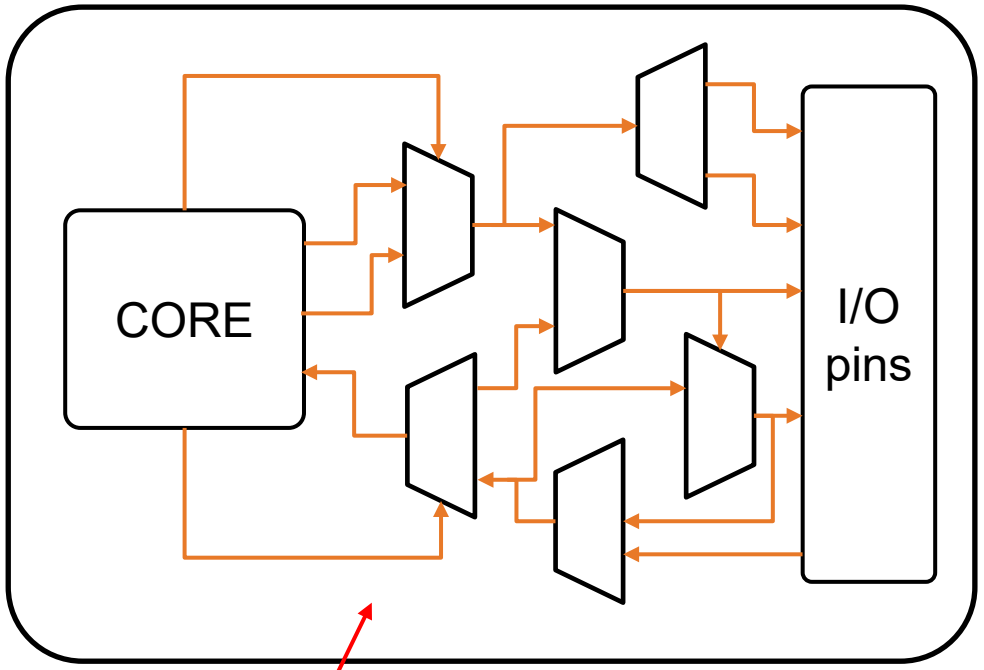


The MII requires 18 pins in total:

- 4 pins for control (TX_EN, TX_ER, RX_DV, RX_ER)
- 8 pins for data I/O (TXD[3:0], RXD[3:0])
- 2 pins for carrier/collision detection (CRS/COL)
- 2 clocks (TXC, RXC)
- 2 pins for management (MDC, MDIO)

The CPU problem

- Modern CPUs and MCUs are configurable for performing a huge number of functions using multiple interfaces



Complex MUX configuration

- The number of functions/interfaces that a CPU can support is strongly limited by the I/O pin multiplexing complexity
  - meeting timings and I/V requirements is difficult
  - SPI, I2C, CAN, USB, Ethernet, …
  - LVCMOS, HSSTL, LVDS, …
- Pins are one valuable resource!!

The PCB problem

- A large number of pins also creates challenges for modern PCB designs
  - The more pins, the more area and/or layers a PCB requires, obviously
    - Most applications are space and cost-constrained (IoT, industrial cabinets, car controls, …)
- Electro-Magnetic Emissions are a big problem, especially because we're dealing with single-ended signals
  - Impedance matching is also a challenge as it typically requires a clean dedicated GND/VCC plane
  - Crosstalk could also be an issue when you have a large amount of pins
- Galvanic isolation is required for many applications
  - Again, the more pins we have, the higher the cost, area, and power
    - ICs for galvanic isolation (e.g., optocouplers) are expensive and consume area and power
- Finally, the package of the PHY ICs itself is a problem. More pins mean higher costs for the PHY as well as for the PCB
  - lower pitches require strict tolerances → more expensive PCB technologies
  - BGAs require a higher number of layers and/or buried (blind) vias

The switch problem

- Switches are facing even more challenges when it comes to SPE
- The two main design “philosophies” are integrated vs. external PHYs
- Integrating the PHYs is a well-known solution that takes away the problem of large pin counts. However, …
  - It takes away a significant amount of flexibility as well. Especially, with the advent of SPE designing multi-purpose PHYs that can do both “normal” Ethernet and SPE is pretty complex and expensive, therefore unlikely to happen.
  - Some PHYs (e.g., 10BASE-T1S/M) shall operate in high-voltage environments, making them unsuitable for integration in low-voltage high-density switch ICs
- On the other hand, external PHYs pose a challenge too
  - Again, the pin count is an obvious bottleneck for increasing the number of ports
  - Having dual/quad/octal PHYs connecting to a single multiplexed high-speed link is also a known solution, but this creates a market issue on one side (low PHY volumes) and a technical challenge on the other (integrating a HIGH number of PHYs in a single package)

More evidence that this is a problem

- The industry is already using non-IEEE MII alternatives, but with drawbacks
  - RMII (reduced MII)
    - uses 10 pins (8 for data/clock/ctrl + 2 for MDC/MDIO) vs 18 of the MII
    - Works at a fixed speed of 50 MHz w/ elastic buffers (potential issue with TSSI)
      - maintaining signal integrity could be a nightmare, especially with long traces
      - timing closure is also a big issue
    - limited support for half-duplex (under-specified)
      - e.g., PLCA does not work (uses RX during TX to generate COL, which violates Clause 4)
    - EME is a problem due to the high-speed shared clock
    - No TX_ER, optional RX_ER → relies on FCS only for frame validation (chance of accepting invalid frames is not less than one time over the age of the universe)
  - OPEN Alliance SPI interface
    - it's a 5-pin MAC client interface, not a MAC/PHY interface
    - works pretty well at 10 Mbps (T1S and T1L), but unlikely to reach 100 Mbps
  - OPEN Alliance PMD interface
    - it's a 3-pin PMA/PMD interface for 10BASE-T1S only

More evidence that this is a problem (2)

- For addressing the switch problem, the industry developed several SERDES-based solutions (e.g., SGMII, QSGMII, USGMII, USXGMI, …)
  - These are proven solutions that are backward compatible with lower speeds
  - See, for example, https://developer.cisco.com/site/usgmii-usxgmii/
- But again, these are non-IEEE solutions

Potential Solutions

Solutions (?)

- I’m not proposing a solution at this time. Rather, I’m raising questions.
  - Is this a good time and place to address this issue?
  - In case, what do we want out of a potential new interface?
- If yes, an initial wish list could be:
  - Address the need for significantly lowering the pin count
  - Ensure all the “new” IEEE features are covered (EEE, PLCA, TSSI, Preemption, …)
    - don’t let the industry create alternate (potentially incomplete) standards!
  - Address PCB challenges (e.g., allow differential signaling vs single-ended)
  - Address the need for integration into high-speed Ethernet switches
  - More? (Open discussion…)

Conclusions

Conclusions

- SPE is bringing back 10/100 Mb/s PHYs
- Currently, the only sub-1Gb/s MAC / PHY interface defined in IEEE is the MII
  - MII uses 18 pins in total
- In today's embedded systems, pins are a very valuable resource
- PHYs with a high pin count create economic and technical challenges
- Ethernet switches using external PHYs also have problems with MII
  - pin count
  - limited, non-standard aggregation capabilities
- Is this the time to define a new interface leveraging modern Si technologies?
  - If yes, is it appropriate to address this topic in 802.3dg?
- There is a growing need for an efficient interface both in the area of integration with high-speed switches and for the end nodes, which are typically strong-embedded systems
- The IEEE has neglected these market needs so far, and the solutions have been developed outside of IEEE

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