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100BASE-T1L PCS and PMA Clause 45 Registers

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Introduction

- This presentation discusses the new PCS and PMA clause 45 registers required for 100BASE-T1L

New 100BASE-T1L Registers

- New 100BASE-T1L control and status registers
  - It may make sense and may be possible to share some of these registers with 10BASE-T1L
  - Especially for register bits that are copies of existing common PMA/PCS control registers
  - However, that might complicate the S/W interface and may go against normal practice
- Some existing common PMA / PCS registers
  - BASE-T1 PMA/PMD Extended Ability Register
  - BASE-T1 PMA/PMD Control Register
  - PMA/PMD Control 1 register and PMA/PMD Status 1 register
  - PCS Control 1 register and PCS Status 1 register
- New 100BASE-T1L PMA / PCS control and status registers required for 100BASE-T1L
  - 100BASE-T1L PMA control register
  - 100BASE-T1L PMA status register
  - 100BASE-T1L test mode control register
  - 100BASE-T1L PCS control register
  - 100BASE-T1L PCS status register

BASE-T1 PMA/PMD Extended Ability Register

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

The assignment of bits in the BASE-T1 PMA/PMD extended ability register is shown in Table 45–19. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:7	Reserved	Value always 0	RO
1.18.6	10GBASE-T1 ability	1 = PMA/PMD is able to perform 10GBASE-T1 0 = PMA/PMD is not able to perform 10GBASE-T1	RO
1.18.5	5GBASE-T1 ability	1 = PMA/PMD is able to perform 5GBASE-T1 0 = PMA/PMD is not able to perform 5GBASE-T1	RO
1.18.4	2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 2.5GBASE-T1 0 = PMA/PMD is not able to perform 2.5GBASE-T1	RO
1.18.3	10BASE-T1S ability	1 = PMA/PMD is able to perform 10BASE-T1S 0 = PMA/PMD is not able to perform 10BASE-T1S	RO
1.18.2	10BASE-T1L ability	1 = PMA/PMD is able to perform 10BASE-T1L 0 = PMA/PMD is not able to perform 10BASE-T1L	RO
1.18.1	1000BASE-T1 ability	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1	RO
1.18.0	100BASE-T1 ability	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1	RO

[a]RO = Read only

45.2.1.16.5 10BASE-T1L ability (1.18.2)

When read as a one, bit 1.18.2 indicates that the PMA/PMD is able to operate as a 10BASE-T1L PMA type. When read as a zero, bit 1.18.2 indicates that the PMA/PMD is not able to operate as a 10BASE-T1L PMA type.

- **Add 100BASE-T1L ability register (1.18.7)**
  - When read as a one, bit 1.18.7 indicates that the PMA/PMD is able to operate as a 100BASE-T1L PMA type. When read as a zero, bit 1.18.7 indicates that the PMA/PMD is not able to operate as a 100BASE-T1L PMA type.

BASE-T1 PMA/PMD Control Register

45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

The assignment of bits in the BASE-T1 PMA/PMD control register is shown in Table 45–178.

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2100.15	Reserved	Value always 1	RO
1.2100.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.2100.13:4	Reserved	Value always 0	RO
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved 0 1 1 1 = Reserved 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.214.2 Type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are set to 0010, the mode of operation is 10BASE-T1L. When these bits are set to 0011, the mode of operation is 10BASE-T1S. When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are. set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

- **Add 100BASE-T1L Type selection (1.18.7)**
  - Add new sentence between 1000BASE-T1 and 10BASE-T1L
  - When these bits are set to 0111, the mode of operation is 100BASE-T1L.

PMA/PMD Control 1 Register

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–4. The default value each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device u power up or completion of reset is a normal operational state without management intervention.

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0	RO
1.0.13	Speed selection (LSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
1.0.12	Reserved	Value always 0	RO
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0	RO
1.0.6	Speed selection (MSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 0 0 0 0 = 10 Gb/s	R/W
1.0.1	PMA remote loopback	1 = Enable PMA remote loopback mode 0 = Disable PMA remote loopback mode	R/W
1.0.0	PMA local loopback	1 = Enable PMA local loopback mode 0 = Disable PMA local loopback mode	R/W

- Existing common PMA/PMD control register
- Registers for common functions like software reset, software power-down, and loopback are implemented in multiple clauses
  - 1.2294 is the 10BASE-T1L PMA Control register
    - 1.2294.15 PMA reset is a copy of 1.0.15 Reset
    - 1.2294.14 Transmit disable is a copy of 1.9.0 Global PMD transmit disable
    - 1.2294.11 Low-power is a copy of 1.0.11 Low Power
    - 1.2294.0 Loopback is a copy of 1.0.0 PMA local loopback
- The speed selection bits are not used for 100BASE-T1L as Auto-Negotiation is mandatory

100BASE-T1L PMA Control Register – **New Register**

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45.2.1.231 10BASE-T1L PMA control register (Register 1.2294)

The assignment of bits in the 10BASE-T1L PMA control register is shown in Table 45–193.

Table 45–193—10BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2294.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2294.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2294.13	Reserved	Value always zero	RO
1.2294.12	Transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2294.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2294.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2294.9:1	Reserved	Value always 0	RO
1.2294.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

- Auto-negotiation is mandatory in 100BASE-T1L and transmit level can only be negotiated
  - However, we do need a bit to control the transmit amplitude for test modes
  - The 'Transmit voltage amplitude control' bit should change to 'Test mode transmit voltage amplitude control'
- The following register will be different between 10 and 100 so should have an independent 100BASE-T1L register:
  - EEE enable
- The following registers are used the same way for 10 and 100 so we could consider sharing with 1.2294 or mark as Reserved for 100BASE-T1L
  - PMA reset – copy of 1.0.15 Reset
  - Transmit disable - copy of 1.9.0 Global PMD transmit disable
  - Low-power ability - a copy of 1.0.11 Low Power
  - Loopback – copy of 1.0.0 PMA local loopback

PMA/PMD Status 1 Register

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

The assignment of bits in the PMA/PMD status 1 register is shown in Table 45–5. All the bits in the PMA/PMD status 1 register are read only; therefore, a write to the PMA/PMD status 1 register shall have no effect.

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:10	Reserved	Value always 0	RO
1.1.9	PIASA	PMA ingress AUI stop ability	RO
1.1.8	PEASA	PMA egress AUI stop ability	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Value always 0	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low

- Existing common PMA/PMD status register

45.2.1.2.4 Receive link status (1.1.2)

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

100BASE-T1L PMA Status Register – **New Register**

45.2.1.232 10BASE-T1L PMA status register (Register 1.2295)

The assignment of bits in the 10BASE-T1L PMA status register is shown in Table 45–194.

Table 45–194—10BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2295.15:14	Reserved	Value always 0	RO
1.2295.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2295.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2295.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2295.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2295.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2295.8:3	Reserved	Value always 0	RO
1.2295.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2295.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2295.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL

[a]RO = Read only, LL = Latching low, LH = Latching high

- The following registers may be different between 10 and 100 so should have independent 100BASE-T1L registers for:
  - 2.4 Vpp operating mode ability
  - EEE ability
  - Receive fault ability
- We could share the following registers with 1.2295, but S/W may be simpler with separate registers
  - Receive polarity
  - Receive fault
  - Receive link status
    - Note this is a latch low register, so reading this would also clear the latching condition for register 1.1.2

100BASE-T1L Test Mode Control Register – **New Register**

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45.2.1.233 10BASE-T1L test mode control register (Register 1.2296)

The assignment of bits in the 10BASE-T1L test mode control register is shown in Table 45–195. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–195—10BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2296.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2296.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

- The following registers are likely used the same way between 10 and 100 so could consider sharing with 1.2296
  - Test mode control
- There likely will be additional test modes for 100BASE-T1L
  - For example, for low latency and FEC modes
  - Is there any confusion if the test modes are different between 10 and 100?

45.2.1.233.1 Test mode control (1.2296.15:13)

Transmitter test mode operations defined by bits 1.2296.15:13 are described in 146.5.2. The default value for bits 1.2296.15:13 is zero.

PCS Control 1 Register

45.2.3.1 PCS control 1 register (Register 3.0)

The assignment of bits in the PCS control 1 register is shown in Table 45–234. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–234—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.12	Reserved	Value always 0	RO
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10	Clock stop enable	1 = The PHY may stop the clock during LPI 0 = Clock not stoppable	R/W
3.0.9:7	Reserved	Value always 0	RO
3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = 25/10 Gb/s 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

- Existing common PCS control register
- Registers for common functions like software reset, software power-down, and loopback are implemented in multiple clauses
  - 3.2278 is the 10BASE-T1L PCS Control 1 register
    - 3.2278.15 PCS reset is a copy of 3.0.15 Reset
    - 3.2278.14 Loopback is a copy of 3.0.14 Loopback
- Low Power appears to be different for PCS
  - No copy of 3.0.11 Low Power
- The speed selection bits are not used for 100BASE-T1L as Auto-Negotiation is mandatory

100BASE-T1L PCS Control Register – **New Register**

45.2.3.70 10BASE-T1L PCS control register (Register 3.2278)

The assignment of bits in the 10BASE-T1L PCS control register is shown in Table 45–296. The default value for each bit of the 10BASE-T1L PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–296—10BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2278.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2278.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2278.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.70.1 PCS reset (3.2278.15)

Bit 3.2278.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.70.2 Loopback (3.2278.14)

The 10BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2278.14 is set to one. When in loopback mode, the 10BASE-T1L PCS shall accept data on the transmit path and return it on the receive path. The default value of bit 3.2278.14 is zero.

Bit 3.2278.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

- The following registers are copies of PCS control 1 register and likely used the same way between 10 and 100 so could consider sharing with 3.2278 or mark as Reserved for 100BASE-T1L
  - PCS Reset – copy of 3.0.15 Reset
  - Loopback – copy of 3.0.14 Loopback

PCS Status 1 Register

45.2.3.2 PCS status 1 register (Register 3.1)

The assignment of bits in the PCS status 1 register is shown in Table 45–235. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

Table 45–235—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:12	Reserved	Value always 0	RO
3.1.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.1.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.1.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6	Clock stop capable	1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO
3.1.5:3	Reserved	Value always 0	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

- Existing common PCS status register

45.2.3.2.7 PCS receive link status (3.1.2)

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10/25/40/50/100/200/400GBASE-R, 10GBASE-W, or any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

100BASE-T1L PCS Status Register – **New Register**

45.2.3.71 10BASE-T1L PCS status register (Register 3.2279)

The assignment of bits in the 10BASE-T1L PCS status register is shown in Table 45–297. All the bits in the 10BASE-T1L PCS status register are read only; a write to the 10BASE-T1L PCS status register shall have no effect.

Table 45–297—10BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2279.15:12	Reserved	Value always 0	RO
3.2279.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2279.6:3	Reserved	Value always 0	RO
3.2279.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2279.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

- We could share the following register with 3.2279, but S/W may be simpler with a separate register
  - PCS receive link status
    - Note this is a latch low register, so reading this would also clear the latching condition for register 3.1.2

45.2.3.71.6 PCS receive link status (3.2279.2)

When read as a one, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this bit. This bit shall be implemented with latching low behavior and is a **reflection of the variable scr_status**. If the bit is read while scr_status = OK, then this bit is set. If scr_status = NOT_OK, then this bit is reset.

100BASE-T1L Transmit Fault Description

45.2.1.7.4 Transmit fault (1.8.11)

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for the various PMA/PMDs is given in Table 45–9.

The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

Table 45–9—Transmit fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.2
100BASE-T1	96.4.2

- **Add 100BASE-T1L row to Table 45-9**
  - 100BASE-T1L : 199.4.2

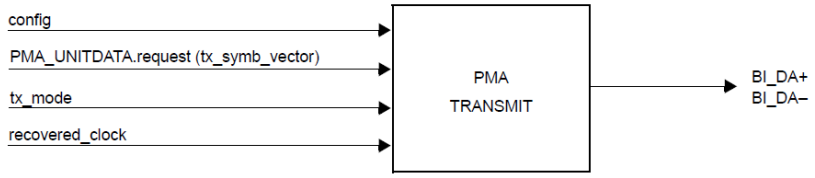


Figure 146–13—PMA Transmit

A single transmitter is used to generate the PAM3 signal BI_DA on the wire using the transmit clock, TX_TCLK (see 146.5.4.5). When the config parameter is set to MASTER, the PMA Transmit function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

199.4.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a three-level modulated signal on the single balanced pair of conductors. When the PHY Control state diagram (Figure 199–13) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. The signals generated by PMA Transmit shall comply with the electrical specifications given in 199.5.3.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 199.5.3.3. The LEADER-FOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 199.4.7 while meeting the jitter requirements of 199.5.3.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

100BASE-T1L Receive Fault Description

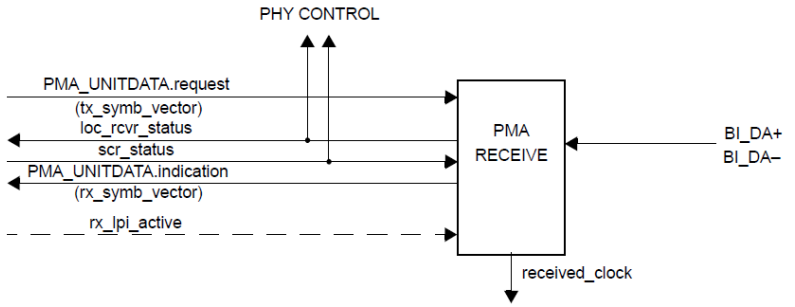
45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for the various PMA/PMDs is given in Table 45–10.

Table 45–10—Receive fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.3
100BASE-T1	96.4.3

- **Add 100BASE-T1L row to Table 45-10**
  - 100BASE-T1L : 199.4.3



NOTE—Signals shown with dashed lines are required only for EEE functionality.

Figure 146–14—PMA Receive

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.232.7.

199.4.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM3 signals on the balanced pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over the receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the pair into the PMA_UNITDATA.indication parameter rx_symb with a symbol error

. . .

The receiver uses knowledge of the sequence of symbols transmitted by the link partner during training to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the condition link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.XXXX.7.

New 100BASE-T1L PCS/PMA Clause 45 Registers

- New registers
  - Add 100BASE-T1L ability register bit (1.18.7) – see slide 4
  - Add 100BASE-T1L Type selection bit (1.18.7) – see slide 5
  - New 100BASE-T1L PMA control register – see slide 7
  - New 100BASE-T1L PMA status register – see slide 9
  - New 100BASE-T1L test mode control register – see slide 10
  - New 100BASE-T1L PCS control register – see slide 12
  - New 100BASE-T1L PCS status register – see slide 14
- Additional rows in tables
  - Add 100BASE-T1L row to Table 45-9 – see slide 15
  - Add 100BASE-T1L row to Table 45-10 – see slide 16

Conclusions

- A summary of the 100BASE-T1L PCS and PMA Clause 45 registers required for 100BASE-T1L has been presented
  - Simplest path is to continue normal practice and have a complete set of register bits for the 100BASE-T1L technology
  - Task Force could decide to mark registers bits that are duplicated in the existing common PMA/PMD and PCS Control registers as Reserved

Questions ?