

## **100BASE-T1L PCS Receive Function**

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## Introduction



- This presentation presents an update to the text for PCS Receive required for the draft
  - The text in section 190.3.4 PCS Receive function of draft 1.0 is really just a placeholder to provide some context for the PCS transmit and PMA training sections which are pretty complete
  - The details, tables and state diagrams for PCS Receive are missing, see the editor's note on page 73

190.3.4 PCS Receive function	34
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Editor's Note (to be removed prior to Working Group Ballot):	36
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The text below is part of the description of the PCS Receive, but lacks the requirements and description	38
of the PCS Receive state diagram operation which needs to be decided before that text can be written. Contributions are requested to fill out PCS Receive requirements before text is filled out here.	39
contributions are requested to fin out ress receive requirements before text is fined out here.	40

- This presentation describes the operation of PCS Receive function including the tables and state diagram
- This presentation also provides the text for the draft, showing the changes required



- The PCS Receive function shall conform to the PCS Receive state diagram in Figure 190–13B
  - When RS-FEC is enabled for the link, the PHY Receive function shall implement the RFER monitor state diagram of Figure 190–13C
- ► PCS Receive operation TRAIN
  - When pcs\_rx\_mode is TRAIN, the PCS Receive function checks the received PAM2 symbols and signals the reliable acquisition of the descrambler by setting scr\_status to OK
    - When config is LEADER, and loc\_rcvr\_status is OK, the PCS Receive function monitors the received PAM2 symbols to determine whether the link partner is signaling reliable operation of its receive link
    - Once reliable operation of the receive link for the remote FOLLOWER is detected, this is communicated to the PHY Control function by setting rem\_flr\_rcvr\_status to OK
    - When the remote PHY is sending formatted training frames the PCS Receive function attains frame and block synchronization based on the formatted training frame
      - The formatted training frame includes an alignment bit every 192 PAM2 16 symbols, which is aligned with the PCS
        partial frame boundary, as well as an InfoField, which is inserted into every 16th PCS partial frame
      - The PCS Receive function signals the detection of a valid InfoField to the PHY Control function by setting rx\_info\_frame to TRUE



### ▶ PCS Receive operation – NORMAL

- When pcs\_rx\_mode is NORMAL, the PCS Receive function applies the inverse of the encoding processes described in 190.3.3 PCS Transmit function
- Every 2N RX\_CLK cycles an (8N+1)B block is received and is decoded to generate a list of N characters each of which represents either a data octet or a control symbol
- These characters are mapped one at a time into rx\_char which is processed in accordance with Figure 190–13B to generate signals at the MII

### ► PCS Receive operation – error conditions

- The PCS Receive function incorporates several means to detect error conditions
  - The PCS Receive state diagram detects packets that are not preceded by start-of-packet control symbols or are not followed by end-of-packet control symbols
  - When RS-FEC is enabled for the link, the RS-FEC frame error ratio (RFER) monitor process, monitors the reliability of the RS decoder and asserts hi\_rfer to indicate an excessive RS- FEC frame error ratio
    - The PCS Receive function may use these detected error conditions to determine whether it is operating reliably and generates pcs\_status accordingly



### ► PCS Receive operation - invalid characters

- Errors during transmission can cause invalid characters to be received that could not have been transmitted
- Received characters shall be identified as invalid characters in the following cases:
  - The received character represents a control symbol with the numerical value 0x00
  - The received character represents the control symbol /Ll/ when EEE is not enabled for the link
  - The received character is declared to be invalid due to a block error
  - Invalid received characters are replaced with characters representing /E/ before the processing shown in Figure 190–13B PCS Receive state diagram is performed

### ▶ PCS Receive operation - block errors

- Errors during transmission can cause block errors during decoding
  - While an (8N + 1)B block is being decoded an invalid pointer can be encountered
    - In this case all received characters from the corresponding octet position to the end of the block are replaced with characters representing /E/
  - If an (8N + 1)B block contains information from the payload of an RS-FEC codeword that cannot be decoded due to uncorrectable errors all characters are replaced with characters representing /E/



### PCS Receive operation – character decoding

- The PCS Receive function decodes each received character into two MII transfers and following Table 190–5p5
- For example /Tu2/ corresponds to an end of frame occurring on a non byte aligned boundary, where the last data nibble is 0x2
  - This is replaced by a normal MII nibble transfer encoding the data value 0x2
  - Followed by normal inter-frame signaling
    - RX\_DV = 0 and RX\_ER = 0

#### Table 190–5p5— Character decoding

Received	Even Transfer			Odd Transfer		
Character	RX_DV	RX_ER	RXD<3:0>	RX_DV	RX_ER	RXD<3:0>
/E/	1	1	0000	1	1	0000
/I/	0	0	0000	0	0	0000
/Su/	0	0	0000	1	0	0101
/Tp/	0	0	0000	0	0	0000
/LI/	0	1	0001	0	1	0001
/R/	0	1	0100	0	1	0100
/Sp/	1	0	0101	1	0	0101
/Tu0/	1	0	0000	0	0	0000
/Tu1/	1	0	0001	0	0	0000
/Tu2/	1	0	0010	0	0	0000
/Tu3/	1	0	0011	0	0	0000
/Tu4/	1	0	0100	0	0	0000
/Tu5/	1	0	0101	0	0	0000
/Tu6/	1	0	0110	0	0	0000
/Tu7/	1	0	0111	0	0	0000
/Tu8/	1	0	1000	0	0	0000
/Tu9/	1	0	1001	0	0	0000
/TuA/	1	0	1010	0	0	0000
/TuB/	1	0	1011	0	0	0000
/TuC/	1	0	1100	0	0	0000
/TuD/	1	0	1101	0	0	0000
/TuE/	1	0	1110	0	0	0000
/TuF/	1	0	1111	0	0	0000
Data Value ROCT<7:0>	1	0	ROCT<3:0>	1	0	ROCT<7:4>



### ▶ PCS Receive operation – block lock

Clauses 149 / 165 have a block\_lock variable defined as follows

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi\_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block\_lock flag is de-asserted. The block\_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block\_lock is asserted and hi\_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the 25GMI.

- Hence, in the case of high RFER block\_lock is set FALSE but may subsequently become TRUE again
- ▶ In this clause we are proposing a different approach
  - This is partially motivated by the desire to have a common approach with or without RS-FEC
  - When RS-FEC is enabled, the link will not come up unless the RS-FEC is operating correctly
  - Once the link comes up, if there is high RFER the PCS is expected to set pcs\_status to NOT\_OK, which is expected to cause loc\_rcvr\_status to become NOT\_OK and thus cause the link to drop
  - We do not try to recover from a situation where the RS-FEC is operating unreliably
  - The fastest and most robust recovery is to drop the link and restart Auto-Negotiation



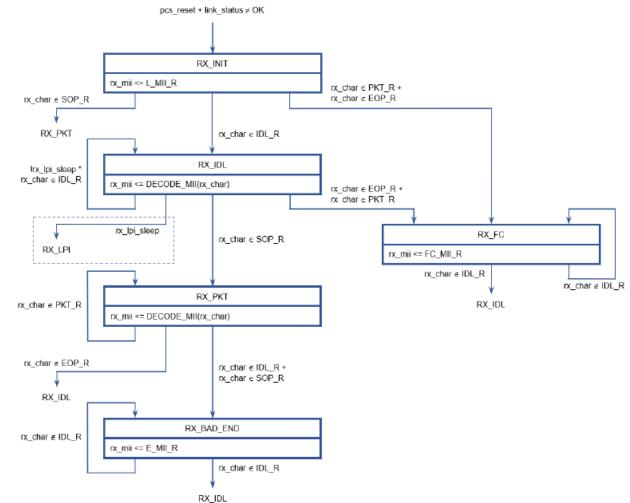
#### PCS Receive function

This state diagram determines rx\_mii

#### rx\_mii<0:1><0:5>

Array containing 2 6-bit elements representing MII transfers. Each element includes the values of RX\_DV, RX\_ER and RXD<3:0> for the corresponding MII transfer.

- The (8N)B/(8N+1)B decoding generates 8N characters
- The PCS receive state diagram operates character by character
- Characters are classified according to the set they belong to
- For example, the set SOP\_R includes all the characters that represent start-of-packet SOP\_R = {/Sp/, /Su/}
- The state diagram, recognizes unexpected sequences of characters and uses them to flag false carrier and bad frame end events
  - These are signaled across the MII
- When EEE is enabled and when 32 consecutive /Ll/ control symbols are detected, the state diagram moves to the RX\_LPI state



NOTE-Signals and functions shown with dashed lines are only required when EEE is enabled for the link.

Figure 190–13B—PCS Receive state diagram, part a



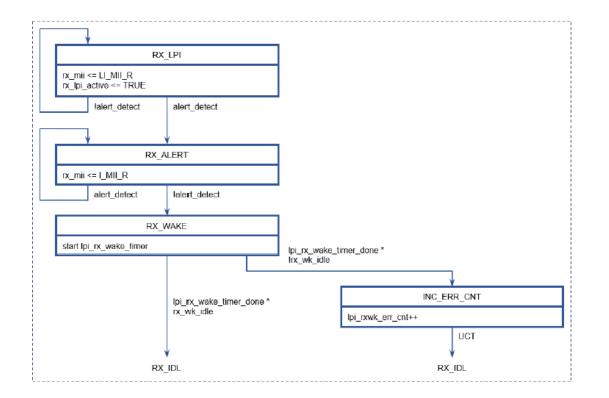
### ▶ PCS Receive function – LPI

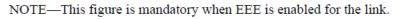
- In the RX\_LPI state the PHY continuously signals Assert LPI at the MII receive pins
- When alert\_detect become TRUE the state diagram transitions to RX\_ALERT and Normal inter-frame is signaled at the MII

#### alert\_detect

Boolean variable that is set TRUE when the PCS Receive state diagram of Figure 190–13B is in the RX\_LPI state or the RX\_ALERT state and a sequence of symbols is received from the PMA via the rx\_symb parameter that is consistent with alert signaling, as specified in 190.3.7.4. It is set FALSE otherwise.

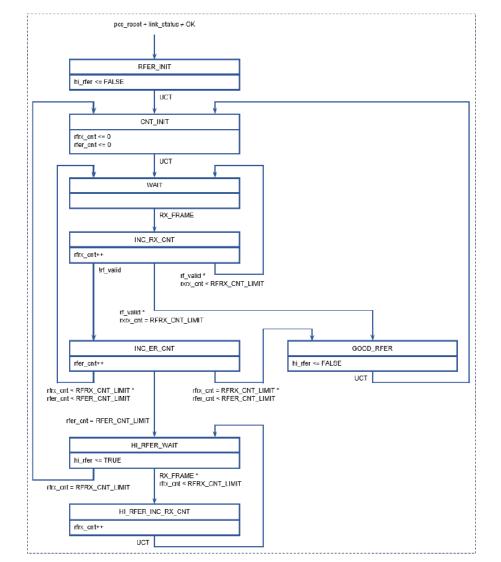
- Once wake signaling appears at the PMA to PCS interface alert\_detect become FALSE and the state diagram transitions to RX\_WAKE
  - The lpi\_rx\_wake\_timer allows the wake signal to propagate through the PCS receive path
  - When RS-FEC is enabled the propagation delay is large
  - Once the lpi\_rx\_wake\_timer expires the PCS receive function checks that the last 8 receive characters are all /l/ control symbols, and if not, the wake error counter is incremented





#### Figure 190–13B—PCS Receive state diagram, part b

- PCS Receive function RFER monitor
- This is based on clause 149 Figure 149-15 with some differences
  - RFER monitoring does not begin until the link is up
    - PHY control was designed to synchronize link establishment
  - We do not have a block\_lock signal
    - Under conditions of high RFER the link drops and we restart Auto-Negotiation
  - In clause 149 the counters are reset when the we enter receive LPI mode
    - We pause the counters but do nor reset them



NOTE-This figure is mandatory when RS-FEC is enabled for the link.

Figure 190–13C—RFER monitor state diagram

# Proposed Text for the Draft



- The following slides include the proposed changes to the text of draft 1.0 required for the draft
  - A number of sections, tables and state diagrams are completely new and are shown inside a blue outline text box 
    with a 'New Text' or 'New Figure' or 'New Table' pointer
  - Some sections have existing text that has been completely rewritten, in these cases the new text (inside 
    ) is shown side by side with the original text inside a red outline text box
  - Original text boxes have a header IEEE P802.3dg™/D1.0, 29th April 2025
    - Original text included for reference that is being kept, is shown inside a brown outline text box
- Note that there are additional Tables and Figures
  - The same numbering is used for existing tables and figures as used in draft 1.0 so that reference to existing draft 1.0 tables and figures is easier
  - New proposed figures have been given numbers 5p5, 13A, 13B and 13C, so that figures 14 and above have the same figure numbers as draft 1.0
  - The tables and figures will be renumbered in the draft
  - Reference to table or figures whose number will change in the draft are show in red



## ► Text changes for section 190.3.4 PCS Receive function

Replace text on page 73, lines 41 to 51 and page 74, lines 1 to 7

#### 190.3.4 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 190–13B. When RS-FEC is enabled for the link, the PHY Receive function shall implement the RFER monitor state diagram of Figure 190–13C.

New

Text

When the pcs\_rx\_mode parameter is TRAIN, the PCS Receive function checks the received PAM2 symbols and signals the reliable acquisition of the descrambler state by setting the scr\_status parameter of the PMA\_SCRSTATUS.request primitive to OK.

When the pcs\_rx\_mode parameter is TRAIN, and the config parameter is LEADER, and the loc\_rcvr\_status parameter is OK, the PCS Receive function monitors the received PAM2 symbols to determine whether the link partner is signaling reliable operation of its receive link. Once reliable operation of the receive link for the remote FOLLOWER is detected, this is communicated to the PHY Control function by setting the rem\_flr\_rcvr\_status parameter of the PMA\_REMFLRRXSTATUS.request primitive to OK.

When the pcs\_rx\_mode parameter is TRAIN, and the loc\_rcvr\_status parameter is OK, and the remote PHY is sending formatted training frames, the PCS Receive function attains frame and block synchronization based on the formatted training frame. The formatted training frame includes an alignment bit every 192 PAM2 symbols, which is aligned with the PCS partial frame boundary, as well as an InfoField, which is inserted into every 16th PCS partial frame. The PCS Receive function signals the detection of a valid InfoField to the PHY Control function by setting the rx\_info\_frame parameter of the PMA\_RXINFOFRAME.request primitive to TRUE.

IEEE P802.3dg<sup>™</sup>/D1.0, 29th April 2025

190.3.4 PCS Receive function

Editor's Note (to be removed prior to Working Group Ballot):

The text below is part of the description of the PCS Receive, but lacks the requirements and description of the PCS Receive state diagram operation which needs to be decided before that text can be written. Contributions are requested to fill out PCS Receive requirements before text is filled out here.

When the pcs\_rx\_mode parameter is TRAIN, the PCS Receive function checks the received PAM2 symbols and signals the reliable acquisition of the descrambler state by setting the scr\_status parameter of the PMA\_SCRSTATUS.request primitive to OK.

When the pcs\_rx\_mode parameter is TRAIN, and the config parameter is LEADER, the PCS Receive function continuously monitors the loc\_rcvr\_status parameter. Once loc\_rcvr\_status is set to OK, the PCS Receive function monitors the received PAM2 symbols to determine whether the link partner is signaling reliable operation of its receive link. Once reliable operation of the receive link for the remote PHY is detected, this is communicated to the PHY Control function by setting the rem\_rcvr\_status parameter of the PMA\_REMRXSTATUS.request primitive to OK.

When the pcs\_rx\_mode parameter is TRAIN, the PCS Synchronization process continuously monitors the loc\_rcvr\_status parameter. When loc\_rcvr\_status is set to OK, the PCS Synchronization process accepts

symbols via the PMA\_UNITDATA.indication primitive. It attains frame and block synchronization based on the formatted training frame structure and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block\_lock flag to indicate whether the PCS has obtained synchronization. The formatted training frame includes an alignment bit every 192 PAM2 symbols, which is aligned with the PCS partial frame boundary, as well as an InfoField, which is inserted in the 16th PCS partial frame. When the PCS Synchronization process is synchronized to this pattern, block\_lock is asserted. 34

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### Continue text changes for section 190.3.4 PCS Receive function

➢ Replace text on page 74, lines 14 to 25

New Text

When the pcs\_rx\_mode parameter is NORMAL, the PCS Receive function applies the inverse of the encoding processes described in 190.3.2 and depicted in Figure 190–5. Every 2N RX\_CLK cycles an (8N+1)B block is received and is decoded to generate a list of N characters each of which represents either a data octet or a control symbol. These characters are mapped one at a time into the rx\_char structure which is processed in accordance with Figure 190–13B to generate signals at the MII.

The PCS Receive function incorporates several means to detect error conditions. The PCS Receive state diagram detects packets that are not preceded by start-of-packet control symbols or are not followed by end-of-packet control symbols. When RS-FEC is enabled for the link, the RS-FEC frame error ratio (RFER) monitor process monitors the reliability of the RS decoder and asserts hi\_rfer to indicate an excessive RS-FEC frame error ratio. The PCS Receive function may use these detected error conditions to determine whether it is operating reliably and generates the pcs\_status variable accordingly. The precise algorithm for generation of pcs\_status is implementation dependent.

#### IEEE P802.3dg™/D1.0, 29th April 2025

<b>o</b> <i>i i</i>	
When the pcs_rx_mode parameter is NORMAL, the RS-FEC frame error ratio (RFER) monitor process	14
monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive	15
RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted	16
upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS	17
Receive process continuo usly accepts blocks. The PCS Receive process monitors these blocks and	18
generates RXD <3:0>, RX_DV and RX_ER on the MII.	19
	20
190.3.4.1 Frame and block synchronization	21
	22
190.3.4.2 PCS Receive descrambler	23
	24
190.3.4.3 Valid and invalid blocks	25



## ► Text for section 190.3.4.1 Invalid characters / 190.3.4.2 Block errors

> New section, insert the following text for section 190.3.4.1

#### 190.3.4.1 Invalid characters

When the pcs\_rx\_mode parameter is NORMAL, the PCS Receive function applies the inverse of the encoding processes described in 190.3.2 to generate a list of N received characters every 2N RX\_CLK cycles as described in 190.3.4. Errors during transmission can cause invalid characters to be received that could not have been transmitted. Received characters shall be identified as invalid characters in the following cases:

- a) The received character represents a control symbol with the numerical value 0x00.
- b) The received character represents the control symbol /LI/ when EEE is not enabled for the link.
- c) The received character is declared to be invalid due to a block error as specified in 190.3.4.2.

Invalid received characters shall be replaced with characters representing /E/ before the processing shown in Figure 190–13B is performed.

#### > New section, insert the following text for section 190.3.4.2

#### 190.3.4.2 Block errors

New Text

**New Text** 

While an (8N + 1)B block is being decoded an invalid pointer can be encountered. In this case all received characters from the corresponding octet position to the end of the block are declared to be invalid and handled as specified in 190.3.4.1.

If an (8N + 1)B block contains information from the payload of an RS-FEC codeword that cannot be decoded due to uncorrectable errors, then all received characters in that block are declared to be invalid and handled as specified in 190.3.4.1.



## ► Text for section 190.3.4.3 Character decoding

 $\geq$  New section, insert the following text for section 190.3.4.3

#### 190.3.4.3 Character decoding

The PCS Receive function decodes each received character into two MII transfers and shall follow Table 190–5p5.

 $\geq$  New table, Table 190–5p5— Character decoding

New Text



Received	Even Transfer			Odd Transfer		
Character	RX_DV	RX_ER	RXD<3:0>	RX_DV	RX_ER	RXD<3:0>
/E/	1	1	0000	1	1	0000
/I/	0	0	0000	0	0	0000
/Su/	0	0	0000	1	0	0101
/Tp/	0	0	0000	0	0	0000
/LI/	0	1	0001	0	1	0001
/R/	0	1	0100	0	1	0100
/Sp/	1	0	0101	1	0	0101
/Tu0/	1	0	0000	0	0	0000
/Tu1/	1	0	0001	0	0	0000
/Tu2/	1	0	0010	0	0	0000
/Tu3/	1	0	0011	0	0	0000
/Tu4/	1	0	0100	0	0	0000
/Tu5/	1	0	0101	0	0	0000
/Tu6/	1	0	0110	0	0	0000
/Tu7/	1	0	0111	0	0	0000
/Tu8/	1	0	1000	0	0	0000
/Tu9/	1	0	1001	0	0	0000
/TuA/	1	0	1010	0	0	0000
/TuB/	1	0	1011	0	0	0000
/TuC/	1	0	1100	0	0	0000
/TuD/	1	0	1101	0	0	0000
/TuE/	1	0	1110	0	0	0000
/TuF/	1	0	1111	0	0	0000
Data Value ROCT<7:0>	1	0	ROCT<3:0>	1	0	ROCT<7:4>

# Proposed Text for the Draft –State Diagrams



## Section 190.3.8.2 State diagrams

> State Diagrams and text for the PCS receive

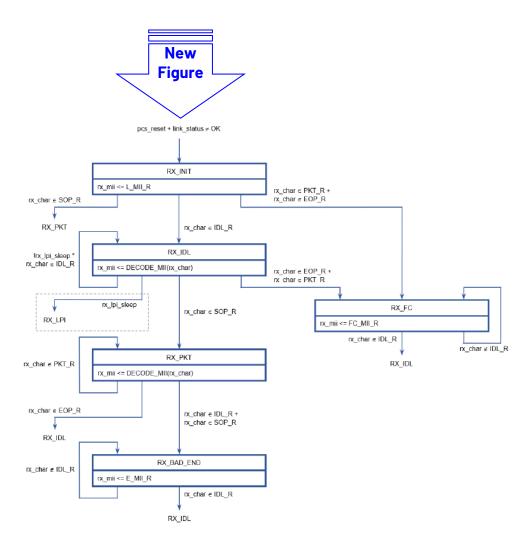
>Add intro text

New Text

The PCS Receive state diagram shown in Figure 190–13B controls the conversion of received characters to signals at the MII. It evaluates the exit conditions for the current state exactly once for every 2 cycles of

RX\_CLK except for the INC\_ERR\_CNT UCT exit condition, which is evaluated immediately after the INC\_ERR\_CNT state actions are complete.

▶ New Figure 190–13B—PCS Receive state diagram, part a



NOTE-Signals and functions shown with dashed lines are only required when EEE is enabled for the link.

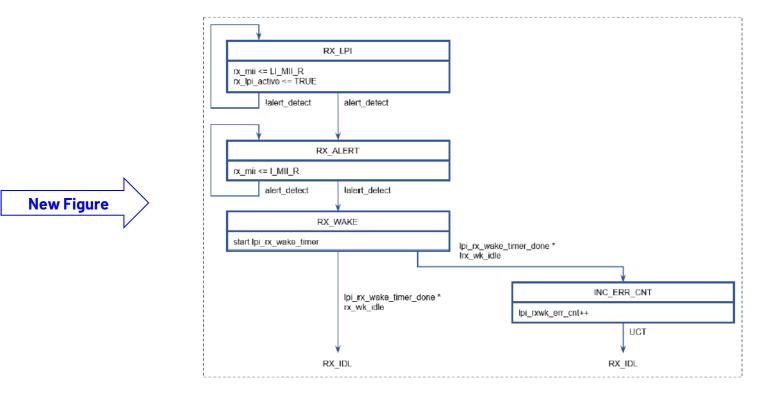
Figure 190–13B—PCS Receive state diagram, part a

## Proposed Text for the Draft –State Diagrams



### ► Continue section 190.3.8.2 State diagrams

- > Continue State Diagrams for the PCS receive
- ▶ New Figure 190–13B—PCS Receive state diagram, part b



NOTE-This figure is mandatory when EEE is enabled for the link.

#### Figure 190–13B—PCS Receive state diagram, part b

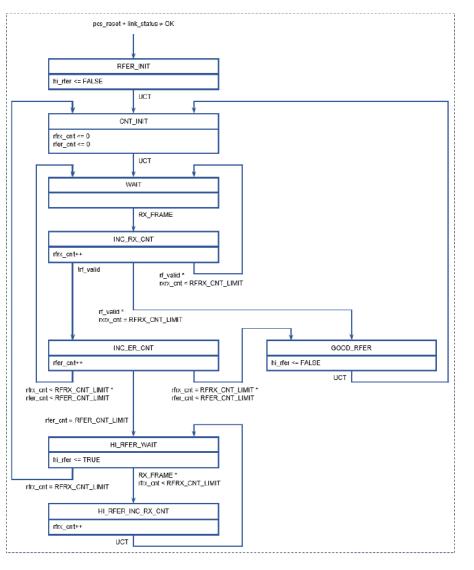
## Proposed Text for the Draft –State Diagrams





- > State Diagrams for the RFER monitor
- ➢ New Figure 190–13C—RFER monitor state diagram





NOTE-This figure is mandatory when RS-FEC is enabled for the link.

Figure 190–13C—RFER monitor state diagram

## Conclusions



- We have not had any presentation on the PCS Receive function and the text in draft 1.0 is just a placeholder
- This presentation describes the PCS Receive Operation and the main differences from previous clauses 149 and 165
- This presentation provides new text and tables for the PCS Receive function for the draft including the necessary state diagrams

Questions?