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Changes to the Text for the Draft for the Clause 45 Registers

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Introduction

- This presentation provides an update to the text and Tables for the draft for the clause 45 registers and for Annex 98B
  - There has been one presentations on the clause 45 registers for 100BASE-T1L
  - This addressed the PMA and PCS registers
- We have adopted one motion on clause 45 registers
  - March 2025 Motion #1:
    Move that the IEEE P802.3dg Task Force adopts slides 1 to 18 of Murray_3dg_03a_0312025 with editorial licenses
    - Complete Clause 45 register set for 100BASE-T1L based on 10BASE-T1L
- However, though this presentation makes a good start on the requirements for the clause 45 registers, there were some errors in this presentation as deriving the 100BASE-T1L registers from 10BASE-T1L is not fully correct
- This presentation proposes changes to complete this work

BASE-T1 PMA/PMD Control Register

- In March we proposed a change to add 100BASE-T1L to the type selection
  - See, slide 5 of Murray_3dg_03_03122025
- This was a mistake and this change is not required for 100BASE-T1L
  - The Type Selection bits are only used if Auto-negotiation is disabled
  - This change should be reverted and this section is not required

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Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x 1~~0~~ x = Reserved 1 0 0 1 = Reserved 1 0 0 0 = 100BASE-T1L 0 1 1 1 = 25GBASE-T1L 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

100BASE-T1L PMA Control Register

- This section should move to start before 1000BASE-T1
  - The register numbering should start at 1.2300, where there is a gap
    - This is between 10BASE-T1S and 1000BASE-T1
- Test mode transmit voltage amplitude control
  - Voltage control for test mode is in the PMA control register
  - This bit should be in the test mode control register
- EEE enable
  - In 100BASE-T1L support for EEE is advertised in the InfoField which has to be exchanged as part of link establishment
  - There is no reason to provide an override mechanism for EEE
- Loopback
  - This bit is for an internal PMA loopback, but in 10BASE-T1L this is an external loopback
  - An external loopback is a special test mode, so it is better to move this loopback enable bit to the test mode control register
- Transmit disable
  - In clause 146 the transmit disable bit is a copy of 1.9.0, but, 1.9.0 is a global PMD transmit disable
  - We do not believe that we should make this bit a copy of 1.9.0 as this is a PMA transmit disable

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45.2.1.251 100BASE-T1L PMA control register (Register 1.2318)

The assignment of bits in the 100BASE-T1L PMA control register is shown in Table 45–212a.

Table 45–212a—100BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2318.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2318.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2318.13	Reserved	Value always zero	RO
1.2318.12	Test mode transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2318.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2318.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2318.9:1	Reserved	Value always 0	RO
1.2318.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a] RO = Read only, R/W = Read/Write, SC = Self-clearing.

100BASE-T1L PMA Status Register

- Loopback ability
  - This is not required since external loopback can always be implemented by disconnecting the cable
    - All other loopback requirements are implemented digitally and are always supported
- 2.4 Vpp operating mode ability
  - This bit should be called **Increased transmit/receive level ability**
- EEE ability
  - In 100BASE-T1L this bit should be in the PCS
  - This bit should be moved to the 100BASE-T1L PCS status register
- Receive fault ability and Receive fault
  - These indications are provided by register 1.8 (PMA/PMD status 2) which also provides Transmit fault ability and Transmit fault and there is an inconsistency in that Tx ability/fault do not exist in this PMA status register
  - The Receive fault ability /fault bits should be removed from the 100BASE-T1L PMA status register
- Receive link status
  - This is really PHY link up not PMA receive link up
  - The description should be PHY receive link up/down

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Table 45–212b—100BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2319.15:14	Reserved	Value always 0	RO
1.2319.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2319.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2319.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2319.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2319.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2319.8:3	Reserved	Value always 0	RO
1.2319.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2319.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2319.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL

[a] RO = Read only, LL = Latching low, LH = Latching high.

100BASE-T1L Test Mode Control Register

Test modes

- Expand the number of possible test modes to 16
  - Expand to 4 bits, 15:12 for Test mode control
  - Add bit 11 for Test mode transmitter LEADER/FOLLOWER configuration
  - A test mode cannot be selected that is not consistent with the supported abilities

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Table 45–212c—100BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2320.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2320.12:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write.

Possible test modes for 100BASE-T1L

- We are considering the following test mode

- *Test mode 1: Jitter*
- *Test mode 2: Jitter with increased transmit level*
- *Test mode 3: Droop*
- *Test mode 4: Droop with increased transmit level*
- *Test mode 5: Formatted training sequence*
- *Test mode 6: Formatted training sequence with increased transmit level*
- *Test mode 7: Idle with RS-FEC disabled*
- *Test mode 8: Idle with RS-FEC disabled and with increased transmit level*
- *Test mode 9: Idle with RS-FEC enabled*
- *Test mode 10: Idle with RS-FEC enabled and with increased transmit level*
- *Test mode 11: External loopback with RS-FEC disabled*
- *Test mode 12: External loopback with RS-FEC disabled and with increased transmit level*
- *Test mode 13: External loopback with RS-FEC enabled*
- *Test mode 14: External loopback with RS-FEC enabled and with increased transmit level*

100BASE-T1L PCS Control Register

- Register numbering
  - The register numbering should start at 3.2295, where there is a gap
    - This is between 10BASE-T1S and 1000BASE-T1
- Loopback
  - This bit should not be a copy of bit 3.0.14 (Loopback) as this is a control bit and should just be for 100BASE-T1L
- Loopback default
  - Some registers specify a default value and some don't
  - Ideally this should be consistent and in a common section
  - Do not specify the default value of the Loopback bit

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Table 45–297a—100BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2280.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2280.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2280.13:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write, SC = Self-clearing.

100BASE-T1L PCS Status Register

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Table 45–297b—100BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2281.15	Reserved	Value always 0	RO
3.2281.14	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.13	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.12	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.11	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.10	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2281.9	Reserved	Value always 0	RO
3.2281.8	100BASE-T1L EEE capability	1 = PHY has 100BASE-T1L EEE capability 0 = PHY does not have 100BASE-T1L EEE capability	RO
3.2281.7	100BASE-T1L RS-FEC capability	1 = PHY has 100BASE-T1L RS-FEC capability 0 = PHY does not have 100BASE-T1L RS-FEC capability	RO
3.2281.6	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2281.5:0	Reserved	Value always 0	RO

[a] RO = Read only, LH = Latching high, LL = Latching low.

- Tx/Rx LPI received / indication
  - The indication/received for transmit and receive LPI is available in 3.1.11:8 (PCS status 1 register) and there is no need to duplicate
  - ➢ We should remove the Tx/Rx LPI received / indication bits from the 100BASE-T1L PCS status register
- Fault
  - It is not specified what this fault condition is, so we either should remove or define what the fault condition is
  - ➢ The fault bit should be removed from the 100BASE-T1L PCS status register
- EEE / RS-FEC capability
  - In the 10BASE-T1L PCS status register, bits 8 and 7 are used for Rx LPI Indication and Fault, it would be better to use different bit positions
  - ➢ We should move the EEE / RS-FEC capability bits to bits 15 and 14
- PCS receive link status
  - In draft 1.0 this bit indicates scr_status, which is not a good indicator of the PSC receive function health as it does not take into account the operation of the RS-FEC decoder or the (8N)B/(8N + 1)B decoder
  - ➢ Use this bit to report pcs_status, which indicates if the PCS is operating reliably

100BASE-T1L Advertisement Register

- 100BASE-T1L advertisement register bit definitions
  - For consistency with previous clauses this should be called a training register
  - ➢ Rename to 100BASE-T1L training register bit definitions
- Supported abilities
  - It should only be possible to advertise an ability if that ability is supported (in the PCS status register)
  - ➢ Only bits representing supported abilities may be set
- Capability
  - Some previous clauses have used ‘capability’ and some have used ‘ability’
  - ➢ Propose we use ability for 100BASE-T1L

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Table 45–297c—100BASE-T1L advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2282.15:2	Reserved	Value always 0	RO
3.2282.1	100BASE-T1L EEE advertisement	1 = 100BASE-T1L EEE capability advertised to link partner 0 = 100BASE-T1L EEE capability not advertised to link partner	R/W
3.2282.0	100BASE-T1L RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised to link partner 0 = 100BASE-T1L RS-FEC capability not advertised to link partner	R/W

[a] RO = Read only, R/W = Read/Write.

100BASE-T1L Link Partner Advertisement Register

- 100BASE-T1L link partner advertisement register bit definitions
  - For consistency with previous clauses this should be called a training register
  - ➢ Rename to 100BASE-T1L link partner training register bit definitions
- Capability
  - Some previous clauses have used ‘capability’ and some have used ‘ability’
  - ➢ Propose we use ability for 100BASE-T1L

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Table 45–297d—100BASE-T1L ink partner advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2283.15:2	Reserved	Value always 0	RO
3.2283.1	100BASE-T1L link partner EEE advertisement	1 = 100BASE-T1L EEE capability advertised by link partner 0 = 100BASE-T1L EEE capability not advertised by link partner	RO
3.2283.0	100BASE-T1L link partner RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised by link partner 0 = 100BASE-T1L RS-FEC capability not advertised by link partner	RO

[a] RO = Read only.

Annex 98B

- Advertisement of 100BASE-T1L abilities
  - In 10BASE-T1 registers 7.526 and 7.527 were added to allow the 10BASE-T1L / 10BASE-T1S abilities to be written and the corresponding link partner abilities to be read
  - This is unnecessary because these are already accessible by registers
    - Registers 7.514, 7.515 and 7.516 allow the advertised abilities to be written
    - Registers 7.517, 7.518 and 7.519 allow the link partner advertised abilities to be read
  - ➢ We do not need to add any new registers for the advertisement of 100BASE-T1L abilities
- Annex 98B
  - We do need to extend the technology ability field bit field (D21 to D47 equivalent to A0 to A26)
  - ➢ We need to add 100BASE-T1L ability in A10
  - ➢ And need to add 100BASE-T1L ability increased transmit/receive level ability in A21

Proposed Text for the Draft

Proposed Text for the Draft

- The following slides include the proposed changes to the text of draft 1.0 required for the draft
  - A number of sections, tables and state diagrams are completely new and are shown inside a blue outline text box with a 'New Text' or 'New Table' pointer
  - Some sections have existing text that has been completely rewritten, in these cases the new text (inside) is shown side by side with the original text inside a red outline text box
  - Original text boxes have a header *IEEE P802.3dg™/D1.0, 29th April 2025*
    - Original text included for reference that is being kept, is shown inside a brown outline text box

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)
  - Reverted change to BASE-T1 PMA/PMD control register
  - Remove section 45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100) from the draft
    - Remove Table 45–178—BASE-T1 PMA/PMD control register bit definitions from the draft

Delete sections

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45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

Change Table 45–178 (as modified by IEEE Std 802.3cy-2023) as shown (unchanged rows not shown):

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x ~~1~~x x = Reserved 1 0 0 1 = Reserved 1 0 0 0 = 100BASE-T1L 0 1 1 1 = 25GBASE-T1L 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a] RO = Read only, R/W = Read/Write.

Change 45.2.1.214.2 (as modified by IEEE Std 802.3cy-2023) as shown:

45.2.1.214.2 Type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are set to 0010, the mode of operation is 100BASE-T1L. When these bits are set to 0011, the mode of operation is 10BASE-T1S. When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1. When these bits are set to 0111, the mode of operation is 25GBASE-T1. When these bits are set to 1000, the mode of operation is 100BASE-T1L. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

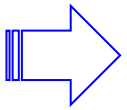
Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.1.237 100BASE-T1L PMA control register (Register 1.2300)
  - This section should move to start before the current section 45.2.1.237, which is 1000BASE-T1, update note on page 28, line 1 to 2

Insert new subclauses 45.2.1.251, 45.2.1.252, and 45.2.1.253 (including Tables and subclauses) after 45.2.1.250 (and its subclause) as follows:

  - The Table numbering should follow in sequence
  - The register numbering for the PMA registers should start at 1.2300, where there is a gap
  - Replace the rows for bits 12, 10 and 0 of Table 45–212a with Reserved rows

1.2318.12	Test mode transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2318.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2318.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W



Reserved	Value always zero	RO

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.237 100BASE-T1L PMA control register (Register 1.2300)
  - Update Table 45–212a—100BASE-T1L PMA control register bit definitions

Update Table

45.2.1.237 100BASE-T1L PMA control register (Register 1.2300)

The assignment of bits in the 100BASE-T1L PMA control register is shown in Table 45–.

Table 45–199—100BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2300.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2300.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2300.13:12	Reserved	Value always 0	RO
1.2300.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2300.10:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write, SC = Self-clearing.

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45.2.1.251 100BASE-T1L PMA control register (Register 1.2318)

The assignment of bits in the 100BASE-T1L PMA control register is shown in Table 45–212a.

Table 45–212a—100BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2318.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2318.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2318.13	Reserved	Value always zero	RO
1.2318.12	Test mode transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2318.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2318.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2318.9:1	Reserved	Value always 0	RO
1.2318.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a] RO = Read only, R/W = Read/Write, SC = Self-clearing.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.237 100BASE-T1L PMA control register (Register 1.2300)
  - Delete text on page 29, line 9 to 10

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45.2.1.251.2 Transmit disable (1.2318.14)

When bit 1.2318.14 is set to one, the PMA shall disable output on the transmit path. When bit 1.2318.14 is set to zero, the PMA shall enable output on the transmit path.

Delete text

Bit 1.2318.14 is a copy of bit 1.9.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.237 100BASE-T1L PMA control register (Register 1.2300)
  - Delete section 45.2.1.251.3 Test mode transmit voltage amplitude control (1.2318.12)
  - Delete section 45.2.1.251.5 EEE enable (1.2318.10)
  - Delete section 45.2.1.251.6 Loopback (1.2318.0)

Delete sections

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45.2.1.251.3 Test mode transmit voltage amplitude control (1.2318.12)

Bit 1.2318.12 is used to set the 2.4 Vpp operating mode when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2318.12 is set to one, the PHY shall operate in 2.4 Vpp operating mode according to 146.5.4.1. If bit 1.2318.12 is set to zero, the PHY shall operate in 1.0 Vpp operating mode according to 146.5.4.1. The default value of bit 1.2318.12 is zero. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.251.5 EEE enable (1.2318.10)

Bit 1.2318.10 is used to enable EEE functionality when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2318.10 is set to one, the PHY shall operate with EEE enabled. If bit 1.2318.10 is set to zero, the PHY shall operate with EEE disabled. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one. The default value of bit 1.2318.10 is zero.

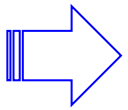
45.2.1.251.6 Loopback (1.2318.0)

The 100BASE-T1L PMA shall be placed in near-end loopback mode of operation when bit 1.2318.0 is set to one. When in loopback mode, the 100BASE-T1L PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2318.0 is zero. Bit 1.2318.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.1.252 100BASE-T1L PMA status register (Register 1.2319)
  - Replace rows for bits 13, 10, 9 and 1 of Table 45–212b with Reserved rows

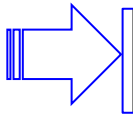
1.2319.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2319.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2319.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2319.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH



Reserved	Value always zero		RO

  - Update text and description for bit 12 of Table 45–212b

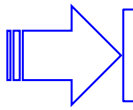
1.2319.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO



1.2301.12	Increased transmit/receive level ability	1 = PMA has increased transmit/receive level ability 0 = PMA does not have increased transmit/receive level ability	RO

  - Update description for bit 0 of Table 45–212b

1.2319.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL



1.2301.0	Receive link status	1 = PHY receive link up 0 = PHY receive link down	RO/LL

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.252 100BASE-T1L PMA status register (Register 1.2319)
  - Update Table 45–212b—100BASE-T1L PMA status register bit definitions

Table 45–200—100BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2301.15:13	Reserved	Value always 0	RO
1.2301.12	Increased transmit/receive level ability	1 = PMA has increased transmit/receive level ability 0 = PMA does not have increased transmit/receive level ability	RO
1.2301.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2301.10:3	Reserved	Value always 0	RO
1.2301.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2301.1	Reserved	Value always 0	RO
1.2301.0	Receive link status	1 = PHY receive link up 0 = PHY receive link down	RO/LL

[a] RO = Read only, LL = Latching low, LH = Latching high.

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Table 45–212b—100BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2319.15:14	Reserved	Value always 0	RO
1.2319.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2319.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2319.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2319.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2319.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2319.8:3	Reserved	Value always 0	RO
1.2319.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2319.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2319.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL

[a] RO = Read only, LL = Latching low, LH = Latching high.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.1.252 100BASE-T1L PMA status register (Register 1.2319)
  - Update section 45.2.1.252.2 2.4 Vpp operating mode ability (1.2319.12)
    - Replace text on page 30, lines 40 to 45 with new text

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45.2.1.252.2 2.4 Vpp operating mode ability (1.2319.12)

When read as a one, this bit indicates that the 100BASE-T1L PHY supports a transmit level of 2.4 Vpp. When read as a zero, this bit indicates that the 100BASE-T1L PHY does not support a transmit level of 2.4 Vpp.

New Text

45.2.1.238.1 Increased transmit/receive level ability (1.2301.12)

When read as a one, this bit indicates that the 100BASE-T1L PHY supports an increased transmit/receive level as defined in 190.5.4.1. When read as zero, this bit indicates that the 100BASE-T1L PHY does not support an increased transmit/receive level.

  - Update section 45.2.1.252.6 Receive polarity (1.2319.2)
    - Replace text on page 31, lines 12 to 15 with new text

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45.2.1.252.6 Receive polarity (1.2319.2)

When read as a zero, bit 1.2319.2 indicates that the polarity of the receiver is not reversed. When read as a one, bit 1.2319.2 indicates that the polarity of the receiver is reversed.

New Text

45.2.1.238.3 Receive polarity (1.2301.2)

When read as a one, bit 1.2301.2 indicates that the polarity of the receiver is reversed. When read as zero, bit 1.2301.2 indicates that the polarity of the receiver is not reversed.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.252 100BASE-T1L PMA status register (Register 1.2319)
  - Delete section 45.2.1.252.1 Loopback ability (1.2319.13)
  - Delete section 45.2.1.252.4 EEE ability (1.2319.10)
  - Delete section 45.2.1.252.5 Receive fault ability (1.2319.9)
  - Delete section 45.2.1.252.7 Receive fault (1.2319.1)

Delete sections

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45.2.1.252.1 Loopback ability (1.2319.13)

When read as a one, this bit indicates that the 100BASE-T1L PHY supports PMA loopback. When read as a zero, this bit indicates that the 100BASE-T1L PHY does not support PMA loopback.

45.2.1.252.4 EEE ability (1.2319.10)

When read as a one, this bit indicates that the 100BASE-T1L PHY supports EEE. When read as a zero, this bit indicates that the 100BASE-T1L PHY does not support EEE.

45.2.1.252.5 Receive fault ability (1.2319.9)

When read as a one, bit 1.2319.9 indicates that the 100BASE-T1L PMA has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2319.9 indicates that the 100BASE-T1L PMA does not have the ability to detect a fault condition on the receive path.

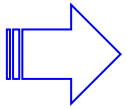
45.2.1.252.7 Receive fault (1.2319.1)

When read as a one, bit 1.2319.1 indicates that the 100BASE-T1L PMA has detected a fault condition on the receive path. When read as a zero, bit 1.2319.1 indicates that the 100BASE-T1L PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2319.9. The 100BASE-T1L PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.1.253 100BASE-T1L test mode control register (Register 1.2320)
  - Replace row for bits 15:13 of Table 45–212c with a row for bits 15:12

1.2320.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W



1.2302.15:12	Test mode control	1 1 0 0 = Test mode 14 1 1 0 0 = Test mode 13 1 1 0 0 = Test mode 12 1 0 1 1 = Test mode 11 1 0 1 0 = Test mode 10 1 0 0 1 = Test mode 9 1 0 0 0 = Test mode 8 0 1 1 1 = Test mode 7 0 1 1 0 = Test mode 6 0 1 0 1 = Test mode 5 0 1 0 0 = Test mode 4 0 0 1 1 = Test mode 3 0 0 1 0 = Test mode 2 0 0 0 1 = Test mode 1 0 0 0 0 = Normal (non-test) operation	R/W

  - New row for bit 11 of Table 45–212c

1.2302.11	Test mode transmitter LEADER/FOLLOWER configuration	1 = PHY transmits as LEADER 0 = PHY transmits as FOLLOWER	R/W

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.253 100BASE-T1L test mode control register (Register 1.2320)
  - Update Table 45–212c—100BASE-T1L test mode control register bit definitions

Update Table

Table 45–201—100BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2302.15:12	Test mode control	1 1 0 0 = Test mode 14 1 1 0 0 = Test mode 13 1 1 0 0 = Test mode 12 1 0 1 1 = Test mode 11 1 0 1 0 = Test mode 10 1 0 0 1 = Test mode 9 1 0 0 0 = Test mode 8 0 1 1 1 = Test mode 7 0 1 1 0 = Test mode 6 0 1 0 1 = Test mode 5 0 1 0 0 = Test mode 4 0 0 1 1 = Test mode 3 0 0 1 0 = Test mode 2 0 0 0 1 = Test mode 1 0 0 0 0 = Normal (non-test) operation	R/W
1.2302.11	Test mode transmitter LEADER/FOLLOWER configuration	1 = PHY transmits as LEADER 0 = PHY transmits as FOLLOWER	R/W
1.2302.10:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write.

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Table 45–212c—100BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2320.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2320.12:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.1.253 100BASE-T1L test mode control register (Register 1.2320)
  - Add new sentence on page 32, after line 4

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45.2.1.253.1 Test mode control (1.2320.15:13)

Transmitter test mode operations defined by bits 1.2320.15:13 are described in 190.5.2. The default value for bits 1.2320.15:13 is zero.

New Text

45.2.1.239.1 Test mode control (1.2302.15:12)

Transmitter test mode operations defined by bits 1.2302.15:12, are described in 190.5.2. The default value for bits 1.2302.15:12 is zero. If a value that is not consistent with the supported abilities is written to 1.2302.15:12, then bits 1.2302.15:12 are reset to zero.

  - New section, insert the following text for section 45.2.1.239.1(bit 11)

New Text

45.2.1.239.1 Test mode transmitter LEADER/FOLLOWER configuration (1.2302.11)

When bit 1.2302.11 is set to one, the PHY transmits as LEADER when operating in test modes 5 to 14. When bit 1.2302.11 is set to zero, the PHY transmits as FOLLOWER when operating in test modes 5 to 14

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.3.71a 100BASE-T1L PCS control register (Register 3.2280)
  - The register numbering for the PCS registers should start at 1.2295, where there is a gap
    - This between 10BASE-T1S and before 1000BASE-T1
  - Delete text on page 33, line 19 to 23

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45.2.3.71a.2 Loopback (3.2280.14)

The 100BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2280.14 is set to one. When in loopback mode, the 100BASE-T1L PCS shall accept data on the transmit path and return it on the receive path.

Delete text

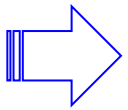
The default value of bit 3.2280.14 is zero.

Bit 3.2280.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.3.71b 100BASE-T1L PCS status register (Register 3.2281)
  - Replace rows for bits 14, 13, 12, 11 and 10 of Table 45–297b with Reserved rows

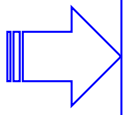
3.2281.14	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.13	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.12	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.11	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.10	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH



Reserved	Value always zero	RO

  - Move bits 8 & 7 of Table 45–297b to bits 15 & 14 and update text and description

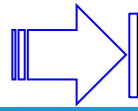
3.2281.8	100BASE-T1L EEE capability	1 = PHY has 100BASE-T1L EEE capability 0 = PHY does not have 100BASE-T1L EEE capability	RO
3.2281.7	100BASE-T1L RS-FEC capability	1 = PHY has 100BASE-T1L RS-FEC capability 0 = PHY does not have 100BASE-T1L RS-FEC capability	RO



3.2296.15	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
3.2296.14	RS-FEC ability	1 = PCS has RS-FEC ability 0 = PCS does not have RS-FEC ability	RO

  - Update description for bit 6 of Table 45–297b

3.2281.6	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL



3.2296.6	PCS status	1 = PCS status is OK 0 = PCS status is not OK	

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71b 100BASE-T1L PCS status register (Register 3.2281)
  - Update Table 45–297b—100BASE-T1L PCS status register bit definitions

Table 45–303—100BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2296.15	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
3.2296.14	RS-FEC ability	1 = PCS has RS-FEC ability 0 = PCS does not have RS-FEC ability	RO
3.2296.13:7	Reserved	Value always 0	RO
3.2296.6	PCS status	1 = PCS status is OK 0 = PCS status is not OK	
3.2296.5:0	Reserved	Value always 0	RO

[a] RO = Read only.

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Table 45–297b—100BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2281.15	Reserved	Value always 0	RO
3.2281.14	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.13	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2281.12	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.11	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2281.10	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2281.9	Reserved	Value always 0	RO
3.2281.8	100BASE-T1L EEE capability	1 = PHY has 100BASE-T1L EEE capability 0 = PHY does not have 100BASE-T1L EEE capability	RO
3.2281.7	100BASE-T1L RS-FEC capability	1 = PHY has 100BASE-T1L RS-FEC capability 0 = PHY does not have 100BASE-T1L RS-FEC capability	RO
3.2281.6	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2281.5:0	Reserved	Value always 0	RO

[a] RO = Read only, LH = Latching high, LL = Latching low.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71b 100BASE-T1L PCS status register (Register 3.2281)
  - Update sections 45.2.3.71b.6 100BASE-T1L EEE capability (3.2281.8), 45.2.3.71b.7 100BASE-T1L RS-FEC capability (3.2281.7) and 45.2.3.71b.8 PCS receive link status (3.2281.6)
    - Replace text on page 35, lines 1 to 16 with new text

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45.2.3.71b.6 100BASE-T1L EEE capability (3.2281.8)

When read as a one, bit 3.2281.8 indicates that the PHY supports 100BASE-T1L EEE. When read as a zero, bit 3.2281.8 indicates that the PHY does not support 100BASE-T1L EEE.

45.2.3.71b.7 100BASE-T1L RS-FEC capability (3.2281.7)

When read as a one, bit 3.2281.7 indicates that the PHY supports 100BASE-T1L RS-FEC. When read as a zero, bit 3.2281.7 indicates that the PHY does not support 100BASE-T1L RS-FEC.

45.2.3.71b.8 PCS receive link status (3.2281.6)

When read as a one, bit 3.2281.6 indicates that the 100BASE-T1L PCS receive link is up. When read as a zero, bit 3.2281.6 indicates that the 100BASE-T1L PCS receive link was down since the last read from this bit. This bit shall be implemented with latching low behavior and is a reflection of the variable scr_status. If the bit is read while scr_status = OK, then this bit is set. If scr_status = NOT_OK, then this bit is reset.

New Text

45.2.3.77.1 EEE ability (3.2296.15)

When read as one, this bit indicates that the 100BASE-T1L PHY supports EEE. When read as zero, this bit indicates that the 100BASE-T1L PHY does not support EEE.

45.2.3.77.2 RS-FEC ability (3.2296.14)

When read as one, this bit indicates that the 100BASE-T1L PHY supports RS-FEC. When read as zero, this bit indicates that the 100BASE-T1L PHY does not support RS-FEC.

45.2.3.77.3 PCS status (3.2296.6)

When read as one, this bit indicates that the 100BASE-T1L pcs_status parameter, specified in 190.2.2.7, is OK. When read as zero, this bit indicates that the 100BASE-T1L pcs_status parameter is NOT_OK.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.3.71c 100BASE-T1L advertisement register (Register 3.2282)
  - Rename to 100BASE-T1L training register for consistency with previous clauses

Table 45–304—100BASE-T1L training register bit definitions

Bit(s)	Name	Description	R/W[a]

  - Replace text on page 35, lines 18 to 22 with new text

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45.2.3.71c 100BASE-T1L advertisement register (Register 3.2282)

The assignment of bits in the 100BASE-T1L advertisement register is shown in Table 45–297c. The default value for each bit of the 100BASE-T1L advertisement register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

New Text

45.2.3.78 100BASE-T1L training register (3.2297)

The 100BASE-T1L training register determines the abilities that are advertised to the link partner during training. Only bits representing supported abilities may be set. The assignment of bits in the 100BASE-T1L training register is shown in Table 45–304.

  - Move bits 1 & 0 of Table 45–297c to bits 15 & 14 and update text and description

3.2282.1	100BASE-T1L EEE advertisement	1 = 100BASE-T1L EEE capability advertised to link partner 0 = 100BASE-T1L EEE capability not advertised to link partner	R/W
3.2282.0	100BASE-T1L RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised to link partner 0 = 100BASE-T1L RS-FEC capability not advertised to link partner	R/W

3.2297.15	EEE advertisement	1 = EEE ability is advertised to the link partner 0 = EEE ability is not advertised to the link partner	R/W
3.2297.14	RS-FEC advertisement	1 = RS-FEC ability is advertised to the link partner 0 = RS-FEC ability is not advertised to the link partner	R/W

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71c 100BASE-T1L advertisement register (Register 3.2282)
  - Update Table 45–297c—100BASE-T1L advertisement register bit definitions

Table 45–304—100BASE-T1L training register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2297.15	EEE advertisement	1 = EEE ability is advertised to the link partner 0 = EEE ability is not advertised to the link partner	R/W
3.2297.14	RS-FEC advertisement	1 = RS-FEC ability is advertised to the link partner 0 = RS-FEC ability is not advertised to the link partner	R/W
3.2297.13:0	Reserved	Value always 0	RO

[a] RO = Read only, R/W = Read/Write.

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Table 45–297c—100BASE-T1L advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2282.15:2	Reserved	Value always 0	RO
3.2282.1	100BASE-T1L EEE advertisement	1 = 100BASE-T1L EEE capability advertised to link partner 0 = 100BASE-T1L EEE capability not advertised to link partner	R/W
3.2282.0	100BASE-T1L RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised to link partner 0 = 100BASE-T1L RS-FEC capability not advertised to link partner	R/W

[a] RO = Read only, R/W = Read/Write.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71c 100BASE-T1L advertisement register (Register 3.2282)
  - Update sections 45.2.3.71c.1 100BASE-T1L EEE advertisement (3.2282.1) and 45.2.3.71c.2 100BASE-T1L RS-FEC advertisement (3.2282.0)
    - Replace text on page 35, lines 1 to 16 with new text

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45.2.3.71c.1 100BASE-T1L EEE advertisement (3.2282.1)

When set as a one, bit 3.2282.1 indicates to the link partner that the 100BASE-T1L PHY is advertising 100BASE-T1L EEE capability. When set as a zero, bit 3.2282.1 indicates to the link partner that the 100BASE-T1L PHY is not advertising 100BASE-T1L EEE capability. This bit shall be set to zero if the 100BASE-T1L PHY does not support 100BASE-T1L EEE.

45.2.3.71c.2 100BASE-T1L RS-FEC advertisement (3.2282.0)

When set as a one, bit 3.2282.0 indicates to the link partner that the 100BASE-T1L PHY is advertising 100BASE-T1L RS-FEC capability. When set as a zero, bit 3.2282.0 indicates to the link partner that the 100BASE-T1L PHY is not advertising 100BASE-T1L RS-FEC capability. This bit shall be set to zero if the 100BASE-T1L PHY does not support 100BASE-T1L RS-FEC.

New Text

45.2.3.78.1 EEE advertisement (3.2297.15)

When bit 3.2297.15 is set to one, the 100BASE-T1L PHY advertises EEE ability to the link partner during training.

45.2.3.78.2 RS-FEC advertisement (3.2297.14)

When bit 3.2297.14 is set to one, the 100BASE-T1L PHY advertises RS-FEC ability to the link partner during training.

Proposed Text for the Draft – Clause 45 Registers

- Text change for section 45.2.3.71d 100BASE-T1L link partner advertisement register (Register 3.2283)
  - Rename to 100BASE-T1L training register for consistency with previous clauses

Table 45–305—100BASE-T1L link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]

  - Replace text on page 36, lines 1 to 6 with new text

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45.2.3.71d 100BASE-T1L link partner advertisement register (Register 3.2283)

The assignment of bits in the 100BASE-T1L link partner advertisement register is shown in Table 45–297d. All the bits in the 100BASE-T1L link partner advertisement register are read only; a write to the 100BASE-T1L link partner advertisement register shall have no effect.

New Text

45.2.3.79 100BASE-T1L link partner training register (3.2298)

The assignment of bits in the 100BASE-T1L training register is shown in .

  - Move bits 1 & 0 of Table 45–297d to bits 15 & 14 and update text and description

3.2283.1	100BASE-T1L link partner EEE advertisement	1 = 100BASE-T1L EEE capability advertised by link partner 0 = 100BASE-T1L EEE capability not advertised by link partner	RO
3.2283.0	100BASE-T1L link partner RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised by link partner 0 = 100BASE-T1L RS-FEC capability not advertised by link partner	RO

3.2298.15	Link partner EEE advertisement	1 = EEE ability is advertised by the link partner 0 = EEE ability is not advertised by the link partner	RO
3.2298.14	Link partner RS-FEC advertisement	1 = RS-FEC ability is advertised by the link partner 0 = RS-FEC ability is not advertised by the link partner	RO

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71d 100BASE-T1L link partner advertisement register (Register 3.2283)
  - Update Table 45–297c—100BASE-T1L advertisement register bit definitions

Table 45–305—100BASE-T1L link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2298.15	Link partner EEE advertisement	1 = EEE ability is advertised by the link partner 0 = EEE ability is not advertised by the link partner	RO
3.2298.14	Link partner RS-FEC advertisement	1 = RS-FEC ability is advertised by the link partner 0 = RS-FEC ability is not advertised by the link partner	RO
3.2298.13:0	Reserved	Value always 0	RO

[a] RO = Read only.

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Table 45–297d—100BASE-T1L ink partner advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2283.15:2	Reserved	Value always 0	RO
3.2283.1	100BASE-T1L link partner EEE advertisement	1 = 100BASE-T1L EEE capability advertised by link partner 0 = 100BASE-T1L EEE capability not advertised by link partner	RO
3.2283.0	100BASE-T1L link partner RS-FEC advertisement	1 = 100BASE-T1L RS-FEC capability advertised by link partner 0 = 100BASE-T1L RS-FEC capability not advertised by link partner	RO

[a] RO = Read only.

Proposed Text for the Draft – Clause 45 Registers

- Continue text change for section 45.2.3.71d 100BASE-T1L link partner advertisement register (Register 3.2283)
  - Update sections 45.2.3.71d.1 100BASE-T1L link partner EEE advertisement (3.2283.1) and 45.2.3.71d.2 100BASE-T1L link partner RS-FEC advertisement (3.2283.0)
    - Replace text on page 36, lines 25 to 35 with new text

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45.2.3.71d.1 100BASE-T1L link partner EEE advertisement (3.2283.1)

When read as a one, bit 3.2283.1 indicates that the 100BASE-T1L link partner is advertising 100BASE-T1L EEE capability. When read as a zero, bit 3.2283.1 indicates that the 100BASE-T1L link partner is not advertising 100BASE-T1L EEE capability.

45.2.3.71d.2 100BASE-T1L link partner RS-FEC advertisement (3.2283.0)

When read as a one, bit 3.2283.0 indicates that the 100BASE-T1L link partner is advertising 100BASE-T1L RS-FEC capability. When read as a zero, bit 3.2283.0 indicates that the 100BASE-T1L link partner is not advertising 100BASE-T1L RS-FEC capability.

25 26 27 28 29 30 31 32 33 34 35

New Text

45.2.3.79.1 Link partner EEE advertisement (3.2298.15)

When read as one, bit 3.2298.15, indicates that EEE ability is advertised by the link partner during training.

45.2.3.79.2 Link partner RS-FEC advertisement (3.2298.14)

When read as one, bit 3.2298.14, indicates that RS-FEC ability is advertised by the link partner during training.

Proposed Text for the Draft – Annex 98B

- New section Annex 98B
  - New text for Annex 98B and associated sub-sections
  - New entries in Table 98B–1—Technology Ability Field bit assignments for 100BASE-T1L
    - Add A10, 100BASE-T1L ability
    - Add A21, 100BASE-T1L ability increased transmit/receive level ability

Annex 98B

IEEE 802.3 Selector Base Page definition

98B.3 Technology Ability Field bit assignments

Table 98B–1—Technology Ability Field bit assignments

Bit	Selector description
…	
A10	100BASE-T1L ability
A9 through A20	
A21	100BASE-T1L increased transmit/receive level ability
…	

Conclusions

- This presentation provides an update to the text and Tables for the draft for the clause 45 registers and for Annex 98B

Questions ?