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Delay Constraints and LPI Timing Parameters

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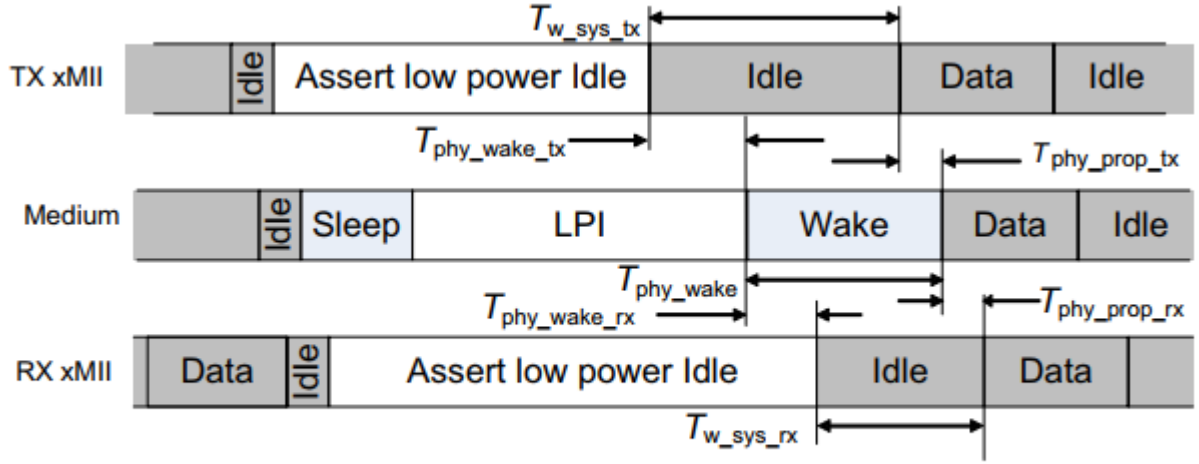
Delay Constraints

- The 100BASE-T1L supports and optional Reed-Solomon Forward Error Correction (RS-FEC) capability which offers enhanced noise protection at the expense of a significant increased latency.
- Therefore, two different sets of propagation delay constraints are proposed for 100BASE-T1L:
  - When the optional RS-FEC is not implemented or is disabled for the link (Low latency mode)
    - Transmit delay ≤ 360 ns (36 BT) and Receive delay ≤ 960 ns (96 BT)
    - Same as Clause 96 (100BASE-T1)
  - When the optional RS-FEC is implemented and enabled for the link (Burst error protection mode with high latency)
    - The sum of transmit and receive data delays ≤ 15,360 ns (3 pause_quanta)

LPI Timing parameters Review



$$T_{w\_sys\_tx}(\min) = T_{w\_sys\_rx}(\min) + T_{phy\_shrink\_tx}(\max) + T_{phy\_shrink\_rx}(\max) \quad (1)$$

$$T_{w\_phy}(\min) = T_{phy\_wake}(\min) + T_{phy\_shrink\_tx} \quad (2)$$

$T_{w\_sys\_res}$ (min) is greater of $T_{w\_sys\_tx}$ (min) and T_{w_phy} (min)

$$T_{phy\_shrink\_tx}(\max) = (T_{phy\_wake\_tx}(\max) - T_{phy\_prop\_tx}(\min)) \quad (3)$$

$$T_{phy\_shrink\_rx}(\max) = (T_{phy\_wake\_rx}(\max) - T_{phy\_prop\_rx}(\min)) \quad (4)$$

where

$T_{phy\_wake\_tx}$ = xMII start of wake to MDI start of wake delay
$T_{phy\_prop\_tx}$ = xMII to MDI data propagation delay
$T_{phy\_wake\_rx}$ = MDI start of wake to xMII start of wake delay
$T_{phy\_prop\_rx}$ = MDI to xMII data propagation delay
T_{phy_wake} = Minimum wake duration required by PHY

Figure 78–5—LPI mode timing parameters and their relationship to minimum system wake time

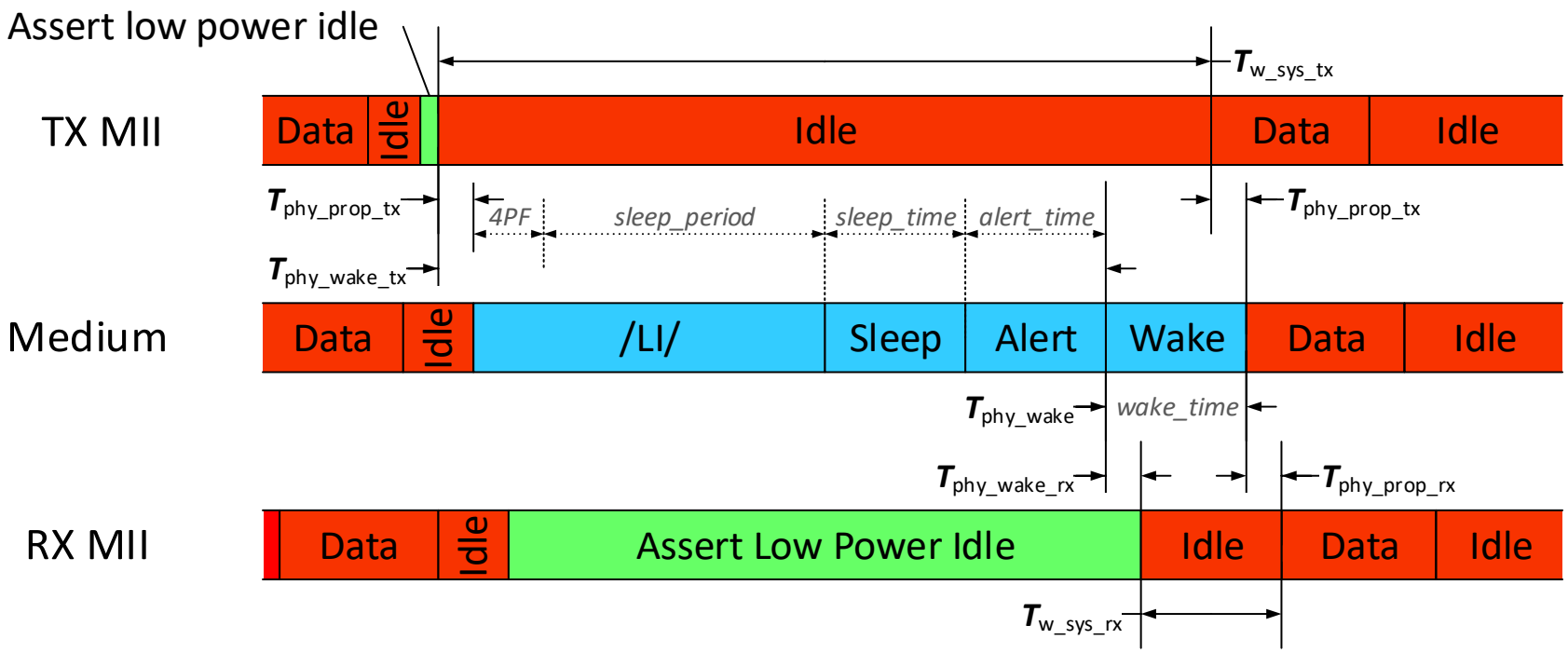
* Note: $T_{w\_sys\_res}$ is not defined in IEEE Std 802.3™-2022
See https://www.ieee802.org/3/az/public/jan09/law_1_0109_V3_0.pdf

LPI Timing Parameters References

- Definitions, calculations and parameters calculation based on:
  - https://www.ieee802.org/3/az/public/jan09/law_1_0109_V3_0.pdf
  - https://www.ieee802.org/3/az/public/adhoc/shrinkage/grimwood_01_0209.pdf
  - https://www.ieee802.org/3/az/public/mar09/law_1_0309.pdf

LPI timing parameters for 100BASE-T1L – Case 1

Case 1: Transmit wake signal before transmission of sleep is complete



Notes:

- When 8 + 2N consecutive MII Assert LPI transfers, where the last 2N transfers correspond to a (8N+1)B block, are indicated on the TX MII, the PHY TX will enter EEE and start transmitting (8N+1)B blocks constructed encoding N assert LPI (/LI/) control symbols (LIBLOCK_T), per the PCS transmit state diagram of Figure 190-12.
- After synchronizing to a 4 PF boundary, transmission of the sleep signal is restricted to start at predefined PFC values separated 16 PF periods (*sleep_period*), per the EEE transmit state diagram of Figure 190-13. The sleep signal is composed of 8 PF periods (*sleep_time*) within which, each (8N+1)B block is a LIBLOCK_T.
- The PHY TX will not enter EEE if less than 8 + 2N consecutive TX MII Assert LPI transfers are indicated on the TX MII, but once it is entered it will go through the full sleep-alert-wake cycle.

LPI timing parameters for 100BASE-T1L – Case 1

$T_{phy\_wake\_tx} = T_{phy\_prop\_tx} + 4\ PF + sleep\_period + sleep\_time + alert\_time$
$= T_{phy\_prop\_tx} + 4\ PF + 16\ PF + 8\ PF + 8\ PF$
$= T_{phy\_prop\_tx} + 86.4\ \mu s$

$T_{phy\_shrink\_tx} = T_{phy\_wake\_tx} - T_{phy\_prop\_tx}$ (3)
$= T_{phy\_prop\_tx} + 86.4\ \mu s - T_{phy\_prop\_tx}$
$= 86.4\ \mu s$

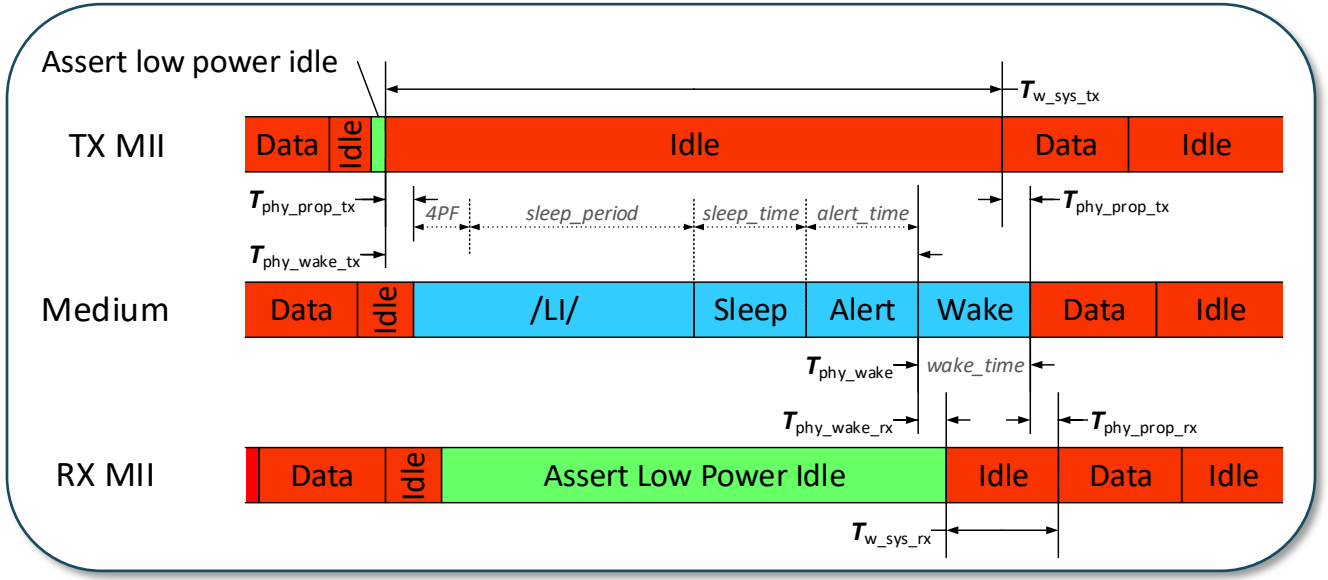
$T_{phy\_wake\_rx} = T_{phy\_prop\_rx}$

$T_{phy\_shrink\_rx} = T_{phy\_wake\_rx} - T_{phy\_prop\_rx}$ (4)
$= 0\ \mu s$

$T_{w\_phy} = T_{phy\_wake} + T_{phy\_shrink\_tx}$ (2)
$= 8\ PF + T_{phy\_shrink\_tx}$
$= 19.2\ \mu s + 86.4\ \mu s$
$= 105.6\ \mu s$

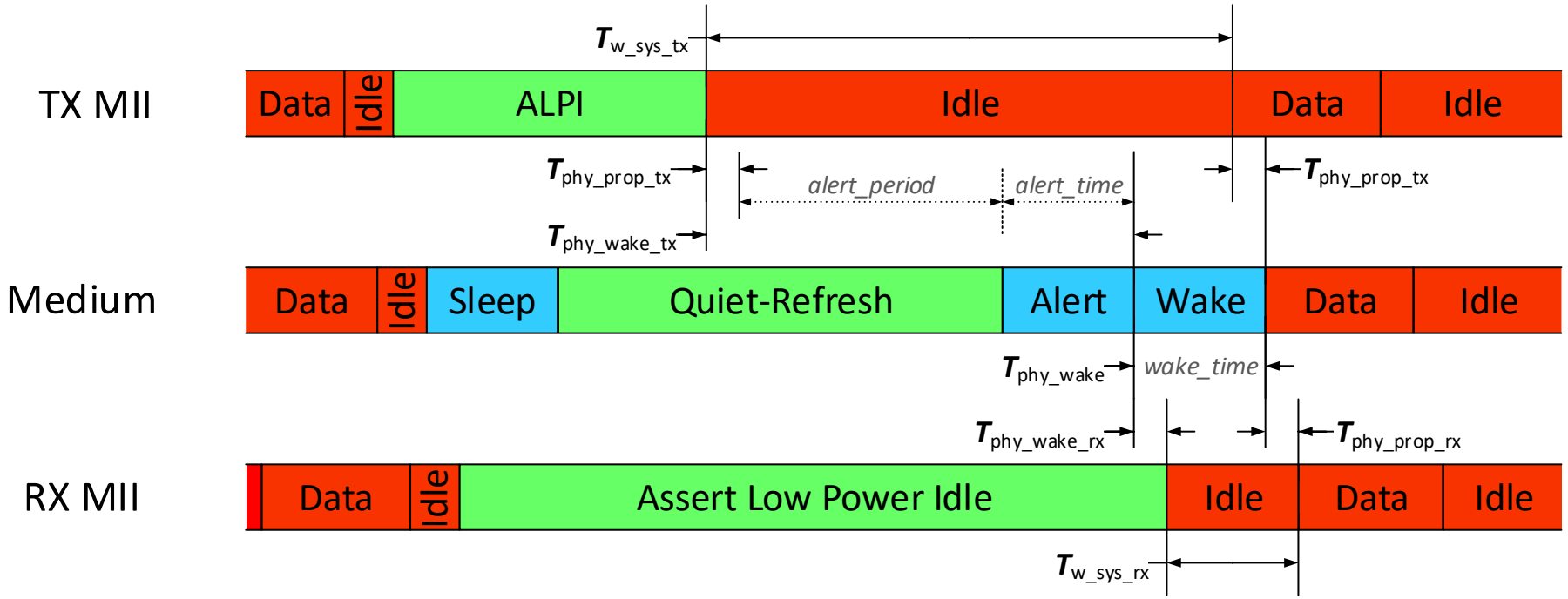
$T_{w\_sys\_rx} = T_{phy\_wake} - T_{phy\_shrink\_rx}$
$= wake\_time - 0\ \mu s$
$= 8\ PF$
$= 19.2\ us$

$T_{w\_sys\_tx} = T_{w\_sys\_rx} + T_{phy\_shrink\_tx} + T_{phy\_shrink\_rx}$ (1)
$= 19.2\ \mu s + 86.4\ \mu s + 0\ \mu s$
$= 105.6\ us$



LPI timing parameters for 100BASE-T1L – Case 2

Case 2: Transmit wake signal after transmission of sleep is complete



LPI timing parameters for 100BASE-T1L – Case 2

$T_{phy\_wake\_tx} = T_{phy\_prop\_tx} + alert\_period + alert\_time$
$= T_{phy\_prop\_tx} + 16\ \text{Partial Frames (PF)} + 8\ \text{PF}$
$= T_{phy\_prop\_tx} + 57.6\ \mu s$

$T_{phy\_shrink\_tx} = T_{phy\_wake\_tx} - T_{phy\_prop\_tx}$ (3)
$= T_{phy\_prop\_tx} + 57.6\ \mu s - T_{phy\_prop\_tx}$
$= 57.6\ \mu s$

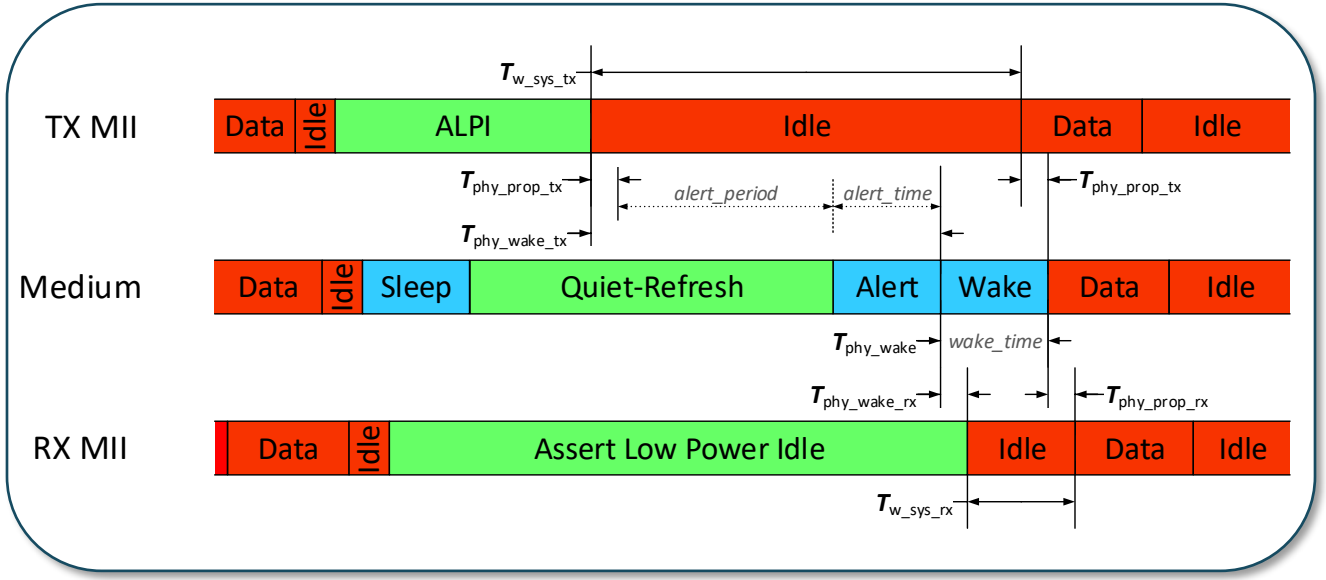
$T_{phy\_wake\_rx} = T_{phy\_prop\_rx}$

$T_{phy\_shrink\_rx} = T_{phy\_wake\_rx} - T_{phy\_prop\_rx}$ (4)
$= 0\ \mu s$

$T_{w\_phy} = T_{phy\_wake} + T_{phy\_shrink\_tx}$ (2)
$= 8\ \text{PF} + T_{phy\_shrink\_tx}$
$= 19.2\ \mu s + 57.6\ \mu s$
$= 76.8\ \mu s$

$T_{w\_sys\_rx} = T_{phy\_wake} - T_{phy\_shrink\_rx}$
$= wake\_time - 0\ \mu s$
$= 8\ \text{PF}$
$= 19.2\ us$

$T_{w\_sys\_tx} = T_{w\_sys\_rx} + T_{phy\_shrink\_tx} + T_{phy\_shrink\_rx}$ (1)
$= 19.2\ \mu s + 57.6\ \mu s + 0\ \mu s$
$= 76.8\ us$



LPI timing parameters for 100BASE-T1L - Proposed Values

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (µs)	T_{w_phy} (min) (µs)	$T_{phy\_shrink\_tx}$ (min) (µs)	$T_{phy\_shrink\_rx}$ (min) (µs)	$T_{w\_sys\_rx}$ (min) (µs)
100BASE-T1L	Case-1	105.6	105.6	86.4	0	19.2
	Case-2	76.8	76.8	57.6	0	19.2

Proposed Text for the Draft

Proposed Text for the Draft – Delay constraints

- Text for section 190.10 Delay constraints
  - This section is empty, insert the following text in section 190.10

IEEE P802.3dg™/D1.2, 7th July 2025

190.10 Delay constraints

New Text

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

For an implementation of a 100BASE-T1L PHY without the optional RS-FEC capability or when the optional RS-FEC is not enabled for the link, the delay of the transmit path shall not exceed 36 bit times (360 ns), and the delay of the receive path shall not exceed 96 bit times (960 ns). Transmit data delay is measured from the input of a given unit of data at the MII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the MII.

The sum of the transmit and receive data delays shall not exceed 1536 bit times (3 pause_quanta or 15360 ns) when the optional RS-FEC is enabled for the link.

A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 80.4 and its references.

NOTE 1—The physical medium interconnecting two PHYs introduces additional delay in a link. Equation (80–1) specifies the delay per meter of electrical cable in nanoseconds and may be used for 100BASE-T1L, given a bit time for 100 Mbit/s Ethernet of 10 ns.

NOTE 2—The transmit and receive delays are not testable in a system implementation, and only total delay from MII to MII is testable.

NOTE 3— The total delay can be tested using the PHY external loopback test mode specified in 190.5.2.1.

Proposed Text for the Draft – LPI timing parameters

- Update Table 78-4—Summary of the LPI timing parameters for supported PHYs or interfaces

New Table

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (µs)	T_{w_phy} (min) (µs)	$T_{phy\_shrink\_tx}$ (min) (µs)	$T_{phy\_shrink\_rx}$ (min) (µs)	$T_{w\_sys\_rx}$ (min) (µs)
…						
100BASE-T1L	Case-1	105.6	105.6	86.4	0	19.2
	Case-2	76.8	76.8	57.6	0	19.2
…						

IEEE P802.3dg™/D1.2, 7th July 2025

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (µs)	T_{w_phy} (min) (µs)	$T_{phy\_shrink\_tx}$ (max) (µs)	$T_{phy\_shrink\_rx}$ (max) (µs)	$T_{w\_sys\_rx}$ (min) (µs)
…						
100BASE-T1L	Case-1	TBD	TBD	TBD	TBD	TBD
	Case-2	TBD	TBD	TBD	TBD	TBD
…						

Backup Slides

LPI signaling timing for 100BASE-T1L

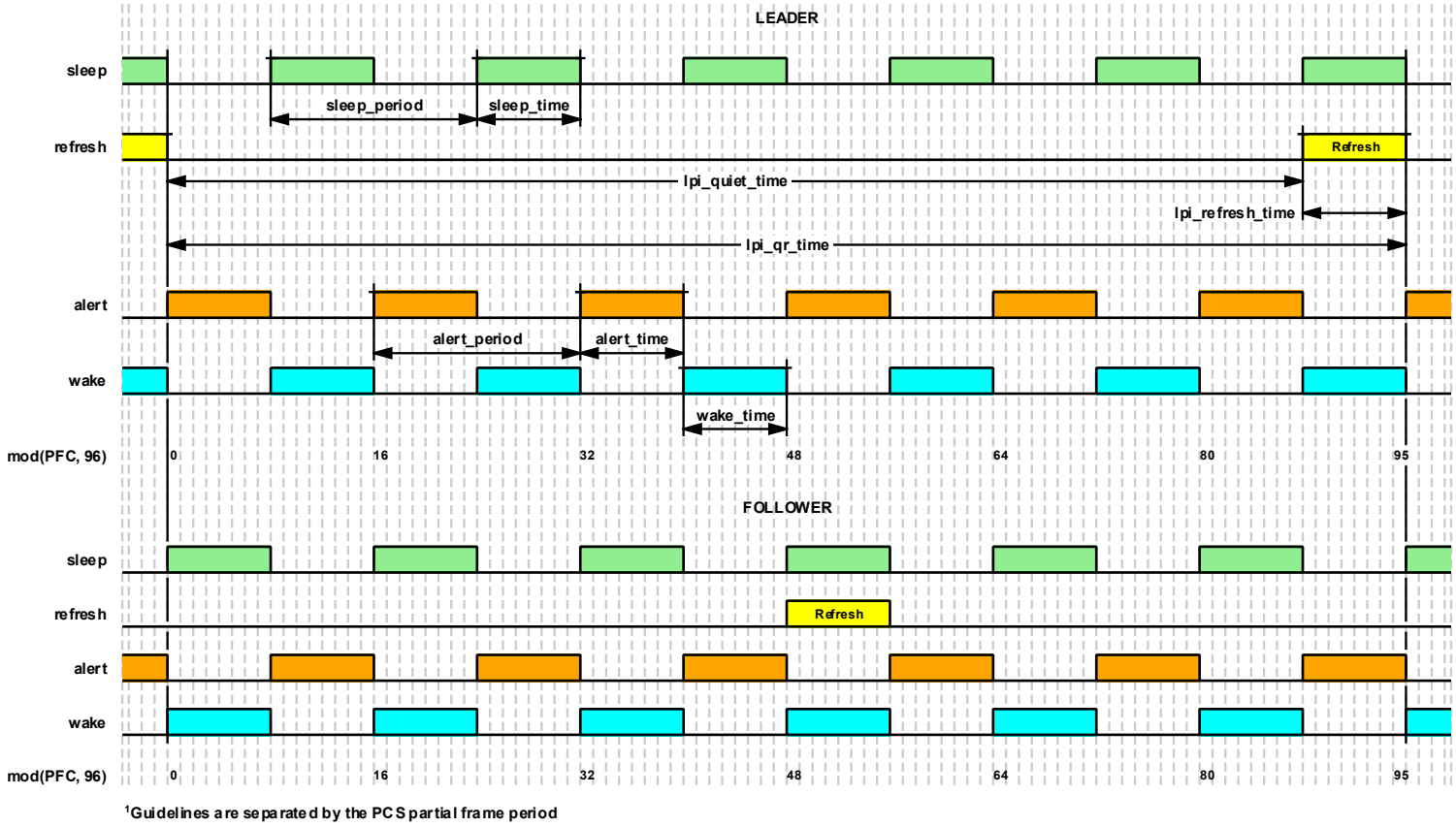


Figure 190-11–LPI signaling timing