



IEEE 802.3dg

Task Force

100BASE-T1L MDI

Specifications

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Current MDI Mode Conversion Loss Specification

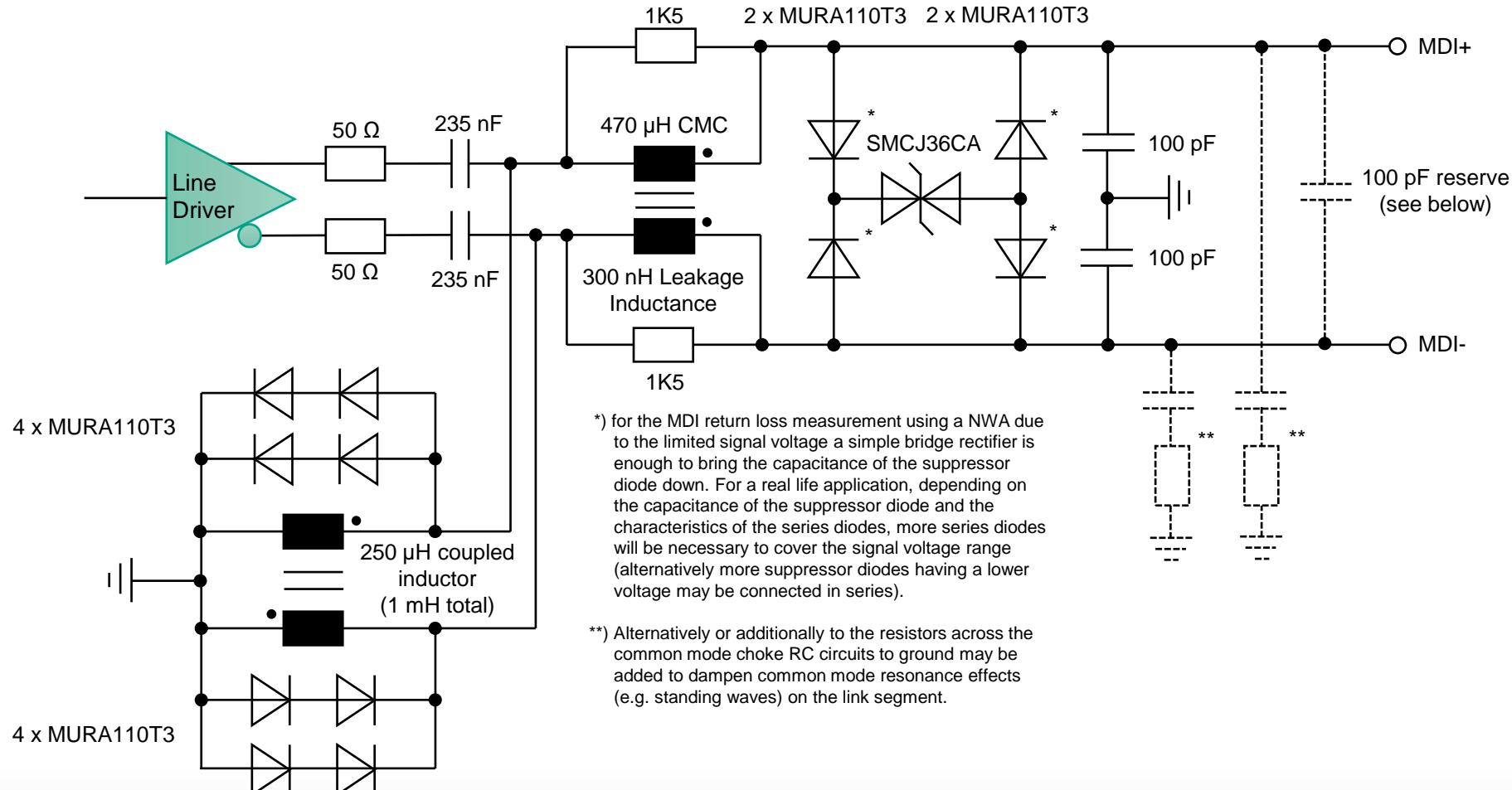
- Currently the MDI mode conversion loss defined in Clause 190.8.2.2 is:

$$MDI\ Conversion\ Loss \geq \begin{cases} 48\ dB & \text{for } 1\ MHz \leq f < 30\ MHz \\ 43.7\ dB - 19.2\ dB \cdot \log_{10} \left(\frac{f_{MHz}}{50\ MHz} \right) & \text{for } 30\ MHz \leq f \leq 100\ MHz \end{cases}$$

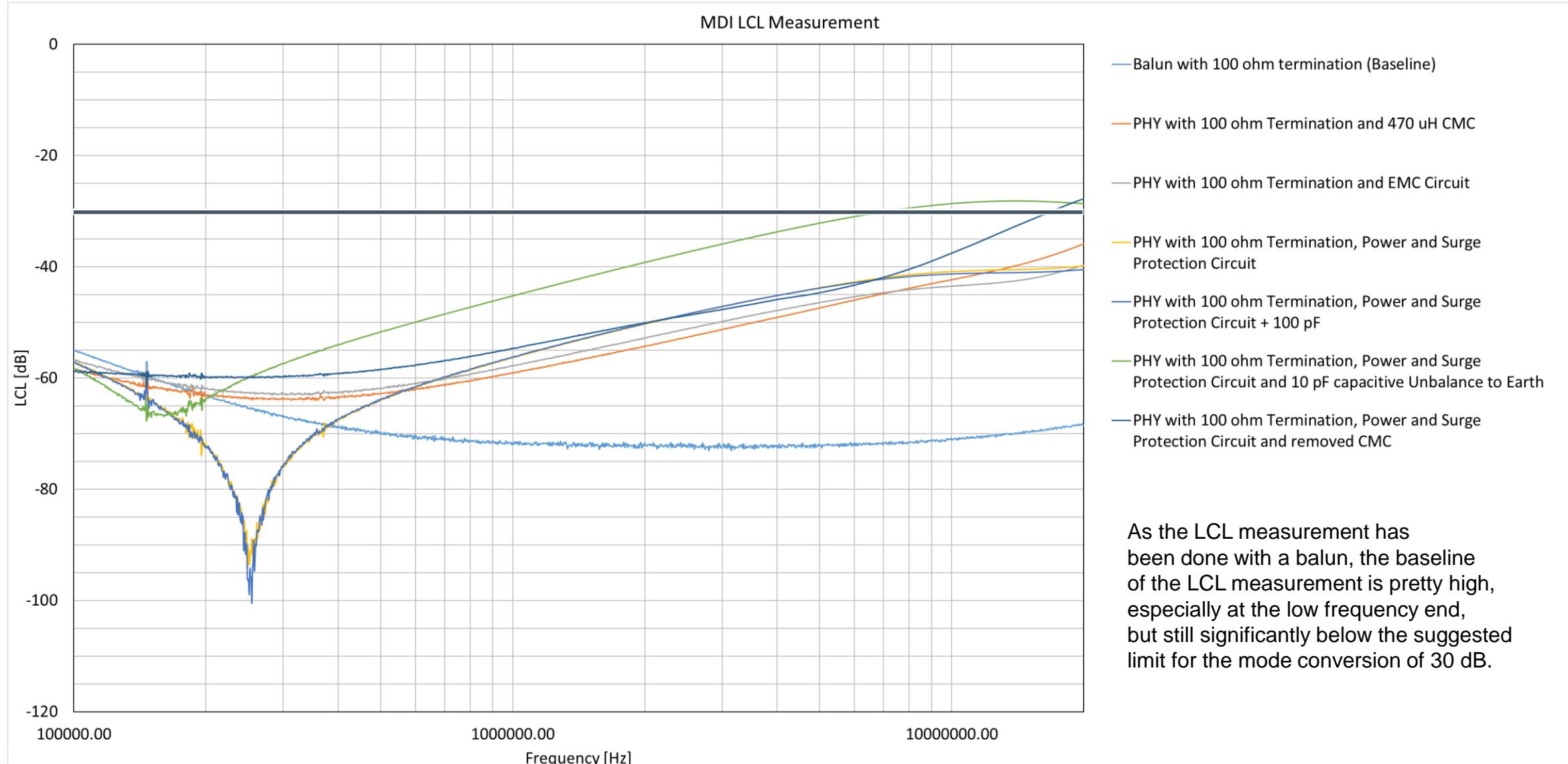
- The MDI Mode Conversion Loss has been defined based on the mode conversion loss of a 10/100 Mbit/s pulse transformer with integrated CMC, which is connecting the MDI (e.g., RJ45) over short distance PCB traces with the PHY IC, as appropriate isolation transformers are commonly available.
- In powered systems additionally to the isolation transformer further inductors and likely also an external common mode choke (CMC) and protection elements for the power coupling network are necessary.
- If in high power applications two separate power inductors have to be used, these inductors have relatively high tolerances (e.g. 5 % of the nominal inductance (assuming grinded ferrite cores)).
- Even when using a coupled inductor with two windings these larger inductors also face internal parasitic intra- and interwinding capacitances and asymmetries in the construction (e.g. having an upper and a lower separated winding on a two section bobbin to reduce the interwinding capacitances), which influence the MDI mode conversion loss.
- As the needed power feeding and EMC protection components are large in size, the unbalance on the PCB layout is also expected to be significantly higher than the unbalance of a standard 10/100/1000 Mbit/s Ethernet interface without powering circuit.

MDI Mode Conversion Loss Measurement for 10BASE-T1L

- For 100BASE-T1L currently no test circuit exists. For 10BASE-T1L the following power coupling/protection circuit has been suggested (see https://www.ieee802.org/3/cg/public/May2018/Graber_3cg_02a_0418.pdf):



MDI Mode Conversion Loss Measurement for 10BASE-T1



MDI Mode Conversion Loss for 100BASE-T1L

- As it can be seen on the previous slide, the expected mode conversion loss is higher than the currently specified limit.
- Extrapolating the measurements on the previous slide for 10BASE-T1L from 20 MHz to 30 MHz, the MDI mode conversion loss reaches about 33 - 35 dB (ignoring the artificially added unbalance of 10 pF and the implementation without CMC).
- Therefore, with some margin it is suggested to set the MDI mode conversion loss limit for frequencies below 30 MHz to 30 dB.
- The new suggested MDI mode conversion loss limit would be:

$$MDI\ Conversion\ Loss \geq \begin{cases} 30\ dB & for\ 1\ MHz \leq f < 30\ MHz \\ 30\ dB - 20\ dB \cdot \log_{10} \left(\frac{f_{MHz}}{30\ MHz} \right) & for\ 30\ MHz \leq f \leq 100\ MHz \end{cases}$$

- The suggested MDI mode conversion loss limit is, related to the baseline 5 dB higher than for 10BASE-T1L (30 dB up to 30 MHz for 100BASE-T1L vs. 25 dB up to 10 MHz for 10BASE-T1L), thus from an interoperability perspective it is expected to be reasonable.
- The change also needs a discussion about the impact on the EMC behavior of the overall system as the relaxed MDI mode conversion loss specification leads to a higher differential disturbing signal, e.g. during EFT testing, which in principle can result in packet losses that need to be covered by the upper layer protocols (e.g. by repeating a disturbed telegram).

MDI Return Loss for 10BASE-T1

- During working group ballot the MDI return loss specification has also been relaxed for powered systems, as mainly the expected parasitic capacitances in the system lead to a worse MDI RL in the upper frequency range:

$$MDI\ Return\ Loss \geq \begin{cases} 16\ dB - 20\ dB \cdot \log_{10} \left(\frac{2\ MHz}{f_{MHz}} \right) & \text{for } 1\ MHz \leq f < 2\ MHz \\ 16\ dB & \text{for } 2\ MHz \leq f \leq 20\ MHz \\ 16\ dB - 20\ dB \cdot \log_{10} \left(\frac{f_{MHz}}{20\ MHz} \right) & \text{for } 20\ MHz \leq f \leq 100\ MHz \end{cases}$$

- Reminder: The validation of the new limit and an analysis about a potential influence on the PHY design and reachable link segment length are still open and feedback is appreciated.

Thank you!