



**IEEE 802.3dg**

**Task Force**

**100BASE-T1L MDI RL**

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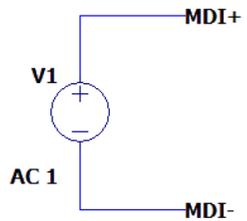
# Current MDI RL Specification

- Currently the MDI RL defined in Clause 190.8.2.1 is:

$$MDI \text{ Return Loss} \geq \begin{cases} 16 \text{ dB} - 20 \text{ dB} \cdot \log_{10} \left( \frac{2 \text{ MHz}}{f_{\text{MHz}}} \right) & \text{for } 1 \text{ MHz} \leq f < 2 \text{ MHz} \\ 16 \text{ dB} & \text{for } 2 \text{ MHz} \leq f \leq 40 \text{ MHz} \\ 10 \text{ dB} - 20 \text{ dB} \cdot \log_{10} \left( \frac{f_{\text{MHz}}}{80 \text{ MHz}} \right) & \text{for } 40 \text{ MHz} \leq f \leq 100 \text{ MHz} \end{cases}$$

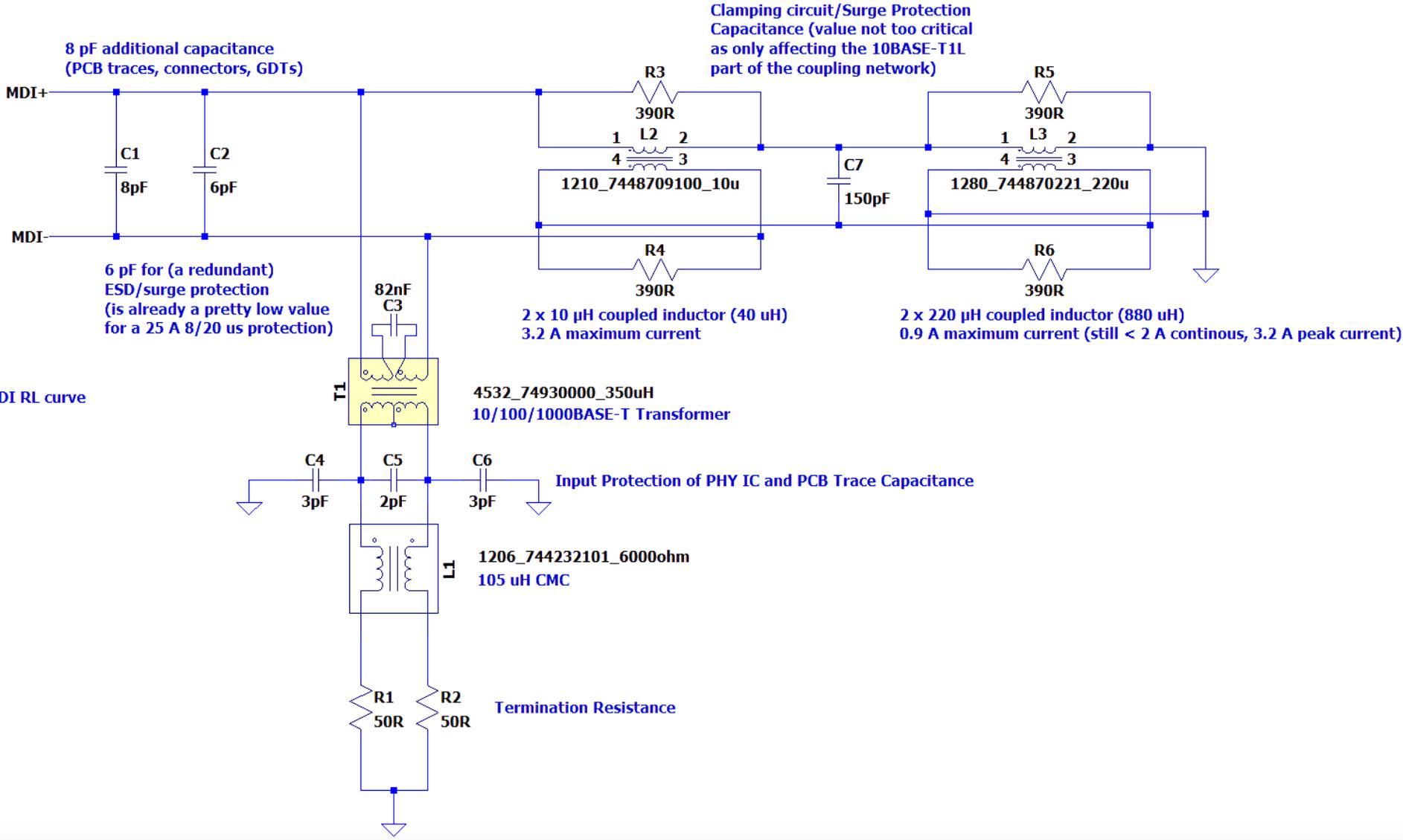
- The MDI RL has been defined based on the 1000BASE-T MDI RL specification, as appropriate isolation transformers are commonly available.
- In powered systems additionally to the isolation transformer further inductors and likely also a common mode choke for the power coupling network are necessary.
- These inductors have relatively high internal parasitic intra- and interwinding capacitances, which influence the MDI RL, especially in the higher frequency range.
- Due to the high current, e.g. flowing on an Ethernet-APL trunk, a significant amount of energy can be stored in the power coupling inductors, which needs to be dissipated in the clamping/EMC protection circuit in case of a freewheeling event.
- This causes the need for larger protection elements, providing a higher parasitic capacitance.

# MDI RL Simulation (Trunk Port, simplified Circuit)

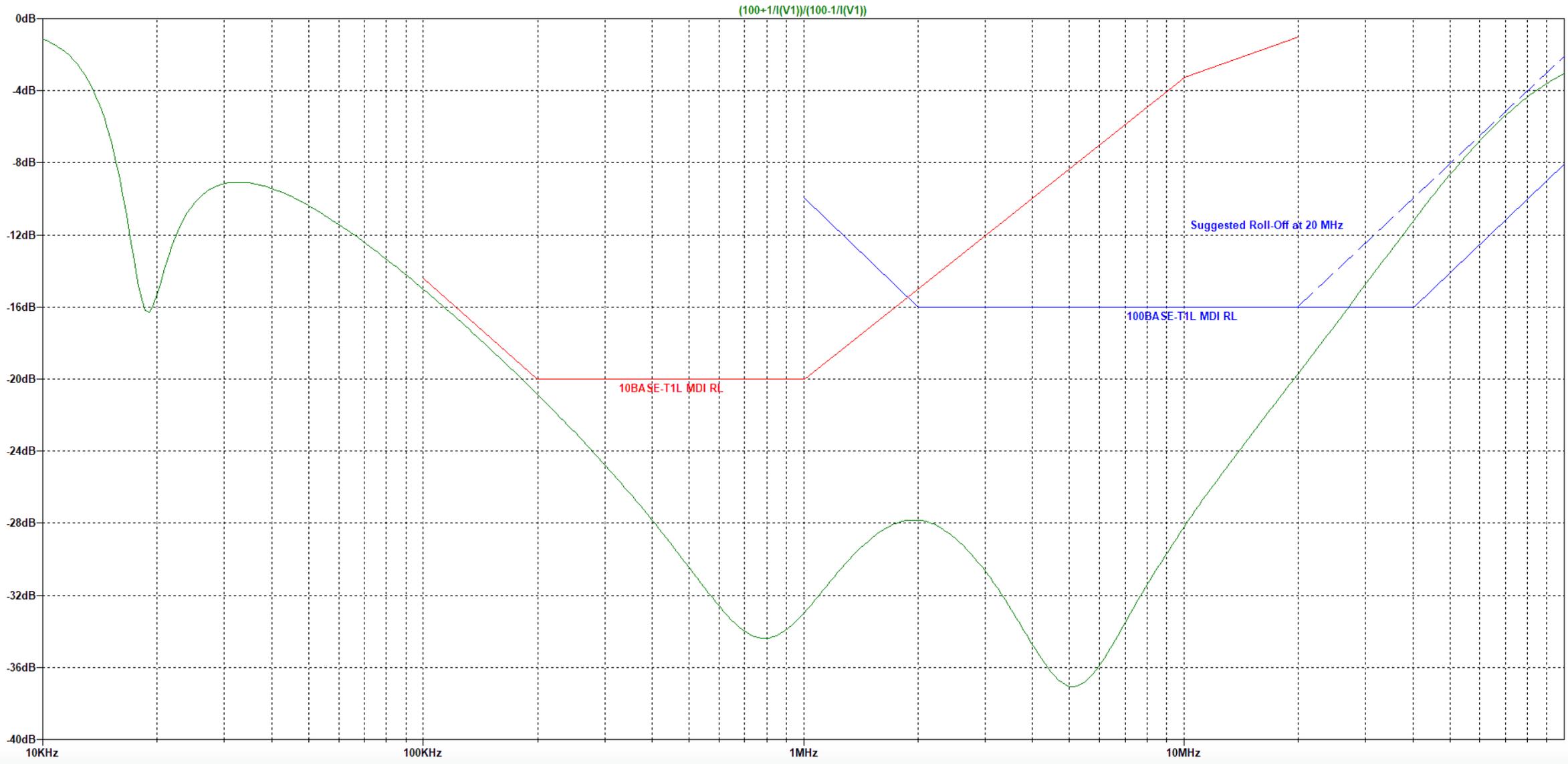


.ac dec 100 10k 100Meg

Plot  $(100+1/I(V1))/(100-1/I(V1))$  for MDI RL curve



# MDI RL Simulation Result



# MDI RL Specification

- As it can be seen on the previous slide, even when trying to minimize the capacitive load, for a practical implementation the 40 MHz corner frequency of the MDI RL specification is expected to be too high.
- Therefore, it is suggested to reduce the corner frequency from 40 MHz to 20 MHz.
- This leads to higher reflections at the MDI and thus a reduced signal energy at the receiver.
- Nevertheless, changing the corner frequency from 40 MHz to 20 MHz, still would lead to a similar MDI RL at Nyquist frequency as for 10BASE-T1L (10.4 dB @ 3.75 MHz for 10BASE-T1L and 10 dB @ 40 MHz for 100BASE-T1L).
- The new suggested MDI RL limit would be:

$$MDI \text{ Return Loss} \geq \begin{cases} 16 \text{ dB} - 20 \text{ dB} \cdot \log_{10} \left( \frac{2 \text{ MHz}}{f_{\text{MHz}}} \right) & \text{for } 1 \text{ MHz} \leq f < 2 \text{ MHz} \\ 16 \text{ dB} & \text{for } 2 \text{ MHz} \leq f \leq 20 \text{ MHz} \\ 16 \text{ dB} - 20 \text{ dB} \cdot \log_{10} \left( \frac{f_{\text{MHz}}}{20 \text{ MHz}} \right) & \text{for } 20 \text{ MHz} \leq f \leq 100 \text{ MHz} \end{cases}$$

- Needs discussion about the impact on a PHY IC implementation (e.g., input voltage range, EC length) and if a change of the link segment would be required (e.g., reduced IL limits for a powered system due to a reduced signal energy at the receiver).
- It would be good to also get further input from powering experts related to their view on (10)/100BASE-T1L powering circuits.

**Thank you!**