Editor’s Report: P802.3dg draft 1.0

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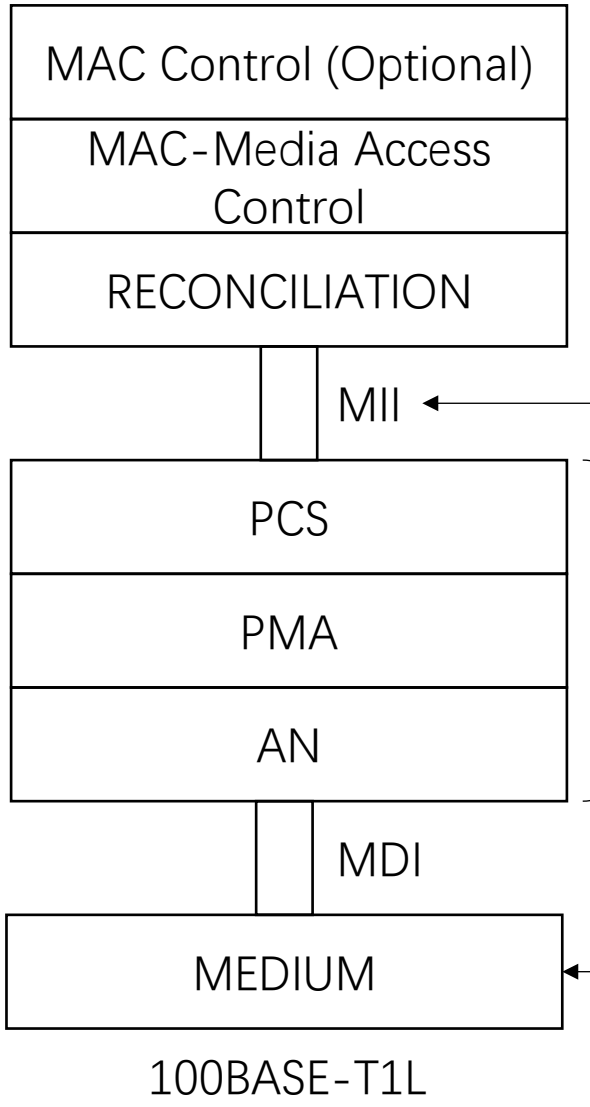
IEEE P802.3dg Task Force May 2025

Introduction

- Review of the adopted baselines
- Updates in D1.0 & ask for proposals
- Expectations for this meeting
- Next step

Adopted baselines



MII:

- New Sequence Ordered Set to be added on MII per slide 3 of Lo_3dg_01a_0724.pdf.
- Add aLF/aRF to Clause 22 MII in p10 of Murray_3dg_01_03122025.pdf

PCS&PMA:

- Rules of nibble combing at input/output of the 8N/(8N+1) according to p3, p9, p10-12, p15 of Lo_3dg_01a_0724.pdf
- PAM3 with 8B6T according to Murray_3dg_01a_07152024.
- Modification on 8N/(8N+1) according to p13,14 of Lo_3dg_01a_0724.pdf.
- PCS Tx Scrambler according to Murray_3dg_02_09172024.pdf.
- set the auxiliary bit in the PHY frame to zero.
- Control code and Mode encoding/decoding & pseudo code for 8N/(8N+1) in p3~p8&p10 of Murray_3dg_01a_11132024.pdf.
- EEE adopted in p4 to7 of Murray_3dg_03a_11132024.pdf.
- Auto-Negotiation adopted in p3 to p7 of Fitzgerald_3dg_01_11132024.pdf.
- Training and PHY Control State Diagram adopted in Curran_3dg_01a_01202025.pdf.
- Registers in Murray_3dg_03a_0312025.pdf.
- Block Structure Option B in p10 to p13 of Murray_3dg_02_03122025.pdf

Link Segment

- Link segment parameters (RL, IL, PSANEXT & PSAACR-F and TCL) as in link_segment_090723.pdf.

Updates in d1.0 (1)

Clause 45. Management Data Input/Output (MDIO) Interface		Notes
45.2.1 PMA/PMD registers		
45.2.1.7	PMA/PMD status 2 register (Register 1.8)	
45.2.1.7.4	Transmit fault (1.8.11)	
45.2.1.7.5	Receive fault (1.8.10)	
45.2.1.16	BASE-T1 PMA/PMD extended ability register (1.18)	
45.2.1.16.1aa	100BASE-T1L ability (1.18.8)	
45.2.1.214	BASE-T1 PMA/PMD control register (Register 1.2100)	
45.2.1.214.2	Type selection (1.2100.3:0)	
45.2.1.251	100BASE-T1L PMA control register (Register 1.2318)	Adopted baselines in Mar. and contents added
45.2.1.251.1	PMA reset (1.2318.15)	
45.2.1.251.2	Transmit disable (1.2318.14)	
45.2.1.251.3	Test mode transmit voltage amplitude control (1.2318.12)	
45.2.1.251.4	Low-power (1.2318.11)	
45.2.1.251.5	EEE enable (1.2318.10)	
45.2.1.251.6	Loopback (1.2318.0)	
45.2.1.252	100BASE-T1L PMA status register (Register 1.2319)	
45.2.1.252.1	Loopback ability (1.2319.13)	
45.2.1.252.2	2.4 Vpp operating mode ability (1.2319.12)	
45.2.1.252.3	Low-power ability (1.2319.11)	

Updates in d1.0 (2)

Clause 45. Management Data Input/Output (MDIO) Interface		**Notes**
45.2.1.252.4	EEE ability (1.2319.10)	Adopted baselines in Mar. and contents added
45.2.1.252.5	Receive fault ability (1.2319.9)	
45.2.1.252.6	Receive polarity (1.2319.2)	
45.2.1.252.7	Receive fault (1.2319.1)	
45.2.1.252.8	Receive link status (1.2319.0)	
45.2.1.253	100BASE-T1L test mode control register (Register 1.2320)	
45.2.1.253.1	Test mode control (1.2320.15:13)	
45.2.3 PCS registers		Updated
45.2.3.71a	100BASE-T1L PCS control register (Register 3.2280)	
45.2.3.71a.1	PCS reset (3.2280.15)	
45.2.3.71a.2	Loopback (3.2280.14)	
45.2.3.71b	100BASE-T1L PCS status register (Register 3.2281)	
45.2.3.71b.1	Tx LPI received (3.2281.14)	
45.2.3.71b.2	Rx LPI received (3.2281.13)	
45.2.3.71b.3	Tx LPI indication (3.2281.12)	
45.2.3.71b.4	Rx LPI indication (3.2281.11)	
45.2.3.71b.5	Fault (3.2281.10)	
45.2.3.71b.6	100BASE-T1L EEE capability (3.2281.8)	
45.2.3.71b.7	100BASE-T1L RS-FEC capability (3.2281.7)	
45.2.3.71b.8	PCS receive link status (3.2281.6)	

Updates in d1.0 (2)

Clause 45. Management Data Input/Output (MDIO) Interface		**Notes**
45.2.3.71c	100BASE-T1L advertisement register (Register 3.2282)	Updated with removal of SEQ adv.
45.2.3.71c.1	100BASE-T1L EEE advertisement (3.2282.1)	
45.2.3.71c.2	100BASE-T1L RS-FEC advertisement (3.2282.0)	
45.2.3.71d	100BASE-T1L link partner advertisement register (Register 3.2283)	
45.2.3.71d.1	100BASE-T1L link partner EEE advertisement (3.2283.1)	
45.2.3.71d.2	100BASE-T1L link partner RS-FEC advertisement (3.2283.0)	
Clause 190 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1L		• 190.3.3.4 Block structure updated according to adopted baseline texts in Mar. • Remove Editor's notes • converting tables and figures into frame.

Ask for Technical contents (1)

Registers - PMA/PMD types	
~~45.2.1~~	~~Table 45-3~~
~~45.2.1.7~~	~~Tables 45-9 & 45-10 Transmit & Receive fault locations~~
~~45.2.1.16~~	~~Table 45-19 (BASE-T1 PMA/PMD extended ability)~~
~~45.2.1.214~~	~~Table 45-178 (BASE-T1 PMA/PMD control register Type selection)~~
~~45.2.1.236a~~	~~Table 45-198a 100BASE-T1L PMA control register bit definitions~~
~~45.2.1.236b~~	~~Table 45-198b 100BASE-T1L PMA status register bit definitions~~
~~45.2.1.236c~~	~~Table 45-198c 100BASE-T1L test mode control register bit definitions~~
~~45.2.3~~	~~Table 45-233 PCS registers (consider relocating PCS registers at either 3.2280 or 3.2295)~~
~~45.2.3.88a~~	~~100BASE-T1L PCS status register (location fits within what is in dg draft 0p3)~~
~~45.2.7~~	~~Table 45-378 Auto-Negotiation MMD registers~~
~~45.2.7.27a~~	~~Table 45-402a 100BASE-T1L AN status register (7.528)~~
45.5.3.3	PMA register PICS – should wait until mostly complete
45.5.3.4	PCS register PICS – should wait until mostly complete

Ask for Technical contents (2)

Clause 78 EEE	
78.1.4	Table 78-1 clause
78.2	Table 78-2 summary of T_s, T_q, T_r
78.5	Table 78-4 Summary of Tw_sys_tx, phy, shrink, and sys timing parameters

Clause 98 Auto-Negotiation	
98.2.1	add 100BASE-T1L
98.5.1	add 100BASE-T1L to power on
98.5.2	add 100BASE-T1L to link_fail_inhibit_timer
98.6.2a	add 100BASE-T1L to option type (or add it to 10BASE-T1L option type existing.
98.6.8	change condition on SD11, SD12 to include 100BASE-T1L
98B.3	Technology Ability Field bit assignments

Clause 104 Power	
104.1.3	add 100BASE-T1L to PoDL system types

Ask for Technical contents (3)

Clause 190 100BASE-T1L	
190.1.3	Proposal for Figure 190–2—Functional block diagram is needed
199.5	PMA electrical specifications
199.5.1	EMC Tests
199.5.2	Test modes
199.5.3	Test fixture
199.5.4	Transmitter electrical specification
199.5.5	Receiver electrical specifications
199.5.6	PMA local loopback
199.6.2	LEADER-FOLLOWER configuration
199.8	MDI specification
199.9	Environmental specifications
199.1	Delay constraints

Expectations for this meeting

- Discuss ordering of register bits in CL45 – Valerie will lead the discussion
- Discuss on comments and proposed responses received against D1.0.

Summary

- Draft (D1.0) is provide in private area and start task force review.
- We highly encourage colleagues to check clauses asks for technical contents and bring your contributions along with similar sections in 802.3 (preferably with baseline texts) to facilitate the baseline work.
- Again, if you see anything missing in the draft (which the group has already made decisions), please contact editors to incorporate it.
- Next Step:
  - Adopted comment resolution in this meeting to generate the next version.

Thank you!