PCS & PMA proposal

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PCS and PMA proposal

- **Proposal is to adopt the P802.3cz BASE-U PCS and PMA for P802.3dh**

- BASE-U PCS & PMA meets the P802.3dh project's **objectives**
- BASE-U PCS & PMA is **technically complete and mature** (P802.3cz is currently in SA ballot)
- BASE-U PCS & PMA meet **automotive requirements**:
  - support all the targeted **data-rates**
  - support **OAM** channel
  - support **EEE**
- BASE-U PCS & PMA is designed to **approach** channel **capacity** limit. Specially relevant for GI-POF (P802.3dh) that has lower bandwidth and higher attenuation than OM3 (P802.3cz)

PCS and PMA proposal

- BASE-U PCS & PMA support fully **adaptive receiver** implementations. This allows:
  - Compensate impairments due to large parametric deviation ➔ high production **yield**
  - Maximize RX **sensitivity** ➔ support of much higher insertion losses for optical connections targeted to harsh environments
  - Enable the use of automotive qualified and high volume low-cost **bulk CMOS** sub-micron tech nodes
- Adoption of BASE-U PCS & PMA in P802.3dh will minimize automotive **market fragmentation**, e.g. same PHYs can be used for OM3 and GI-POF
- **Following slides explain the rational behind this proposal**

Why 802.3cz did not reuse BASE-SR?

BASE-AU vs BASE-SR

Characteristics	BASE-AU	BASE-SR
Data-rates	2.5, 5, 10, 25, 50	10, 25, 50
Application T_{BS} range (C)	−40 to +125	0 to +85
OAM channel support	**YES** OAM channel is an Automotive requirement 802.3bp, 802.3bv, 802.3ch, P802.3cy specifies OAM. OAM is also operative during LPI.	**NO**
Dependability functions support (link margin, OAM)	**YES**	**NO**
Link establishment is bidirectional	**YES**	**NO**
EEE support	PHY TX remains transmitting signals during LPI, however data generated by PCS is modified wrt normal operation to allow big power saving , while OAM channel is operative and wake signal detection is robust. LPI is defined for 2.5, 5, 10, 25, and 50 Gb/s.	Fast wake mode, where PCS encodes LPI as in normal operation. Power saving is very limited in the receiver. LPI is only defined for 25 and 50 Gb/s.
Data-aided timing-recovery supported	**YES** Required the highly sensitive RX for high insertion loss channels	**NO**
Data-aided equalization supported	**YES** Required the highly sensitive RX for high insertion loss channels	**NO**
Design startegy	**Maximize supported channel insertion loss**	**Maximize link distance**
Modal dispersion	Small impact	Defines the max distance by ISI limitation. Specially relevant in 10 Gb/s
Chromatic dispersion	Negligible impact	Defines the MPN with RMS width. Specially relevant in 10 Gb/s
Mode Partition Noise	Negligible impact	Limit the channel capacity. Specially relevant in 10 Gb/s
Main noise limitation	Receiver (PD, TIA, Sampling)	Transmitter (RIN, MPN)
Link budget	**Limited by TX distortion and RX noise**	**Limited by TX and channel distortions, MPN and RIN**
Transmitter is validated with equalized reference RX	**YES**, for all the rates (Decision Feedback Equalizer)	**NO** for 10 and 25 Gb/s. **YES** for 50 Gb/s (linear Feed-Forward Equalizer)

BASE-U PCS & PMA distinctive features

PHD data: PHY control, OAM, dependability

Table 166–2—PHD structure

Field name	Description	Number of bits	Valid values
PHD.TX.NEXT.MODE	Transmission mode of the next Transmit Block, indicated to link partner to align its reception (see 166.5.1)	3	0: normal transmission 1: BER test mode transmission 2 through 7: reserved
PHD.RX.LINKSTATUS	Indicates whether the local PHY is able to receive 65-bit blocks with reliability. The value of this field is determined by the PHY quality monitor state diagram (see 166.3.4.6.4). The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_status (see 166.3.4.1)	1	0: NOT_OK 1: OK
PHD.RX.HDRSTATUS	Indicates whether the local PHY is able to receive the PHD from its link partner with reliability. The value of this field is determined by the local PHD reception monitor state diagram (see 166.3.4.5). The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_hdr_lock (see 166.3.4.1)	1	0: NOT_OK 1: OK
PHD.RX.LINKMARGIN	The value of this field is determined by the PHY quality monitor state diagram (see 166.3.4.6.4) in response to link margin estimation as defined in 166.3.4.6.2. Upon reception of a valid PHD, the field is stored in bits 3.2351.7:0 (see 45.2.3.93)	8	This field is fixed-point formatted (8, 3) and is provided in $\log_2$ units (see 166.3.4.6.2). See 166.1.1 for fixed-point format.
PHD.CAP.LPI	This field indicates whether the PHY supports EEE and has enabled the announcement of this ability (see 166.4)	1	0: EEE is not supported or it is not announced 1: EEE is supported and it is announced
PHD.CAP.OAM	This field indicates whether the PHY supports BASE-U OAM and has enabled the announcement of this ability (see 166.11)	1	0: BASE-U OAM is not supported or it is not announced 1: BASE-U OAM is supported and it is announced
	Reserved	65	0
PHD.OAM.DATA0	BASE-U OAM message data field 0 (see 166.11)	12	0x000 through 0xFFF
PHD.OAM.MSGT	BASE-U OAM message identification bit (see 166.11)	1	0 or 1
PHD.OAM.MERT	BASE-U OAM STA read identification bit (see 166.11)	1	0 or 1
PHD.OAM.PHYT	BASE-U OAM PHY reception identification bit (see 166.11)	1	0 or 1
	Reserved	1	0
PHD.OAM.DATA1	BASE-U OAM message data field 1 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA2	BASE-U OAM message data field 2 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA3	BASE-U OAM message data field 3 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA4	BASE-U OAM message data field 4 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA5	BASE-U OAM message data field 5 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA6	BASE-U OAM message data field 6 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA7	BASE-U OAM message data field 7 (see 166.11)	16	0x0000 through 0xFFFF
PHD.OAM.DATA8	BASE-U OAM message data field 8 (see 166.11)	16	0x0000 through 0xFFFF

- PHD transports information used for several purposes:
  - Announce transmission mode (normal or BER test)
  - PHY control, link monitoring, bidirectional link establishment
  - Link-margin so that remote and local link margin can monitored for dependability
  - Negotiation of optional features
  - OAM channel: it provides low rate reliable exchange of messages between STA peers attached to link partners using MDIO registers. Used to implement specific automotive features:
    - Wake-up propagation over active links (e.g. ISO 21111-2)
    - Synchronized sleep-down transition between link partners (e.g. ISO 21111-2)
    - Transportation of remote dependability information: e.g. temperature, voltage monitors, physical layer monitors, etc. (e.g. Open Alliance TC15, advance diagnostics)
- PHD uses pre-allocated time slots for transmission, independent of xGMII transmission

PHD: encoding and transmission

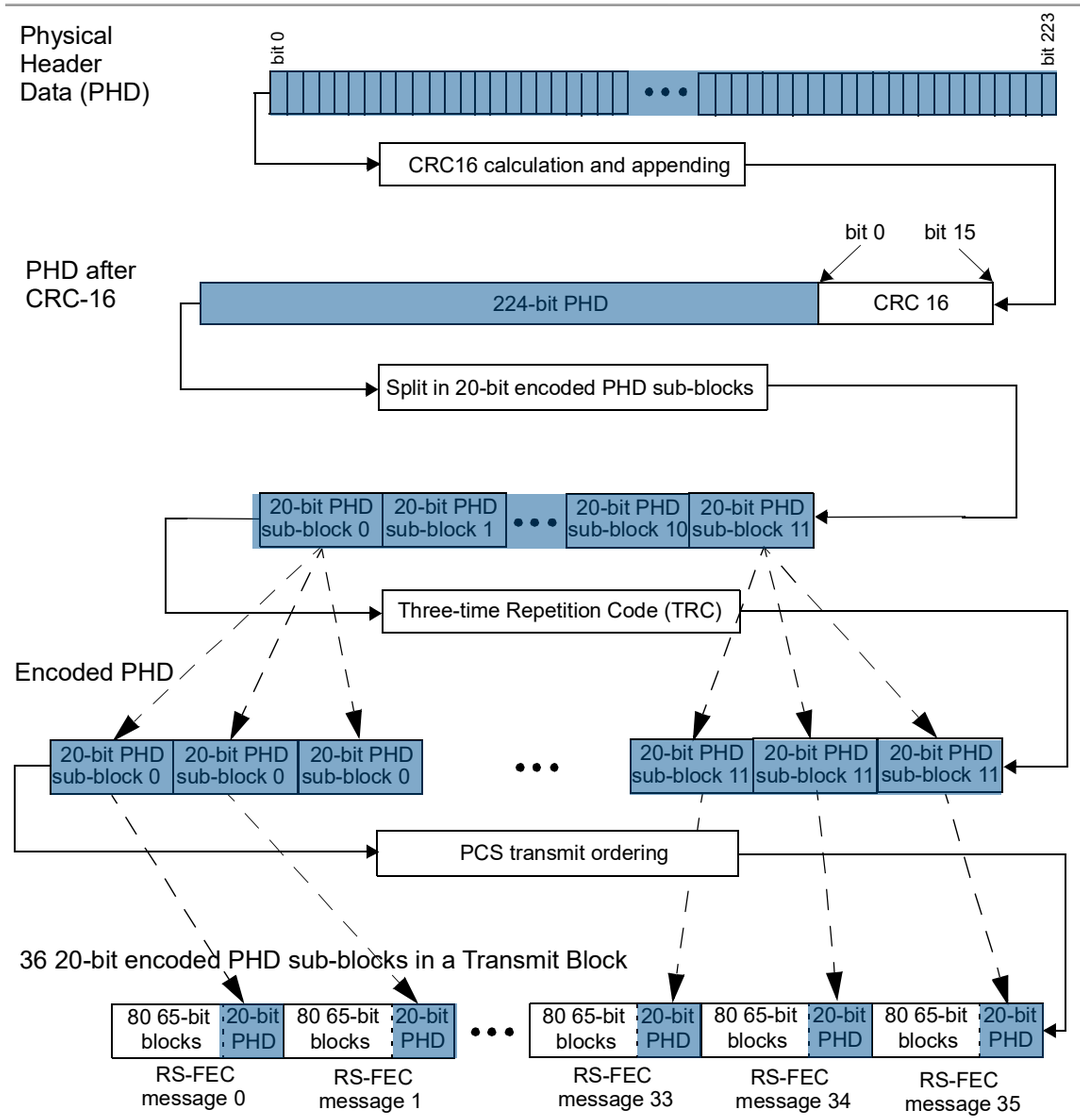


Figure 166–10—Physical Header Data transmit bit order

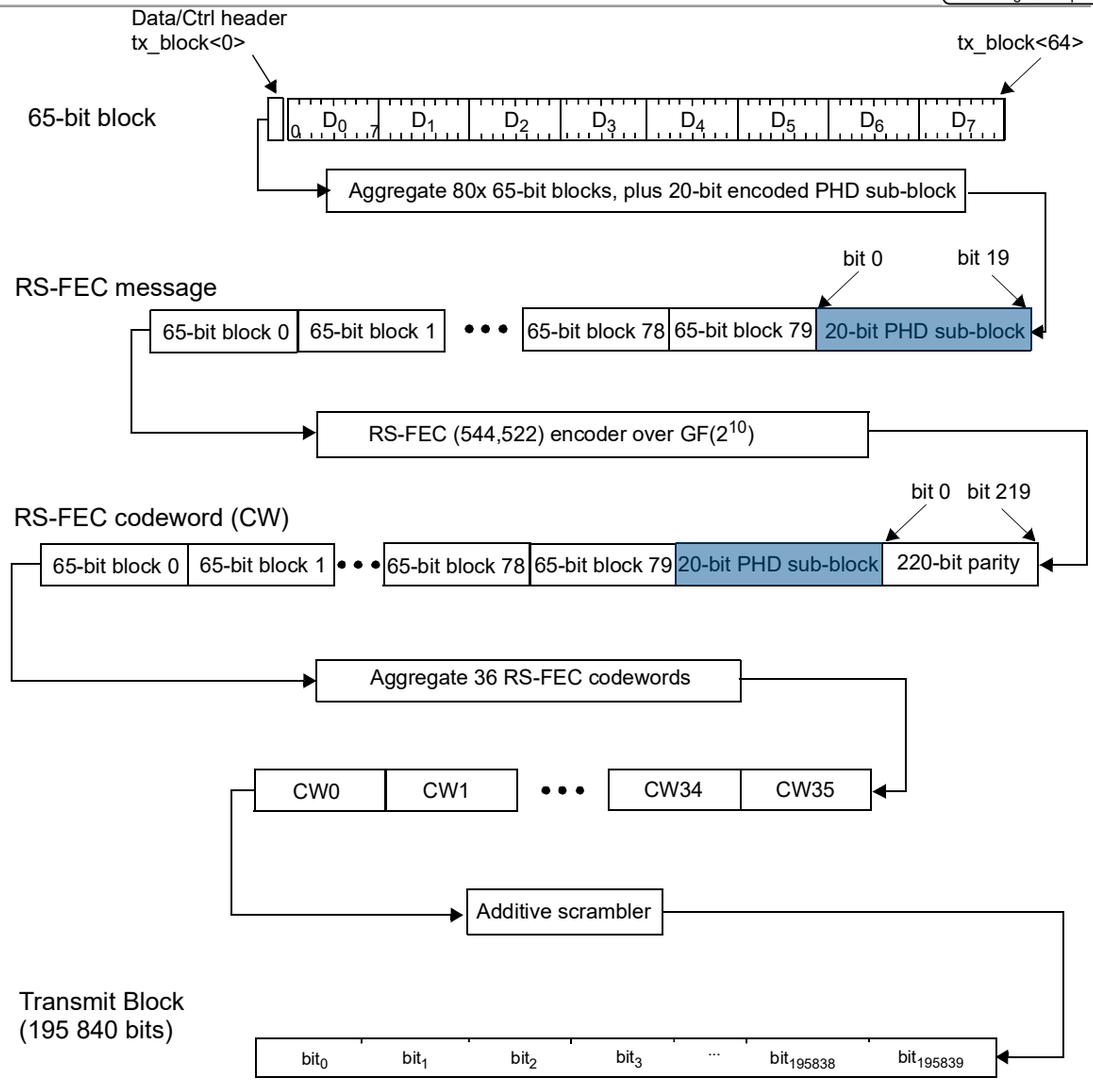


Figure 166–11—PCS transmit bit order

- A 3-repetition code is used as inner code, interleaved and concatenated with the RS code for error correction
- The reliability of PHD is dramatically boosted wrt xGMII data (BER from 10^{-6} to 10^{-12}, from 10^{-12} to 10^{-24}) and is insensitive to error bursts caused by DFE

- In general, simulations show that a RS code over GF(2^{10}) is almost not affected by DFE bursts for the number of feedback taps specified in the TDFOM reference RX
- CRC16 is used for error detection

PCS encoding, space allocation for PHD and FEC

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	10	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	10	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	10	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	10	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	10	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	10	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	10	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	10	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 49–7—64B/66B block formats

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\,C_1\,C_2\,C_3/O_4\,D_5\,D_6\,D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\,C_1\,C_2\,C_3/S_4\,D_5\,D_6\,D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/S_4\,D_5\,D_6\,D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/O_4\,D_5\,D_6\,D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/C_4\,C_5\,C_6\,C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 166–14—65-bit block format for BASE-U PCS connected to XGMII or 25GMII

- 2-bit sync is converted into 1-bit data control header (trivial transcoding)
- “sync” field made sense in BASE-R PCS with serial PMA w/o FEC and EQ where simple detection was implemented, e.g. sync is not scrambled, so 1 signal transition is guaranteed per each 66-bit block
- Synchronization function is implemented in different way in 802.3cz
- Saved space is allocated for PHD and RS-FEC parity: 80 bits are saved per CW, 20 for PHD, 60 for parity (~30% of parity)

PCS encoding, space allocation for PHD and FEC

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7$	10	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$S_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$	10	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0 D_1 D_2 D_3 Z_4 Z_5 Z_6 Z_7$	10	0x4B	D_1	D_2	D_3	O_0	0x000_0000		
$T_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0 T_1 C_2 C_3 C_4 C_5 C_6 C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0 D_1 T_2 C_3 C_4 C_5 C_6 C_7$	10	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0 D_1 D_2 T_3 C_4 C_5 C_6 C_7$	10	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0 D_1 D_2 D_3 T_4 C_5 C_6 C_7$	10	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0 D_1 D_2 D_3 D_4 T_5 C_6 C_7$	10	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0 D_1 D_2 D_3 D_4 D_5 T_6 C_7$	10	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0 D_1 D_2 D_3 D_4 D_5 D_6 T_7$	10	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 82–5—64B/66B block formats

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$S_0 D_1 D_2 D_3 D_4 D_5 D_6 D_7$	1	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0 D_1 D_2 D_3 Z_4 Z_5 Z_6 Z_7$	1	0x4B	D_1	D_2	D_3	O_0	0x000_0000		
$T_0 C_1 C_2 C_3 C_4 C_5 C_6 C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0 T_1 C_2 C_3 C_4 C_5 C_6 C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0 D_1 T_2 C_3 C_4 C_5 C_6 C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0 D_1 D_2 T_3 C_4 C_5 C_6 C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0 D_1 D_2 D_3 T_4 C_5 C_6 C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0 D_1 D_2 D_3 D_4 T_5 C_6 C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0 D_1 D_2 D_3 D_4 D_5 T_6 C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0 D_1 D_2 D_3 D_4 D_5 D_6 T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 166–15—65-bit block format for BASE-U PCS connected to 50GMII

- Same arguments behind the 50GMII PCS encoding

PHD link establishment

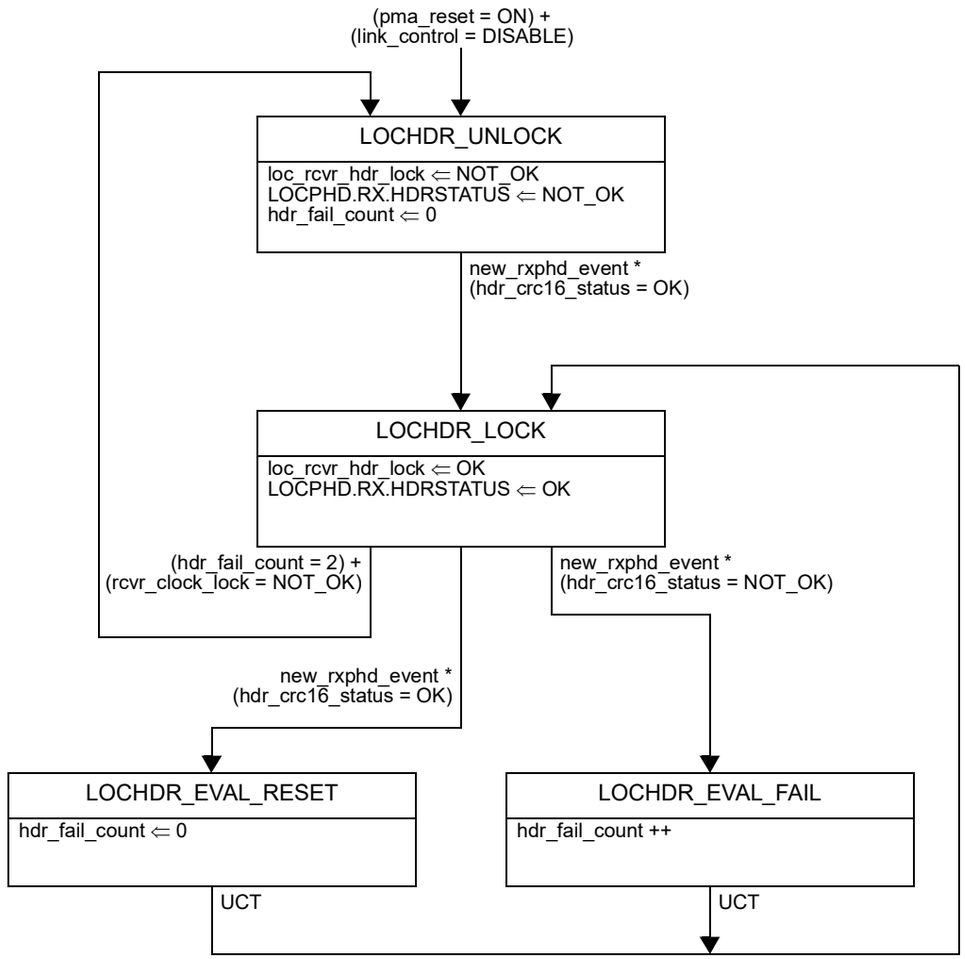


Figure 166–26—Local PHD reception monitor state diagram

- PHD bidirectional link is established before the link for xGMII data transportation, so that the PHY control and link monitor functions are reliable
- Due to the much higher reliability of the PHD link, the PHYs can exchange PHY control information, link margin and OAM messages for dependability/monitoring even if quality of link has been degraded and xGMII data cannot be exchanged with reliability

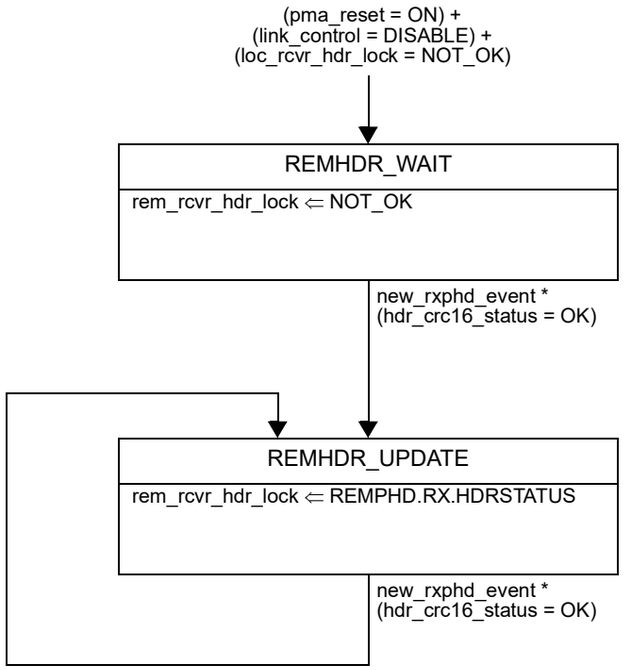


Figure 166–27—Remote PHD reception monitor state diagram

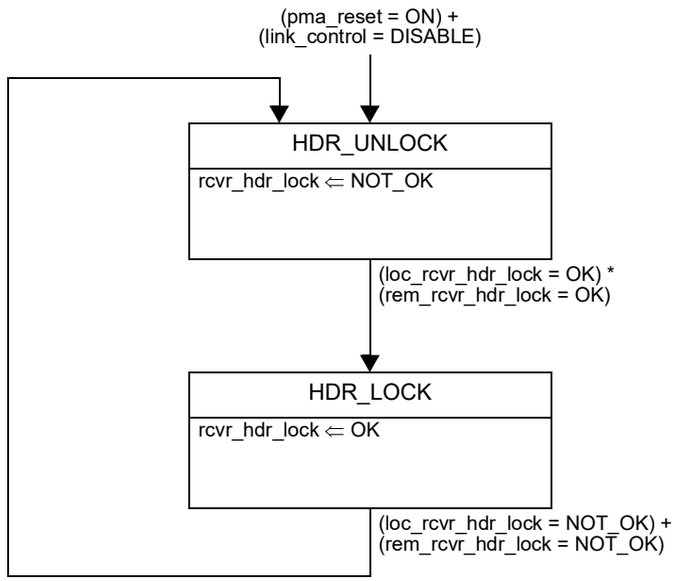


Figure 166–28—PHD monitor state diagram

Bidirectional PHY control and link establishment

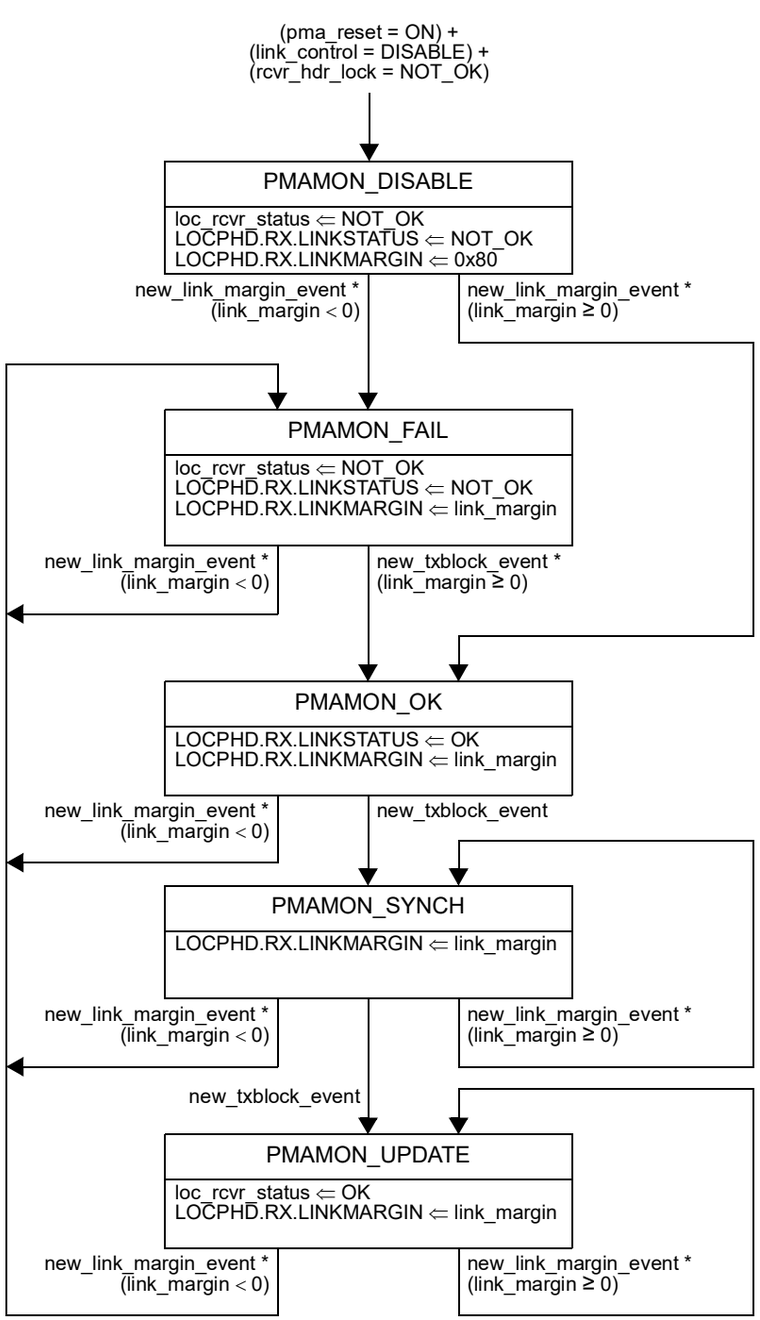


Figure 166–29—PHY quality monitor state diagram

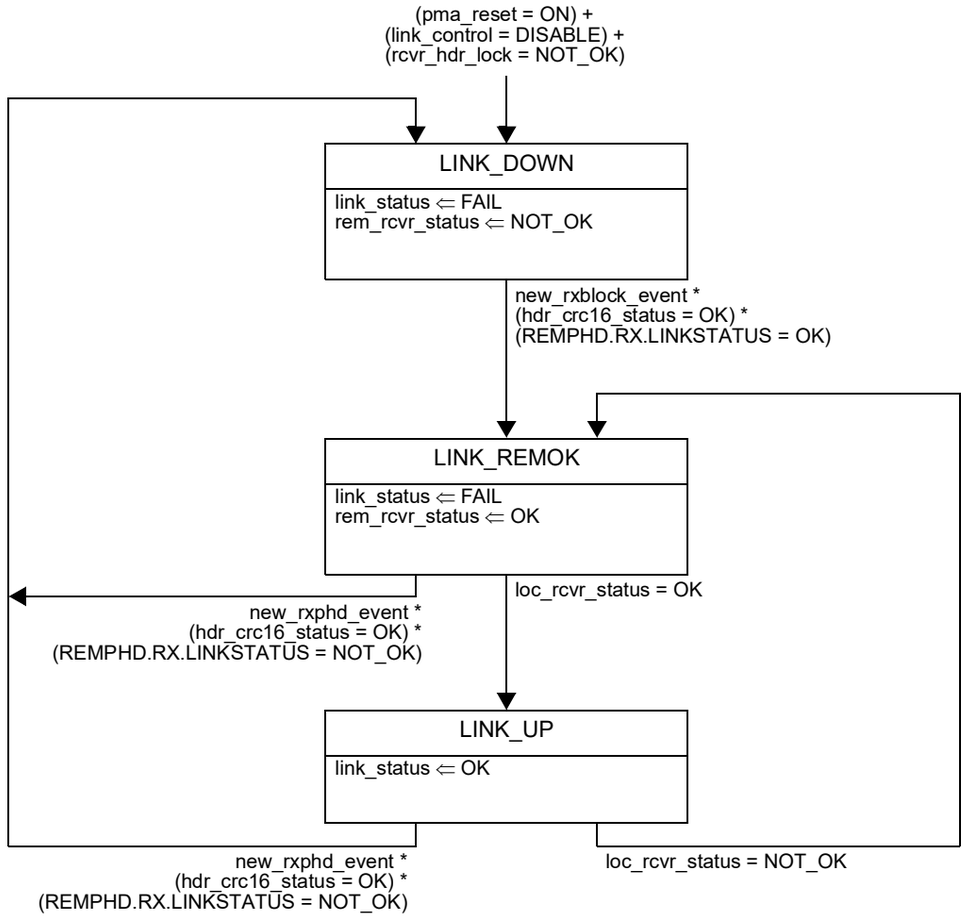
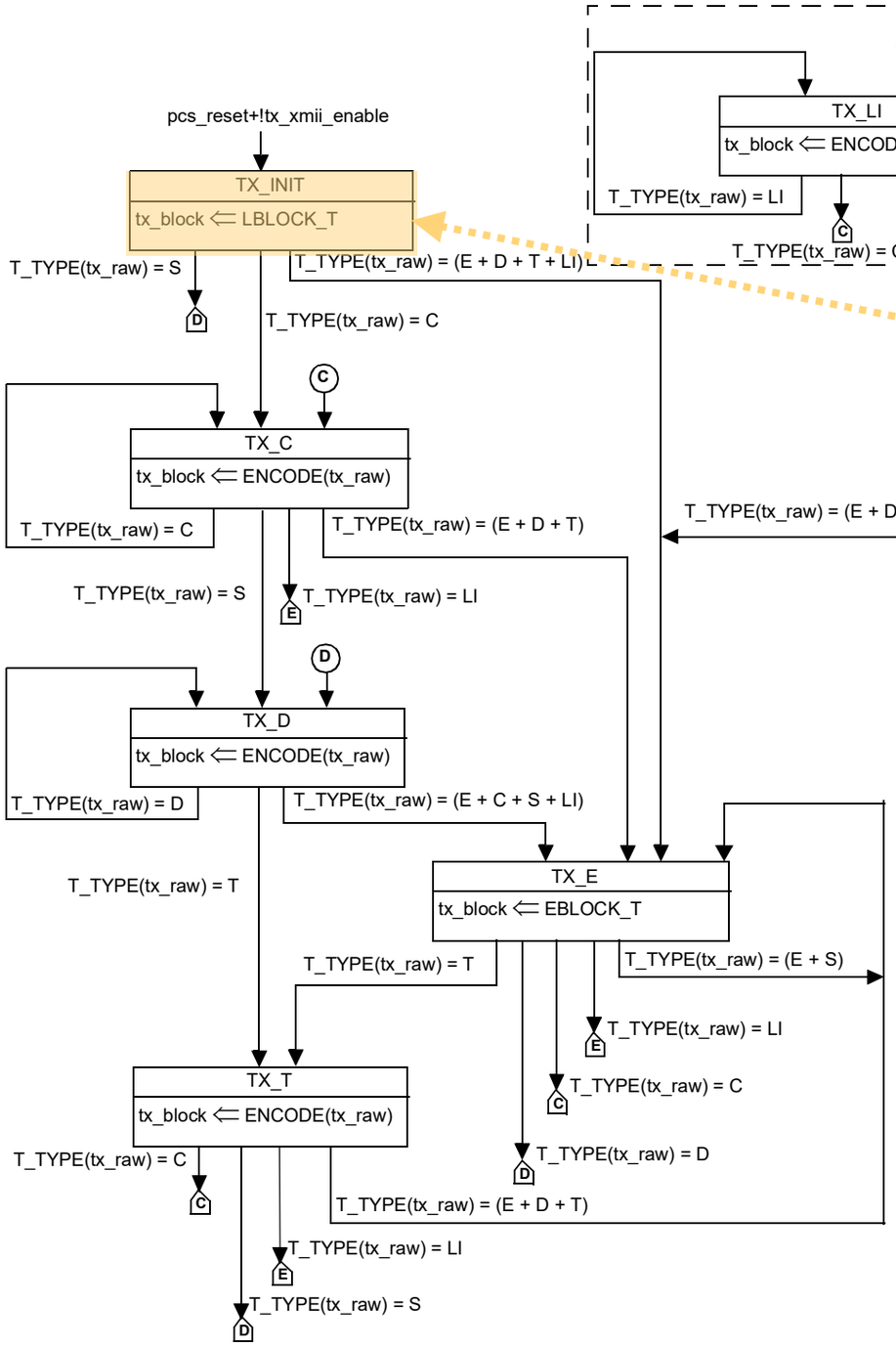


Figure 166–25—Link monitor state diagram

- Link is indicated OK only when both link partners have validated reliable reception
- Link is established synchronously in both link partners, so every packet transmitted in one side will reach the remote side once link status was indicated OK
- State diagrams communicates using PHD

Data-aided TR and EQ support



NOTE—Optional state (inside the dotted box) and transition E are mandatory for PHYs with the EEE capability.

Figure 166–16—PCS 64B/65B transmit state diagram

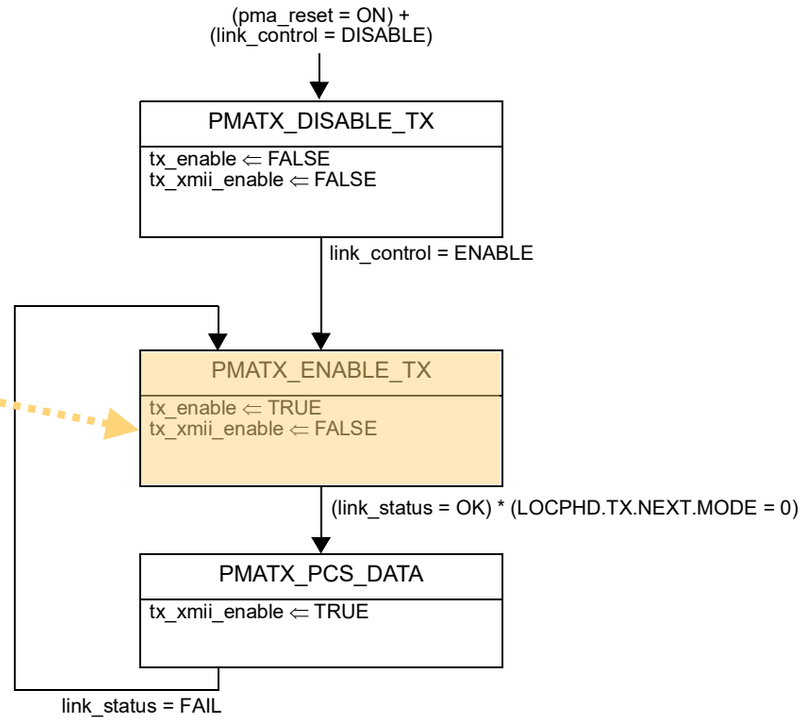


Figure 166–23—PHY Tx control state diagram

- In TX_INIT, the PCS 64B/65B transmit state diagram sends to the RS-FEC encoder a 65-bit vector containing two local fault ordered sets (XGMII/25GMII) or one local fault ordered set (50GMII)
- This will happen until PHY TX control state diagram assigns tx_xmii_enable <= TRUE, which only will happen when bidirectional link is established (link_status = OK) and no BER test mode has been configured
- Therefore, the 80 65-bit blocks of each RS-FEC CW encodes the same pre-defined information; 20-bit PHD sub-blocks are in general different for each RX-FEC CW, so the parity as well
- However, the output of RS-FEC is scrambled ….

Data-aided TR and EQ support

166.2.2.5 Binary scrambler

The 195 840 bits that compose the aggregation of 36 CW from the output of the RS-FEC encoder shall be scrambled prior to transmission using a binary scrambler that produces the same result as the implementation shown in Figure 166–9.

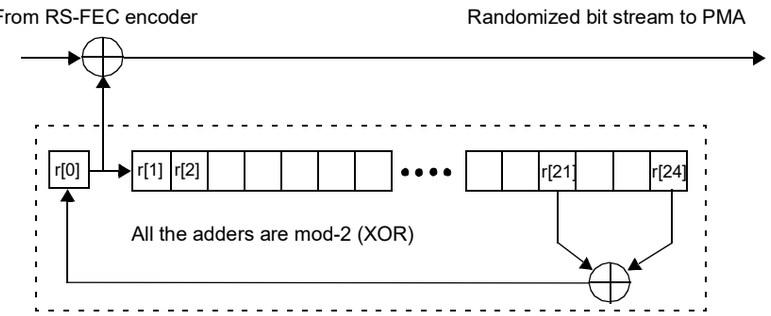


Figure 166–9—Binary scrambler

The block of 195 840 bits generated at the output of the binary scrambler is called Transmit Block.

The shift register of the binary scrambler in Figure 166–9 r[0:24] shall be initialized with 0x0FB9659 for BASE-AU PHYs with parameter $G = 1$ and with 0x020492C for BASE-AU PHYs with parameter $G = 2$ (see Table 166–1), where the leftmost digit corresponds to the initial value of register element r[0]. Therefore, the least significant bit of the rightmost digit corresponds to the initial value of register element r[24].

The initial value of r[0] is xor-ed with the first bit from the RS-FEC encoder to generate the first input bit to the PMA.

The initialization shall be performed at the beginning of each Transmit Block.

- Shift register of the additive binary scrambler is initialized at the beginning of each Transmit Block
- Because of that, the receiver a-priori knows the value of each symbol that is being sent by the transmitter belonging to the first 80 x 65 bits of each RS-FEC CW
- Therefore, the receiver can implement data-aided adaptive algorithms for timing-recovery and equalization using the 95.5% symbols of each Transmit Block
- This is important when eyes are closed, which happens in high rates (10, 25 and 50 Gb/s), high temperature and high attenuation
- Once the algorithms have converged, blind adaptive algorithms can be used for continuous tracking of the varying channel and clock conditions, enabling the transmission of user data (link_status = OK)
- Initialization values (different for NRZ and PAM4) has been selected to maximize detection of the start of Transmit Block by cross correlation

Channel equalization

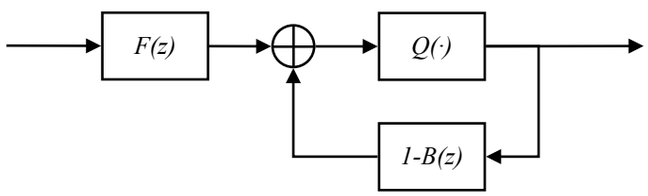
- P802.3cz link model and PHY design is **capacity approaching.**
  - Shannon's capacity in the output of RX is computed based on the PSD of signal and all the noise sources in terms effective SNRe
- In order to approach the channel SNRe, a **canonical equalizer** is used: MMSE-DFE (read [1, 2, 3])
- MMSE-DFE is used for noise whitening and ISI compensation: TX distortion, channel EMB, **RX BW limitation** (the most relevant for rates <= 25 Gb/s)
- MMSE-DFE is essential to support **high insertion loss** channel and compensate **production impairments**
- **Finite length** MMSE-DFE is required in practical implementations so that error propagation is bounded
- Max nº of FBF taps is limited considering the GF size of RS-FEC code, modulation depth and channel response
- **Finite length** MMSE-DFE is defined in **TDFOM**

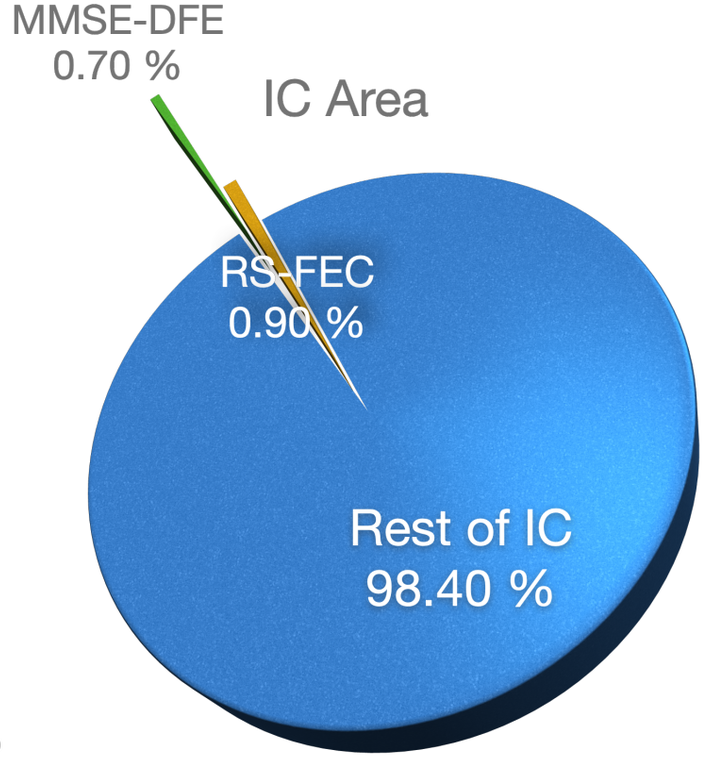
Table 166–16— BASE-AU TDFOM reference equalizer number of taps

Parameter	2.5GBASE-AU	5GBASE-AU	10GBASE-AU	25GBASE-AU	50GBASE-AU
Number of taps of the $F(z)$ filter (N_F)	4			8	
Number of taps of the $B(z)$ filter (N_B)	3				2

$$F(z) = \sum_{i=0}^{N_F - 1} f[i] z^{-i}$$

$$B(z) = 1 + \sum_{i=1}^{N_B - 1} b[i] z^{-i}$$





[1] John M. Cioffi et al., "MMSE Decision-Feedback Equalizers and Coding-Part I: Equalization Results," October 1995, IEEE Transactions on Communications, Vol. 43, No. 10

[2] John M. Cioffi et al., "MMSE Decision-Feedback Equalizers and Coding-Part II: Coding Results," October 1995, IEEE Transactions on Communications, Vol. 43, No. 10

[3] John M. Cioffi, "Equalization", Course EE379A: Digital Communications - Signal Processing, Chapter 3, Stanford University, [Online], Available: https://cioffi-group.stanford.edu/doc/book/chap3.pdf

BASE-U OAM

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OAM channel

Table 115–17—List of all possible 1000BASE-H OAM message status

TXO_REQ	TXO_MSGT	TXO_PHYT	TXO_MERT	Message K + 1 status	Message K status	Message K – 1 status
0	a	a	a	Not written by local STA	Sent by local PHY ACK by remote PHY ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
0	a	!a	!a	Not written by local STA	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
0	a	a	!a	Not written by local STA	Sent by local PHY ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
0	a	!a	a	Not written by local STA	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY No ACK by remote STA
1	a	a	a	Written by local STA Pending transmission by local PHY	Sent by local PHY ACK by remote PHY ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	!a	!a	Written by local STA Pending transmission by local PHY	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	a	!a	Written by local STA Pending transmission by local PHY	Sent by local PHY ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	!a	a	Written by local STA Pending transmission by local PHY	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY No ACK by remote STA

- 802.3cz reuses the OAM channel of 802.3bv
- Separated set of MDIO registers is used
- Robust protocol for exchange of messages is defined so that no messages are lost,
- Even if the PHD link conditions are severely degraded the OAM channel is reliable
- Both STAs are aware of the transmission and reception status of messages

OAM state diagrams

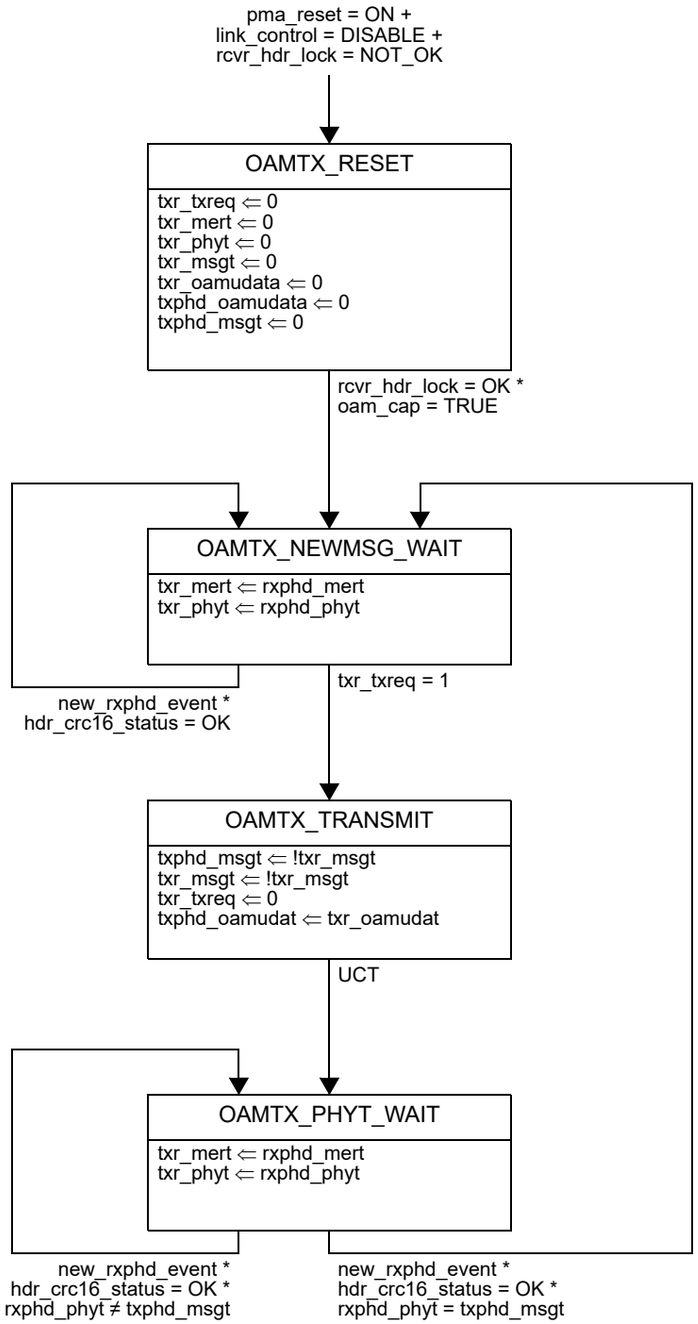


Figure 115–42—PHY 1000BASE-H OAM transmit control state diagram

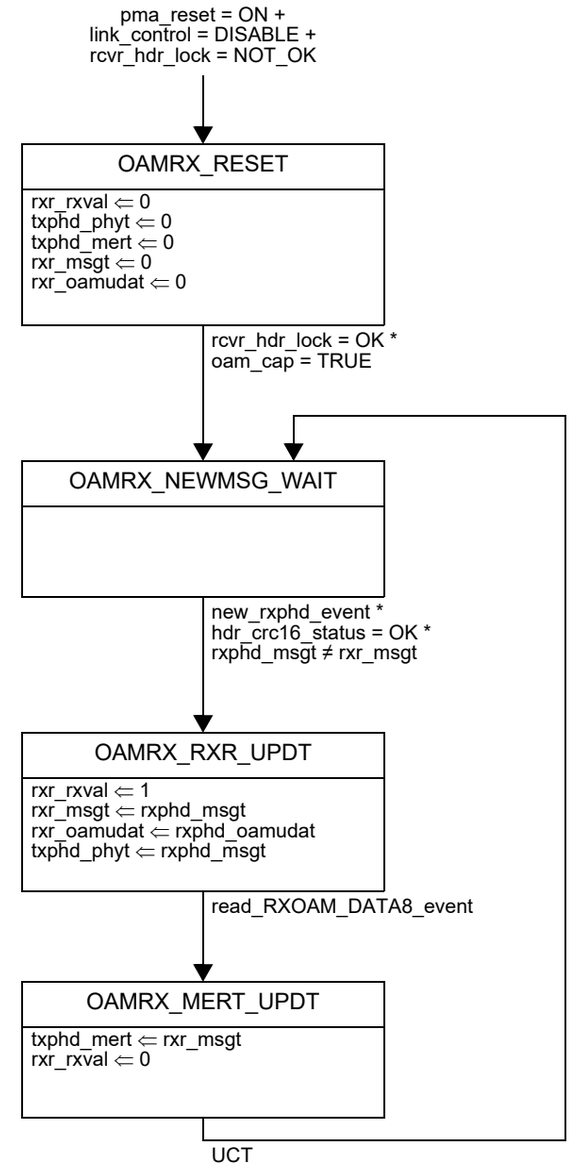


Figure 115–43—PHY 1000BASE-H OAM receive control state diagram

OAM channel, example of message from A to B

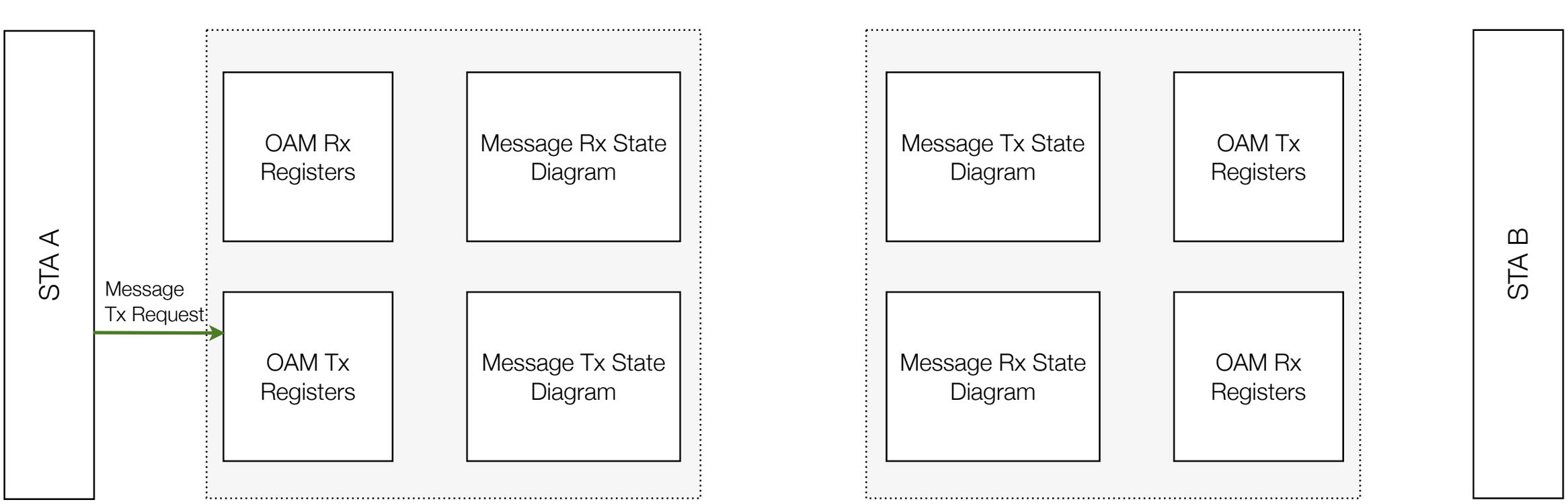
- Step 1: STA A writes OAM message TX registers and raises TXO_REQ bit

OAM Tx registers

TXO_REQ	TXO_PHYT	TXO_MERT	TXO_MSGT
1	***a***	***a***	***a***

OAM Rx registers

RXO_VAL	RXO_MSGT
0	***a***



OAM channel, example of message from A to B

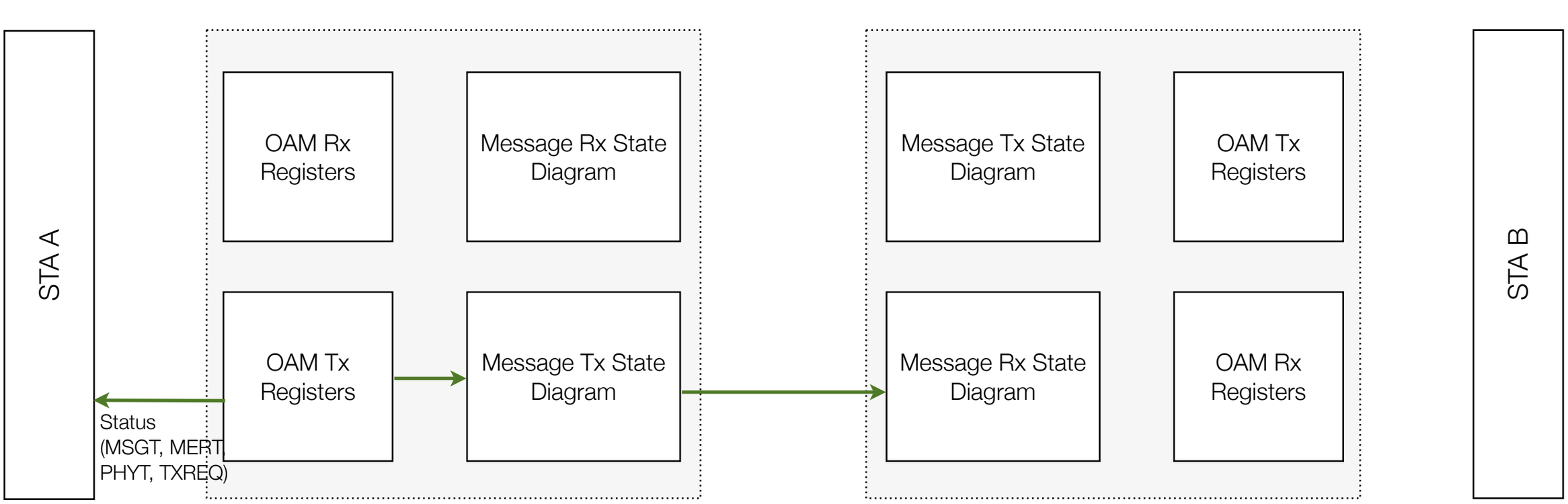
- Step 2: local PHY (A) acknowledges the message to local STA (A) with TXO_MSGT and transmit it to the remote PHY (B)

OAM Tx registers

TXO_REQ	TXO_PHYT	TXO_MERT	TXO_MSGT
0	***a***	***a***	***!a***

OAM Rx registers

RXO_VAL	RXO_MSGT
0	***a***



OAM channel, example of message from A to B

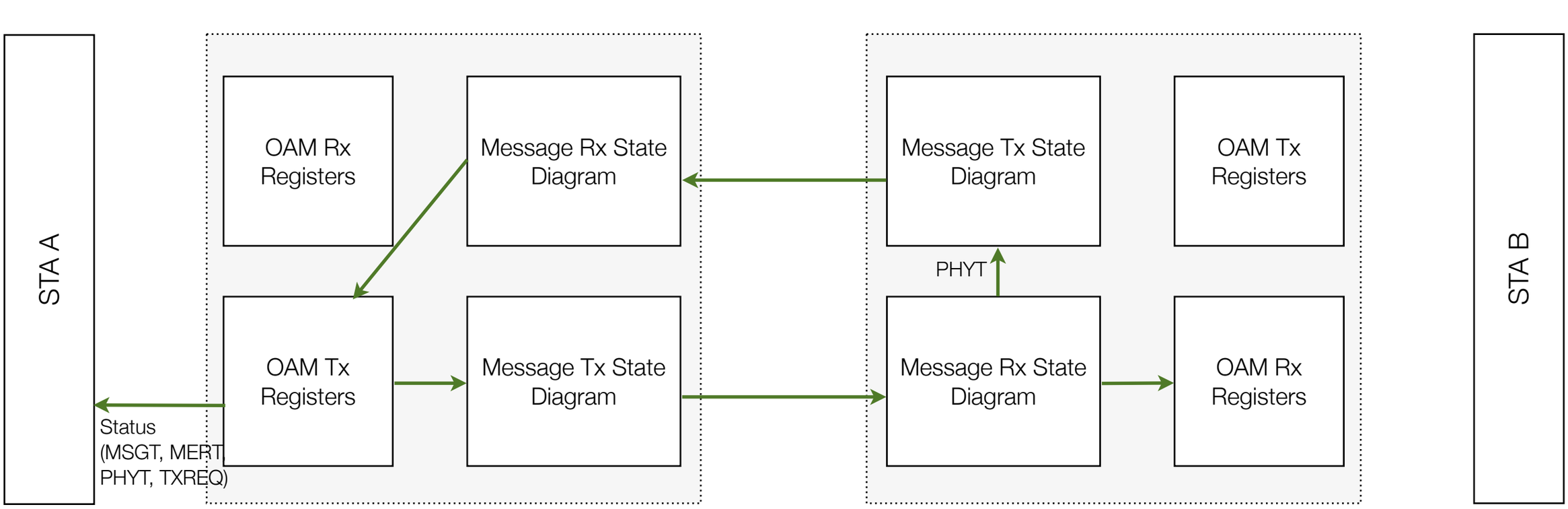
- Step 3: remote PHY (B) receives the message. It signals the reception of the message to the remote STA (B) using RXO_VAL and sends PHYT bit to the local PHY (A) indicating to local STA (A) messages was received by remote PHY (B)

OAM Tx registers

TXO_REQ	TXO_PHYT	TXO_MERT	TXO_MSGT
0	*!a*	*a*	*!a*

OAM Rx registers

RXO_VAL	RXO_MSGT
1	*a*



OAM channel, example of message from A to B

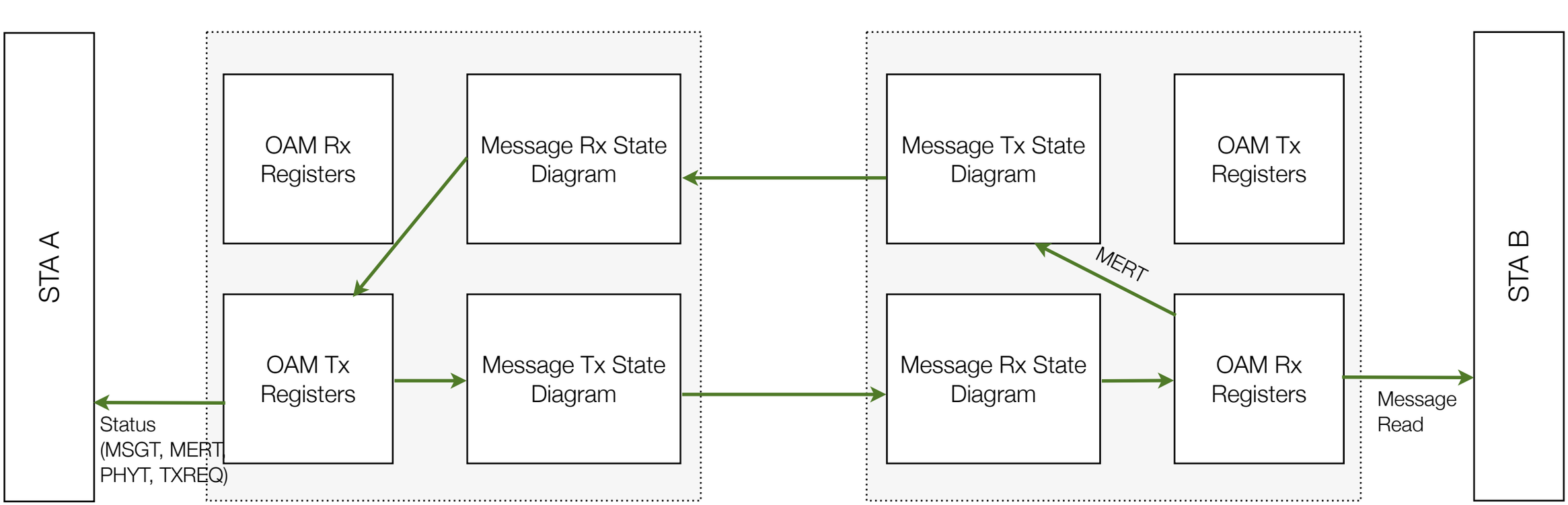
- Step 4: remote STA (B) reads the message, the message read toggle bit MERT reaches the local PHY (A) and it is signaled through the local OAM TX registers to local STA (A) indicating the remote STA (B) already read the message

OAM Tx registers

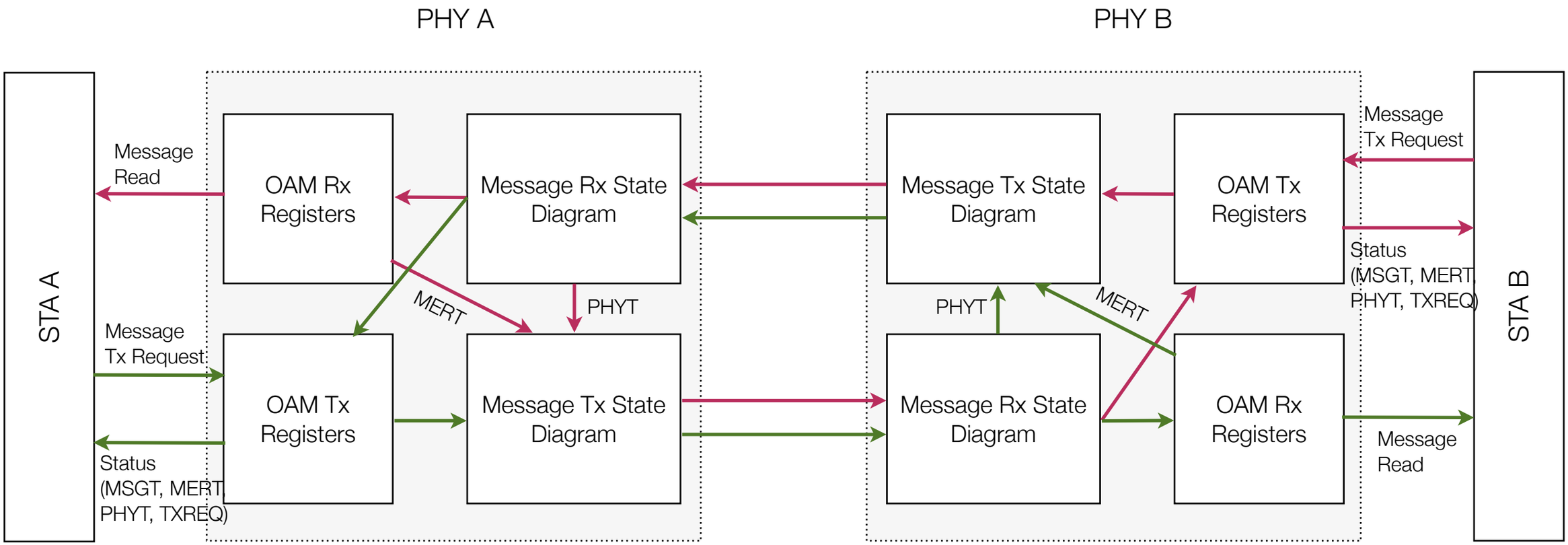
TXO_REQ	TXO_PHYT	TXO_MERT	TXO_MSGT
0	*!a*	*!a*	*!a*

OAM Rx registers

RXO_VAL	RXO_MSGT
0	*!a*



OAM channel, bidirectional TX w/ handshaking



BASE-U EEE

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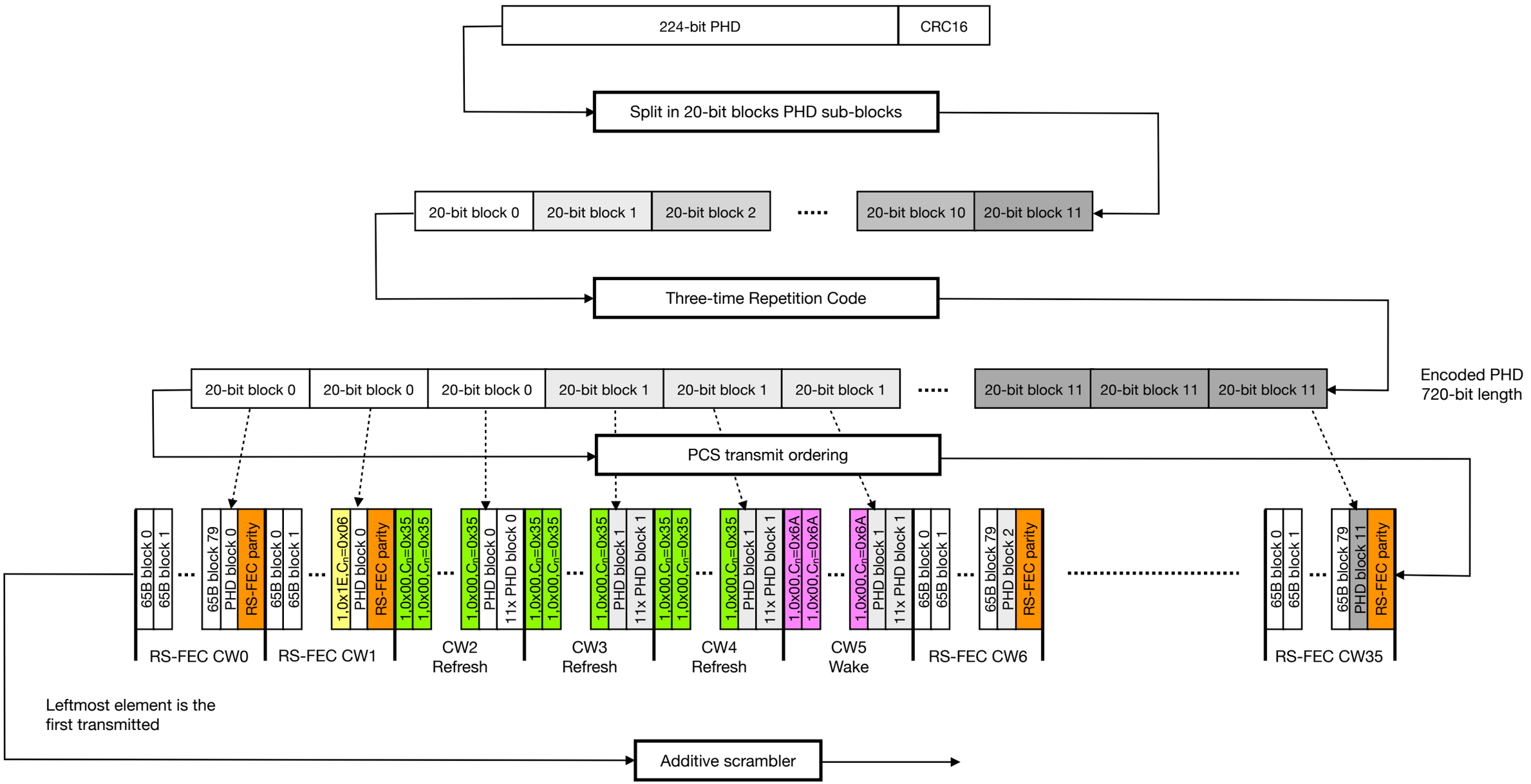
EEE support

- A BASE-U specifies the optional EEE capability following fast wake mode of LPI operation (see 78.1.3.3.1) in the sense that the PHY transmitter remains transmitting signals during LPI (same symbol rate and modulation of normal mode)
- However, the data generated by the PCS sublayer is modified with respect to transparent LPI encoding of normal operation in order to allow power saving, robust OAM side communication channel and robust wake signal detection in the receiver
- Transmitter side is expected to have much lower power consumption than the receiver, in practical implementations. In addition, RS-FEC encoder function can be disabled during LPI

EEE support



Transmit block, composed by 36 RS codewords, 195840 bits

EEE support

- Block type and control codes
  - Block type 0x00 was selected because it is the one with minimum Hamming distance of 4 with all the used block types 0x1E, 0x2D, 0x33, 0x66, 0x55, 0x78, 0x4B, 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1, 0xFF
    - 50GMII uses a subset of block types of XGMI and 25GMII
    - LPI can be detected by the receiver based on detection of the control-data header and the block type field of the 65-bit blocks belonging to the Refresh codewords
  - 7-bit control codes 0x35 (Refresh) and 0x6A (Wake) have been selected to have a minimum Hamming distance of 4 with control codes 0x00 /I/, 0x06 /LI/ and 0x1E /E/ and Hamming distance of 6 between them
    - Wake can be detected by the receiver based on detection of the 7-bit control codes of the 65-bit blocks belonging to the Wake codewords

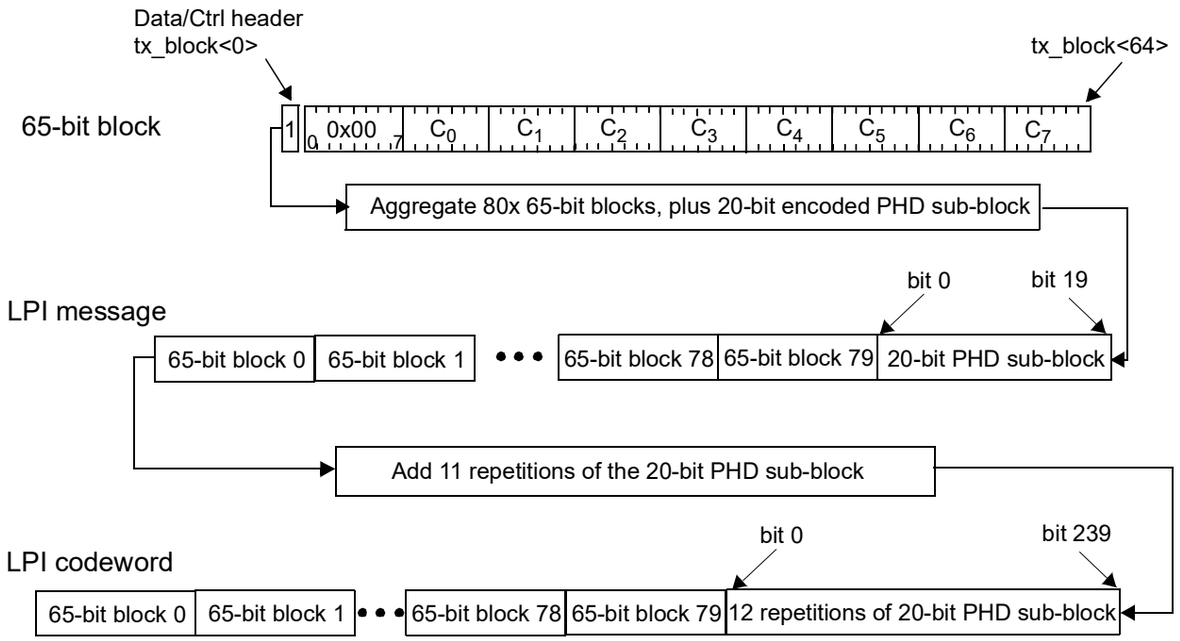


Figure 166–30—LPI codeword transmission

EEE support

- PHD decoding
  - In normal operation, the $BER_{PHD} < 2 \cdot 10^{-24}$ for $RFER < 4.5 \cdot 10^{-10}$ ($BER_{PAYLOAD} < 10^{-12}$) after RS-FEC decoding and TRC decoding
  - In LPI mode, there is a concatenation of mRC (m-time repetition code) with the TRC
    - For m = 11: $BER_{PHD} < 7.4 \cdot 10^{-41}$, after mRC and TRC decoding
    - For m = 9: $BER_{PHD} < 2.0 \cdot 10^{-34}$
    - For m = 7: $BER_{PHD} < 5.6 \cdot 10^{-28}$
    - For m = 5: $BER_{PHD} < 1.7 \cdot 10^{-21}$
    - For m = 3: $BER_{PHD} < 6.7 \cdot 10^{-15}$
    - Selection of m value for the 20-bit PHD sub-blocks decoding depends on receiver implementation
- Receiver power saving depends on the implementation, but in general:
  - After detected LPI, while receiving Refresh codewords, the receiver only needs to sample, equalize and detect a small portion of symbols for each codeword: only the last *n* 65-bit blocks plus the first *m* repeated 20-bit PHD sub-blocks are needed to detect Wake codeword and make robust decoding of PHD content
  - Example: if *n* = 1 and *m* = 7, the (1x65 + 7x20)/5440 = 0.0376 —> less than 4% of the symbols per codeword need to be received
  - In addition, RS-FEC decoder can be fully disabled in LPI
  - Values for *n* and *m* depend on the receiver implementation

Link budget comparison: BASE-AU vs BASE-SR

BASE-AU vs BASE-SR

Characteristics	BASE-AU	BASE-SR
Data-rates	2.5, 5, 10, 25, 50	10, 25, 50
Application T_{BS} range (C)	−40 to +125	0 to +85
OAM channel support	**YES** OAM channel is an Automotive requirement 802.3bp, 802.3bv, 802.3ch, P802.3cy specifies OAM. OAM is also operative during LPI.	**NO**
Dependability functions support (link margin, OAM)	**YES**	**NO**
Link establishment is bidirectional	**YES**	**NO**
EEE support	PHY TX remains transmitting signals during LPI, however data generated by PCS is modified wrt normal operation to allow big power saving , while OAM channel is operative and wake signal detection is robust. LPI is defined for 2.5, 5, 10, 25, and 50 Gb/s.	Fast wake mode, where PCS encodes LPI as in normal operation. Power saving is very limited in the receiver. LPI is only defined for 25 and 50 Gb/s.
Data-aided timing-recovery supported	**YES** Required the highly sensitive RX for high insertion loss channels	**NO**
Data-aided equalization supported	**YES** Required the highly sensitive RX for high insertion loss channels	**NO**
Design startegy	**Maximize supported channel insertion loss**	**Maximize link distance**
Modal dispersion	Small impact	Defines the max distance by ISI limitation. Specially relevant in 10 Gb/s
Chromatic dispersion	Negligible impact	Defines the MPN with RMS width. Specially relevant in 10 Gb/s
Mode Partition Noise	Negligible impact	Limit the channel capacity. Specially relevant in 10 Gb/s
Main noise limitation	Receiver (PD, TIA, Sampling)	Transmitter (RIN, MPN)
Link budget	**Limited by TX distortion and RX noise**	**Limited by TX and channel distortions, MPN and RIN**
Transmitter is validated with equalized reference RX	**YES**, for all the rates (Decision Feedback Equalizer)	**NO** for 10 and 25 Gb/s. **YES** for 50 Gb/s (linear Feed-Forward Equalizer)

Link budget comparison for 25 Gb/s

	25GBASE-AU		25GBASE-SR	
Characteristics	**Value**	**Notes**	**Value**	**Notes**
Max $RIN_{12}OMA$ (dB/Hz)	-124		-128	
Max variation of wavelength center (nm)	+/- 10		+/- 10	
Max RMS spectral width (nm)	0.7		0.6	
Min ER (dB)	4		2	
FEC	RS (544, 522), t = 11, GF(2^{10})		RS (528, 514), t = 7, GF(2^{10})	
Max operating distance OM3 (m)	40		70	
Min EMB (MHz·km)	950		2000	
Min electrical BW (GHz)	**16.8**		**20.2**	**> (0.75 x 25.78125). Therefore TDEC is mostly determined by TX**
Min OMA TP2 (dBm)	**-0.5**	TDFOM = 1 dB	**-3.0**	TDEC = 4.3 dB
Max OMA TP3 stressed sensitivity (dBm)	**-9.6**	TDFOM = 1 dB	**-5.2**	SEC = 4.3 dB
OMA_{TP2} minus stressed OMA_{TP3} budget (dB)	9.1		2.2	
Max channel insertion loss (dB)	8.5		1.8	
Stressed budget minus channel insertion loss (dB)	**0.6**	0.2 dB are allocated for bending. 0.4 dB for MN	**0.4**	
Connectors insertion loss (dB)	**8.0**		**1.5**	
Max cable insertion loss (dB)	**0.5**		**0.3**	

6.9 dB gap

TX 2.5 dB **RX 4.4 dB**

and different environmental conditions

Link budget comparison for 10 Gb/s

	10GBASE-AU		10GBASE-SR	
Characteristics	**Value**	**Notes**	**Value**	**Notes**
Max $RIN_{12}OMA$ (dB/Hz)	-120		-128	
Max variation of wavelength center (nm)	+/- 10		+/- 10	
Max RMS spectral width (nm)	0.7		0.05 to 0.45	Center wavelength and width define min OMA at TP2, because wavelength defines EMB and RMS width defines MPN.
Min ER (dB)	4		3	
Forward Error Correction	RS (544, 522), t = 11, GF(2^{10})	Common to all the rates. Allows for better sensitivity, robust implementation, higher yield, lower cost	NO	
Max operating distance OM3 (m)	40		300	
Min Effective Modal Bandwidth (MHz·km)	950	EMB is reduced at 980nm	2000	
Min electrical bandwidth (GHz)	**16.8**		**4.7**	Important contributor to VECP for long channels
Min OMA TP2 (dBm)	**-1.7**	TDFOM = 1 dB	**-3.8**	@ wc 840nm & ww 0.29nm
Min OMA TP3 non-stressed sensitivity (dBm)	**N/A**		**-11.1**	No eye closure. Optional characteristic.
Max OMA TP3 stressed sensitivity (dBm)	**-12.8**	TDFOM = 1 dB	**-7.5**	VECP = 3.5 dB
OMA_{TP2} minus non-stressed OMA_{TP3} budget (dB)	**N/A**		**7.3**	**No eye closure penalty (very short OM3, ideal TX with no eye closure)**
OMA_{TP2} minus stressed OMA_{TP3} budget (dB)	**11.1**		**3.7**	VECP = 3.5 dB
Max channel insertion loss (dB)	**10.5**		**2.6**	
Stressed budget minus channel insertion loss (dB)	**0.6**		**1.1**	
Connectors insertion loss (dB)	**10.0**		**1.5**	
Max cable insertion loss (dB)	**0.5**		**1.1**	

3.8 dB gap

TX 2.1 dB **RX 1.7 dB** **and different environmental conditions**

Suitability of BASE-U for GI-POF

OM3 vs GI-POF link budget for 25 Gb/s

	25BASE-AU (OM3)		25BASE-PU (GI-POF)	
Characteristics	**Value**	**Notes**	**Value**	**Notes**
Max operating distance (m)	**40**		**15**	Objective
Min EMB (MHz·km)	**950**		**200**	Convervative
Min electrical BW (GHz)	**16.8**		**9.4**	Convervative
Max fiber attenuation (dB/km)	**2**		**100**	GIPOF vendor proposal
Max fiber attenuation (dB)	0.1		1.5	
Max cable attenuation aging (dB)	0.4		1.0	Assumption based on experience with SI-POF (additional +0.6 dB)
Max cable insertion loss (dB)	0.5		2.5	
Macro-bending loss (dB)	0.2		0.2	
Allocation for modal noise (dB)	0.4		0.4	
Max insertion loss per inline connector (dB)	2.0		2.5	Assumed extra 0.5 dB, because concentricity of 490/55 vs 125/50
Max number of inline conenctions	4		2	
Connectors insertion loss (dB)	**8**		**5**	
Max channel insertion loss (dB)	**8.5**		**7.5**	
Min OMA TP2 (dBm)	**-0.5**	TDFOM = 1 dB	**-0.5**	TDFOM = 1 dB
Max OMA TP3 stressed sensitivity (dBm)	**-9.6**	TDFOM = 1 dB	**-8.6**	TDFOM = 1 dB. 1 dB sensitivity penalty wrt OM3 is due to GI-POF ISI
OMA_{TP2} minus stressed OMA_{TP3} budget (dB)	**9.1**	**1.0 dB diff**	**8.1**	
Stressed budget minus channel insertion loss (dB)	**0.6**		**0.6**	
Stressed budget minus channel insertion loss and allocations for bending and modal noise (dB)	**0.0**		**0.0**	

OM3 vs GI-POF link budget for 10 Gb/s

	10BASE-AU (OM3)		10BASE-PU (GI-POF)	
Characteristics	**Value**	**Notes**	**Value**	**Notes**
Max operating distance (m)	**40**		**15**	Objective
Min EMB (MHz·km)	**950**		**200**	Convervative
Min electrical BW (GHz)	**16.8**		**9.4**	Convervative
Max fiber attenuation (dB/km)	**2**		**100**	GIPOF vendor proposal
Max fiber attenuation (dB)	0.1		1.5	
Max cable attenuation aging (dB)	0.4		1.0	Assumption based on experience with SI-POF (additional +0.6 dB)
Max cable insertion loss (dB)	0.5		2.5	
Macro-bending loss (dB)	0.2		0.2	
Allocation for modal noise (dB)	0.4		0.4	
Max insertion loss per inline connector (dB)	2.5		2.5	
Max number of inline conenctions	4		3	
Connectors insertion loss (dB)	**10**		**7.5**	
Max channel insertion loss (dB)	**10.5**		**10.0**	
Min OMA TP2 (dBm)	**-1.7**	TDFOM = 1 dB	**-1.7**	TDFOM = 1 dB
Max OMA TP3 stressed sensitivity (dBm)	**-12.8**	TDFOM = 1 dB	**-12.3**	TDFOM = 1 dB. 0.5 dB sensitivity penalty wrt OM3 is due to GI-POF ISI
OMA_{TP2} minus stressed OMA_{TP3} budget (dB)	**11.1**	**0.5 dB diff**	**10.6**	
Stressed budget minus channel insertion loss (dB)	**0.6**		**0.6**	
Stressed budget minus channel insertion loss and allocations for bending and modal noise (dB)	**0.0**		**0.0**	

Conclusions

- Comprehensive rational behind the design of P802.3cz BASE-U PCS and PMA in comparison with BASE-R has been presented
- BASE-U PCS/PMA design obeys to specific requirements of functionality, performance and environmental conditions of the targeted automotive application
- Link budget analysis for 10 and 25 Gb/s for OM3 and GI-POF channels have been presented considering BASE-U PCS/PMA: channel **insertion losses** and **link budget** are **similar** in P802.3cz and P802.3dh

- **Based on all the presented data, I propose to adopt BASE-U PCS and PMA for 802.3dh**
- **If we do changes in components for .3dh wrt .3cz that DO NOT rely on GIPOF itself (i.e. the reason behind .3dh), confusion will be created in the market that will affect the success of both standards**

Thank you