Many state diagrams in this draft as well as in the base standard use the operator "++" to indicate that the variable be incremented by 1. However, this operator is never defined.

**Suggested Remedy**

- Import Clause 21 and "++".
- Amend 21.5 to include definition of "++".
- Delete the following from state diagram conventions in multiple clauses: "The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented."

**Proposed Response**

**PROPOSED ACCEPT IN PRINCIPLE.**

Import Clause 21 and "++".
Amend 21.5 to include definition of "++".
Delete the following from state diagram conventions in 175.2.6.1, 176.5.1.6, 177.6.1, 184.6.1, 176A.10.1.

"The notation ++ after a counter or integer variable indicates that its value is to be incremented."

Implement with editorial license.

---

**Comment Type:** TR

**Comment Status:** D

**Page:** 5 of 57

**SOORT ORDER:** Clause, Subclause, page, line

**Comment Status:** D

**Response Status:** W

**Comment Status:** D

**Response Status:** W
Comment Type TR Comment Status D 800BASE-ER1 is defined as using 800BASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800BASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." This PHY as noted in Table 169-3a, uses PCS encoding as defined in Clause 186.

Suggested Remedy

Define new name for family/encoding based on Clause 186 encoding.

Proposed Response  

PROPOSED ACCEPT IN PRINCIPLE. The comment correctly points out that the definition is not correct. However, it is not necessary to define a new family.

Change the definition of 800BASE-ER1 and 800BASE-ER1-20 to the following:

1.4.184da 800BASE-ER1: IEEE 802.3 Physical Layer specification for 800 Gb/s PHY using 800BASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 40 km. (See IEEE Std 802.3, Clause 186 and Clause 187). 

1.4.184db 800BASE-ER1-20: IEEE 802.3 Physical Layer specification for 800 Gb/s PHY using 800BASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 20 km. (See IEEE Std 802.3, Clause 186 and Clause 187).

Implement with editorial license.

Comment Type TR Comment Status D 800BASE-ER1-20 is defined as using 800BASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800BASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." This PHY as noted in Table 169-3a, uses PCS encoding as defined in Clause 186.

Suggested Remedy

Define new name for family/encoding based on Clause 186 encoding.

Proposed Response  

PROPOSED ACCEPT IN PRINCIPLE. Resolve using the response to comment #309.

Comment Type T  Since 800BASE-ER1 and -ER1-20 have a separate PCS, the definition for 800BASE-ER1 and ER1-20 should refer to 800BASE-ER1 encoding rather than 800BASE-R encoding.

Suggested Remedy

Change 800BASE-R to 800BASE-ER1 for both the ER1 and ER1-20 definitions.

Proposed Response  

PROPOSED ACCEPT IN PRINCIPLE. Resolve using the response to comment #309.

Comment Type T  The abbreviation "MLSD" is used numerous times in Annex 178A to reference Maximum Likelihood Sequence Detection and should be added to the abbreviations list.

Suggested Remedy

Add MLSD | Maximum Likelihood Sequence Detection

Proposed Response  

PROPOSED ACCEPT IN PRINCIPLE. Implement suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment Type:** TR  **Comment Status:** D  **timesync (bucket)**

He, Xiang  
Huawei  

Add TimeSync entity managed object classes for Inner FEC sublayers defined in Clause 177 and 184.

**Suggested Remedy:**  
(Presentation will be prepared for this comment.)

**Response Status:** W  
**Proposed Response:** PROPOSED REJECT.

The following related presentation was reviewed by the 802.3dj task force during the May Interim meeting:  
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf  
This presentation does not provide sufficient detail to describe the requested change in Clause 30.

**Comment Type:** T  **Comment Status:** D  **timesync (bucket)**

Huber, Thomas  
Nokia  

There should also be an entry for 800GBASE-ER1 since it is a different PCS

**Suggested Remedy:**  
Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R. (or before the entry for 800GBASE-R).

**Response Status:** W  
**Proposed Response:** PROPOSED ACCEPT.

The register bits and names described on page 8 of the presentation will be used with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement the register bits and names described on page 8 of the presentation and with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement with editorial licence.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type** TR  
**Comment Status** D  
**Comment** Add MDIO interface registers for Inner FEC sublayers defined in Clause 177 and 184.

**Suggested Remedy**
Add definitions for the new register set defined for the Inner FEC sublayers in 30.3.1.1 - 30.1.1.14.

(Presentation will be prepared for this comment.)

**Proposed Response**

PROPOSED REJECT.
The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf
This presentation concerns TimeSync management and refers to the register set "30.13.1.1 – 30.13.1.14" rather than "30.3.1.1 – 30.1.1.14".
A different comment (#603) addresses adding registers for inner FEC TimeSync. Another comment (#183) concerns adding additional status counters for the inner FEC which will require new registers.
There is insufficient detail given in this comment (#370) and comment #183 to make a change to Clause 45 for inner FEC register definitions at this time.

**Comment Type** T  
**Comment** Shouldn't LR4 come before LR1 (same reach, narrower) and the order goes up the page, counting the bits forward.

**Suggested Remedy**
Swap 800GBASE-LR4 and 800GBASE-LR1

**Proposed Response**

PROPOSED ACCEPT.

**Comment Type** T  
**Comment** 800GBASE-DR4-2 has longer reach than 800GBASE-FR4-500

**Suggested Remedy**
Swap them

**Proposed Response**

PROPOSED ACCEPT.

**Comment Type** TR  
**Comment** Table 73-5 is missing the indication of highest priority.

**Suggested Remedy**

**Proposed Response**

PROPOSED REJECT.
Table 73-5 already indicates "lowest priority" and 73.7.6 contains this text "priority as defined in Table 73–5 (listed from highest priority to lowest priority)". So adding "highest priority" in the Table 73-5 is redundant.
In table 90A-1, the column titled "Alignment marker/ codeword marker insertion/removal" has a value of 2.56ns for 1.6T in the last row. This value should be the xMII time (at MAC data rate) of one Alignment marker block. The 1.6TE PCS lanes are now running at 100G vs 25G for slower speeds, so this number does not scale directly from the other entries. The value for the 1.6T row should be 1.28ns (a full AM group = 8 256b/257b blocks, so the MII time = 8 * 256 / 1600 = 1.28ns). Note that this column has correct values for 25G, 40G, 50G, and 100G. However, the value listed for 200G, 400G and 800G of 2.56ns should be 5.12ns and should also be fixed in maintenance.

**Suggested Remedy**

Change the accuracy impairment value of 2.56 ns to 1.28 ns for the 1.6T Ethernet rate in Table 90A-1.

**Proposed Response**

PROPOSED ACCEPT.

---

For the added row in Table 90A-1, the potential timestamp accuracy impairment due to alignment marker insertion/removal for 1.6T is incorrect. It should be 1.28ns, not 2.56ns. The values for 200G, 400G, and 800G are also erroneous (should all be 5.12ns). I've filed a maintenance request to correct these, too.

**Suggested Remedy**

Change 2.56 to 1.28ns in the added row for Table 90A-1

**Proposed Response**

PROPOSED ACCEPT.

---

In table 116-3, the last two columns, missusage of PMD names.

**Suggested Remedy**

change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 200GBASE-KR1 and 200GBASE-CR1

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE. Implement the suggested remedy with editorial license.

---

**Suggested Remedy**

change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 400GBASE-KR2 and 400GBASE-CR2

**Proposed Response**

PROPOSED ACCEPT.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Comment Type: TR  Comment Status: D

200GBASE-R SM PMA delay constraint is missing

Suggested Remedy

PROPOSED REJECT.
A suggested remedy is not provided.

200GBASE-R 8:1, 1:8, and 1:1 PMA types, all SM-PMA types are listed. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.

Comment Status: D
Response Status: W

Proposed Response

Mi, Guangcan
Huawei Technologies Co., Ltd

Comment Type: TR  Comment Status: D

In Table 116-9, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

Suggested Remedy

change the content of row SP1 and SP6 in the column of 113.4375Gb/s PMD lane to N/A

Proposed Response

PROPOSED ACCEPT.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Cl 116  SC 116.1.4  P94  L6  # 312
D’Ambrosia, John  Futurewei, U.S. Subsidiary of Huawei

Comment Type  TR  Comment Status  D  Conditional PMA (bucket)

200/400G BASE-R BM-PMA and 200/400G BASE-R SM-PMA are noted as optional in Tables 116-3, 116-4, and 116-4a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not.

Suggested Remedy
For 100Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE-R SM PMA is "C" / conditional if either 200GAUI-1 is implemented. For 200Gb/s based PHYs the 200GBASE-R SM-PMA is mandatory, all AUIs are optional, and 200GBASE-R BM PMA is "C" / conditional if either 200GAUI-2 is implemented. For 100Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE-R SM PMA is "C" / conditional if either 400GAUI-2 is implemented. For 200Gb/s based PHYs the 400GBASE-R SM-PMA is mandatory, all AUIs are optional, and 400GBASE-R BM PMA is "C" / conditional if either 400GAUI-4 is implemented.

Change entries as described above in Tables 116-3, 116-4 and 116-4a for 800GBASE-R BM-PMA and 800GBASE-R SM-PMA to C / with notes as stated above.

Modify entry in Table 178-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C is implemented. Modify entry in Table 178-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-2 C2C is implemented. Modify entry in Table 179-1 to 200GBASE-R SM PMA to Conditional. Add note "c" A 200GBASE-R SM PMA must be implemented if a 200GAUI-1 C2C is implemented. Modify entry in Table 179-2 to 400GBASE-R SM PMA to Conditional. Add note "c" A 400GBASE-R SM PMA must be implemented if a 400GAUI-2 C2C is implemented. Modify entry in Table 181-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented. Modify entry in Table 182-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-4 C2C/C2M is implemented. Modify entry in Table 182-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented.

Proposed Response  Response Status  W  PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #317.

Cl 116  SC 116.2.4  P99  L1  # 313
D’Ambrosia, John  Futurewei, U.S. Subsidiary of Huawei

Comment Type  TR  Comment Status  D  PMA introduction (bucket)

There is no PMD called 400GBASE-LR4.

Suggested Remedy
Change 400GBASE-LR4 to 400GBASE-LR4-6.

Proposed Response  Response Status  W  PROPOSED ACCEPT.

Cl 116  SC 116.2.4  P99  L1  # 314
D’Ambrosia, John  Futurewei, U.S. Subsidiary of Huawei

Comment Type  TR  Comment Status  D  PMA introduction (bucket)

In support of 200 Gb/s per lane signaling - 200GBASE-R BM-PMA and 400GBASE-R PMA, Clause 176 was developed. No addition was made to 116.2 Summary of 200GbE and 400 GbE sublayers was made.

Suggested Remedy
Modify last sentence of 116.2.4 and add additional text. The 200GBASE-R and 400GBASE-R PMAs, which supports bit multiplexing, is specified in Clause 120. The 200GBASE-R and 400GBASE-R PMAs, which supports symbol multiplexing, is specified in Clause 176. Note that "PMA" is used as a general term to represent both types of PMAs for each speed.

Proposed Response  Response Status  W  PROPOSED ACCEPT IN PRINCIPLE.
The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA. Implement the following with editorial license:
Replace the second sentence in 116.2.4 with appropriate editorial instructions to the following:
200GBASE-R and 400GBASE-R PMAs that use bit multiplexing (BM-PMA) are specified in Clause 120. 200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176. Implement with editorial license.
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Comment Type: T  Comment Status: D  (bucket)
A new footnote has appeared "At the PCS receive input, 1 UI is equivalent to 1 bit." attached to an unchanged number. There is no equivalent footnote for Table 116-8. In 802.3, "bit" means MAC bit. I don't know what point the footnote is making - that PCS lanes use binary signalling not PAM4? Nor why it is here. If it were kept, it should say "1 bit on a PCS lane" or similar.

Suggested Remedy:
Delete footnote f

PROPOSED REJECT.
The interface between the PMA and the PCS is an abstract interface. UI interval is the time span of a symbol. Since there there is no physical signal here, only bits are exchanged. The note clarifies that for this interface 1 UI is equivalent to 1 bit being transferred.

Comment Type: T  Comment Status: D  (bucket)
I understand why the use of the stateless encoder decoder is restricted to 200GBASE-R, and 400GBASE-R over 200Gbps lanes. Allowing it on other PMDs/AUIs would be out-of-scope for the 802.3dj project.

HOWEVER, shouldn't common sense prevail, here?
The stateless encoder/decoder was designed such that it is all-but-identical to the stateful encoder, only differing in their treatment of /E/ blocks. Since the 200GBASE-R and 400GBASE-R links are always protected by FEC, it is not as if /E/ blocks can occur at random causing divergent behaviour of the two encoder/decoder types.
There is absolutely no danger of causing backward-compatibility issues, because the stateful encoder/decoder are still allowed for all PMDs
The stateless encoder/decoder was added to the standard to allow greater implementation flexibility (removing long timing paths). But any new PCS implementation that may attach to either 100Gbps/lane or 200Gbps/lane PMDs would have to implement the stateful encoder/decoder! With the stateless encoder, the standard is offering more implementation flexibility that implementors cannot actually use.

Suggested Remedy:
Consider removing the restriction on PMD type when using the stateless encoder and decoder in subclauses 119.2.4.1 and 119.2.5.8, respectively.

PROPOSED REJECT.

As stated in the comment itself, adding an option to support stateless encoding/decoding for PHYs that are not part of the 802.3dj project is out-of-scope.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type** T  **Clause Status** D  **Comment** Precoding (bucket)

Clause 176 is for the symbol mux PMA it should not be used for Annex 120F

**Suggested Remedy**
Remove the reference to 176.9.1.2

**Proposed Response**  **Response Status** W
PROPOSED REJECT.

Annex 120F is amended to include 1.6TAUI-16.

176.8.4 defines the 1.6TBASE-R 16:16 PMA, which has a 16-lane interface that can use 1.6TAUI-16 as a physical interface.

176.9.1.2 describes the precoding function for all symbol-muxing PMAs, which can also be used in the aforementioned PMA.

**Comment Type** TR  **Clause Status** D  **Comment** PHY descriptions (bucket)

same as the previous comment on 800GBASE-CR4

**Suggested Remedy**
make the description consistent

**Proposed Response**  **Response Status** W
PROPOSED REJECT.

It is assumed that the referenced "previous comment" is Comment #154. The language used here is consistent with other similar PHY types in this table. There is similar differences between the PHYs described in this table and the definitions in 1.4.

---

**Comment Type** TR  **Clause Status** D  **Comment** PHY descriptions (bucket)

In Table 169-3, Phy type and clause correlation was marked incorrectly for the columns of 8000GBASE-DR8 PMD and 8000GBASE-DR8-2 PMD

**Suggested Remedy**
remove the unnecessary M in the following rows for 800GBASE-DR8 PMD: 800GBASE-DR4, 800GBASE-FR4-500. remove the unnecessary M in the following rows for 800GBASE-DR8-2 PMD: 800GBASE-DR4-2, 800GBASE-FR4, and 800GBASE-LR4.

**Proposed Response**  **Response Status** W
PROPOSED ACCEPT.

**Comment Type** TR  **Clause Status** D  **Comment** PHY descriptions (bucket)

In Table 169-4, the delay constraints on 800GBASE-R BM-PMA and 800GBASE-R SM-PMA are missing

**Suggested Remedy**
add appropriate rows with TBD if no consensus has been built.

**Proposed Response**  **Response Status** W
PROPOSED REJECT.

800GBASE-R 32:4, 4:32, and 4;4, all SM-PMA types are listed in Table 169-4. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.

**Proposed Response**  **Response Status** W
PROPOSED ACCEPT IN PRINCIPLE.

It is assumed that the comment is referring to Table 169-6 rather than the referenced Table 116-6.

Implement the suggested remedy with editorial license.

---

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn

SORT ORDER: Clause, Subclause, page, line

Page 9 of 57  CI 169  5/30/2024  4:14:17 PM
Comment Type: TR

Suggested Remedy:
- Define new name for family / encoding based on Clause 186 encoding.
- Eliminate table entries for ER1-20 and ER1 from Table 169-3a.
- Create new table for PHY type and clause correlation for new family based on Clause 186 encoding.
- Modify description of entry for 800GBASE-ER1-20 in Table 169-1 to reflect new family name.
- Modify description of entry for 800GBASE-ER1 in Table 169-1 to reflect new family name.

Proposed Response:
- This table lists ALL 800 Gb/s Ethernet PHY types (i.e., 800GBASE), not specifically 800GBASE-R PHY types. The description for 800GBASE-ER1 and 800GBASE-ER1-20 is deceiving and should be updated in line with the definitions in Clause 1. Table 169-3a, lists 800GBASE optical coherent PHY types (not specifically 800GBASE-R), so a separate nomenclature table is not required for 800GBASE-ER1/ER1-20.
- Resolve using the response to comment #315.
In Table 169-2 introduces the 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA in Table 169-2, but there is no real explanation to the use of the sub-layers - just the required PMA service interfaces, as noted in Items C&E. The clarification of these two sublayers is actually defined in 176.2 Conventions, which doesn't make sense.

Suggested Remedy
Move definitions of 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA from 176.2 to 169.1.3 Nomenclature

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.

The terms BM-PMA and SM-PMA are defined in 120.1.1 and 176.1.1. The same terms are listed in 176.2, but the items in this larger list are terms for use only within Clause 176. The definition of BM-PMA and SM-PMA should remain in the subclauses listed above. But they should also be introduced Clause 169.

Resolve using the response to comment #318.

In Table 169-2, 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA are noted as optional in Tables 169-2, 169-3, and Table 169-3a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not.

Suggested Remedy
For 100Gb/s based PHY's the 800GBASE-R BM-PMA is mandatory, all AUIs are optional, and 800GBASE R SM PMA is "C"/ conditional if either 800GAUI-4 is implemented. For 200Gb/s based PHY's the 800GBASE-R SM-PMA is mandatory, all AUIs are optional, and 800GBASE R BM PMA is "C"/ conditional if either 800GAUI-8 is implemented.

Change entries as described above in Tables 169-2, 169-3 and 169-3a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C/ with notes as stated above.

Modify entry in Table 178-3 to 800GBASE-R BM-PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 179-3 to 800GBASE-R SM-PMA to Conditional. Add note "c" A 800GBASE-R SM PMA must be implemented if a 800GAUI-4 C2C is implemented. Modify entry in Table 180-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-4 C2C is implemented. Modify entry in Table 181-1 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-4 C2C is implemented. Modify entry in Table 182-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 183-1 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.

Some guidance as to when the two PMA types are used would be helpful. However, it is not as simple as proposed in the suggested remedy. Guidance is required for all PMAs used within the various xAUIs. Annex 176B provides all of the necessary guidance. Each of the tables listing physical layer clauses associated with PMD types (e.g., Table 180-3 for 800GBASE-DR4) already include a reference to Annex 176B for the AUIs, but not for the two PMA types. Additional guidance in these tables would be helpful.

In the nomenclature tables in Clause 169 it is not necessary to repeat all of these details nor is there any space in these already crowded tables; instead it would be sufficient, efficient, and future-proof to point back to the PMD clauses for guidance.

For each new PMD (Clauses 178, 179, 180 to 183, 185, 186), update the PMD tables in the PMD clause and the associated nomenclature table in Clause 116, 169, and 174, similar to the following for the 800GBASE-DR4 defined in Clause 180.

In Table 180-1, for the 800BASE-R BM-PMA row, change "Optional" to "Conditional" with the following footnote:
"If one or two 800GAUI-n is implemented in a PHY, additional 800GBASE-R BM-PMA or SM-PMA sublayers are required according to the guidelines in Annex 176B.6.1."

Proposed Response
There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500. 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4.

Suggested Remedy
Delete the offending "M"s

Proposed Response
PROPOSED ACCEPT.
There are errors in Table 169.3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500. 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4.

Suggested Remedy
Delete the offending "M"s

PROPOSED ACCEPT.

---

For 800GBASE-LR1 in Table 169.3a:
800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M

Suggested Remedy
Change entries for 800GBASE-LR1 to C for 800GBASE-R BM-PMA and 800GBASE-R SM-PMA
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #317.
[Editor’s note: Changed subclause from 169.1.3 to 169.1.4]
### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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**Comment Type**: TR  **Comment Status**: D

D'Ambrosia, John  Futurewei, U.S. Subsidiary of Huawei

**PMA introduction (bucket)**

In support of 200 Gb/s per lane signaling - 800GBASE-R BM-PMA, Clause 176 was developed. No addition was made to 169.2 Summary of 800 GbE architecture.

**SuggestedRemedy**

Modify 169.2.4 to read -

The PMA sublayer provides a medium-independent means to support the use of a range of physical media.

The 800GBASE-R PMA, which supports bit multiplexing, is specified in Clause 173.

The 800GBASE-R PMA, which supports symbol multiplexing, is specified in Clause 176.

Note that "PMA" is used as a general term to represent both types of PMAs.

**Proposed Response**

Extracted as shown.

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</tr>
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</table>

**Comment Type**: TR  **Comment Status**: W

Hube, Thomas  Nokia

**800GBASE-ER1 PCS**

A new 800GBASE-ER1 PCS is defined in clause 186. It should be mentioned in the introduction clause, 169.2.3 ("Physical Coding Sublayer (PCS)" in 802.3df) which currently only refers to the 800GBASE-R PCS.

**SuggestedRemedy**

Add placeholder text for future text.

**Proposed Response**

PROPOSED REJECT.

A similar diagram is needed for 800GBASE-ER1 and 800GBASE-ER1-20 PHYs.

<table>
<thead>
<tr>
<th>CI</th>
<th>SC</th>
<th>P/L</th>
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</thead>
<tbody>
<tr>
<td>169</td>
<td>169.3.2</td>
<td>122</td>
<td>14</td>
</tr>
</tbody>
</table>

**Comment Type**: T  **Comment Status**: D

Huber, Thomas  Nokia

**800GBASE-ER1/-20 PHY**

A similar diagram is needed for 800GBASE-ER1/-20 PHYs.

**SuggestedRemedy**

Use figure 169-2b as a basis. Replace 800GBASE-R PCS with 800GBASE-ER1 PCS, 800GBASE-LR1 Inner FEC with 800GBASE-ER1 PMA, and 800GBASE-R PMD with 800GBASE-ER1 PMA (and of course renams all the service interfaces to align with that).

**Proposed Response**

PROPOSED REJECT.

A similar diagram for 800GBASE-ER1 and 800GBASE-ER1-20 is provided in Clause 185 which specifies both of these PMD types. No other PMD is of this form so it is not necessary to show a common diagram in Clause 169.

<table>
<thead>
<tr>
<th>CI</th>
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<th>P/L</th>
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<tbody>
<tr>
<td>169</td>
<td>169.3.2</td>
<td>122</td>
<td>14</td>
</tr>
</tbody>
</table>

**Comment Type**: TR  **Comment Status**: D

D'Ambrosia, John  Futurewei, U.S. Subsidiary of Huawei

**800GBASE-ER1/-20 PHY**

There is no figure describing 800GBASE-ER1/-20 describing inter-sublayer service interfaces including 800GBASE-ER1 PCS/PMA.

**SuggestedRemedy**

Add placeholder text for future text.

**Proposed Response**

PROPOSED REJECT.

Resolve using the response to comment #78.

<table>
<thead>
<tr>
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<th>SC</th>
<th>P/L</th>
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<tbody>
<tr>
<td>169</td>
<td>169.3.2</td>
<td>122</td>
<td>14</td>
</tr>
</tbody>
</table>

**Proposed Response**

Extracted as shown.

<table>
<thead>
<tr>
<th>CI</th>
<th>SC</th>
<th>P/L</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td>169</td>
<td>169.3.2</td>
<td>122</td>
<td>14</td>
</tr>
</tbody>
</table>
Comment Type: TR  Comment Status: D

The comment refers to Table 169-4. The Inner-FEC delay appears to be missing from the table.

Suggested Remedy:
add 800GBASE-R inner FEC (values are TBDs)

Proposed Response
Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Comment Type: T  Comment Status: D

The title of Clause 173 does include BM.

Suggested Remedy:
Remove the BM- from Table 171-1 for the Clause 173 entry and footnote A

Proposed Response
Response Status: W
PROPOSED REJECT.

The term BM-PMA is used in Table 171-1, because this table includes reference to both BM and SM PMAs, and the convention we agreed on was in such cases to call out both PMAs explicitly. The same convention is used in tables 178-1, 179-1, 180-1, 182-1 and 183-1.
This is explained in 173.1.1 as follows:
"When necessary for disambiguation, to differentiate the bit-multiplexing PMA (BM-PMA) types defined in this clause from the symbol-multiplexing PMA (SM-PMA) types defined in Clause 176, the term BM-PMA is used. Within this clause the term PMA refers specifically to the BM-PMA."

Comment Type: T  Comment Status: D

In tables 171-3 and 171-5, it is not clear what has changed in the rows that are shown.

Suggested Remedy:
Indicate the changes with revision marks

Proposed Response
Response Status: W
PROPOSED REJECT.

Although it may be hard to see, the draft is following 802.3 editing guidelines. The thing that changed in tables 171-3 and 171-5 is that an "_" was added between "FEC_symbol_error_counter" and "<0:31>" in the status variable column. Being added text, the "_" is underlined in keeping with 802.3 editing convention. The missing underscore was missed in the 802.3df draft, including during the final publication review.
Comment Type TR  Comment Status D (bucket)  

In Table 174-4, the notes for 1.6TBASE-KR8 and 1.6TBASE-CR8 says includes the medium in one direction. No length of the medium was provided, nor any explicit delay due to the medium was provided. While In Table 169-4, a definitive of 14ns allocated for one direction through cable medium was provided for 800GBASE-CR4. One would assume 1.6TBASE-CR8 would be consistent with 800GBASE-CR4. The same problem applies to 1.6TBASE-KR8.

Suggested Remedy

Put in explicit allocation of delay constraints for the medium used in 1.6TBASE-CR8 and 1.6TBASE-KR8. Align with that of 800GBASE-CR4 and 800GBASE-KR4, if technically feasibly.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Use the same text used for 800GBASE-KR8/CR8 in IEEE Std 802.3df-2024. For the 800GBASE-KR4 row change the text in the note column to: "Includes allocation of 14 ns for one direction through backplane medium. See 178.6." For 800GBASE-CR4 row change the text in the note column to: "Includes allocation of 14 ns for one direction through backplane medium. See 179.6."

Comment Type T  Comment Status D (bucket)  

Has any thought been given to how to calculate the latency through the 1.6TBASE-R PCS, i.e. the path data delay values for the purposes of TimeSync? I do not see anything within the 1.6TBASE-R PCS that would prevent proper calculation of the path data delay values.

Clause 90.7.1 is instructive here, explaining that the path data delays should be "reported as if the DDMP is at the start of the FEC codeword". However, the existing language in 90.7.1 is awkward for PCSs with more than one FEC engine like the 1.6TBASE-R PCS, which has four FEC codewords in parallel.

Suggested Remedy

No proposed change to Clause 175. Clause 90.7.1 could be cleaned up to account for when there are multiple FEC codewords in parallel, but I assume that is out-of-scope for the 802.3dj project? I'll submit a maintenance request.

Proposed Response Response Status W

PROPOSED REJECT.

The suggested remedy does not propose an actionable (within the draft) remedy.

Comment Type T  Comment Status D (bucket)  

A note that modifying the data stream could affect TimeSync would be useful.

Suggested Remedy

Add the following note:
"NOTE -- Insertion or removal of characters may affect protocols like times synchronization (see 90.4.1.2)"

Proposed Response Response Status W

PROPOSED REJECT.

It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Theme: Cl 175 SC 175.2.4.4 P 173 L 41 # 363

Slavick, Jeff
Broadcom

Comment Status: bucket

The last sentence is giving the transcoded blocks sent to each flow a name. So it's not really making a flow of blocks. If anything it's making a series or stream of blocks.

Suggested Remedy

Change the last sentence to read: "The transcoded blocks sent to flow 0 are referred to as tx_xcoded_f0<256:0> and the ones sent to flow 1 as tx_xcoded_f1<256:0>.

Proposed Response: Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Change:
"This creates two flows of transcoded blocks, tx_xcoded_f0<256:0> to flow 0, and tx_xcoded_f1<256:0> to flow 1."

to:
"This creates two streams of transcoded blocks, tx_xcoded_f0<256:0> to flow 0, and tx_xcoded_f1<256:0> to flow 1."

Theme: Cl 175 SC 175.2.4.5 P 174 L 50 # 331

de Koos, Andras
Microchip Technology

Comment Status: bucket

Different scrambler seeds for the two flows are NOT strictly necessary for the 1.6TBASE-R PCS. The output PCSLs are never bit muxed, so having identical outputs from FEC A and FEC C, for example, should never have any adverse effect on "clock content" of the SerDes output.

It doesn't hurt to have the scramblers be seeded differently, however.

Suggested Remedy

Consider changing the last sentence on page 173 from:

When reset is asserted, the two scramblers shall be initialized to a value other than zero and different from each other.

To:
When reset is asserted, the two scramblers shall be initialized to values other than zero.

Delete the editor's note near top of page 174.

Theme: Cl 175 SC 175.2.4.5 P 174 L 3 # 454

Opsasnick, Eugene
Broadcom

Comment Status: bucket

The Editor's note at the end of subclause 175.2.4.5 "Scrambler" states that there are no requirements or restrictions in the 1.6TE PCS baselines for the scrambler seeds for each flow. The note also mentions that the corresponding sub-clause in 802.3df for 800GE PCS states that the two flows would have identical outputs if the seeds are identical and the data input is identical (such as after reset). The 1.6TE PCS does not have two separate sets of PCSLs like 800GE PCS, but the PCSL formation could have back-to-back repeating RS-symbol values if identical seeds are used. Suggest to require different seeds after reset in the scramblers of each flow as written in the paragraph above the editor's note.

Suggested Remedy

Remove the editor's note at the top of page 174, and leave the wording in 175.2.4.5 as-is with the requirement that the two scramblers are initialized with different seeds.

Proposed Response: Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.

Comment #331 notes that the 1.6T PCS lanes are never bit-muxed so different seeds may not be necessary. While the effect of identical scrambler seeds is worse with bit-muxing than symbol-muxing, there may still be some detrimental effects with symbol muxing. If there are identical seeds and identical data, then the FEC-A and FEC-B codewords would be identical to the FEC-C and FEC-D codewords, respectively. With symbol muxing, the resulting data on a output lane would be symbols {A, B, C, D} where A=C and B=D. In general, it is safer to require different seeds to avoid any potential side-effect. As the comment #331 points out, it doesn't hurt to have the scramblers seeded differently.

Delete the editor's note near top of page 174.

Theme: Cl 175 SC 175.2.4.5 P 174 L 3 # 454

Ofelt, David
Juniper Networks

Comment Status: bucket

Editor's Note asks if we should require different reset values for the scramblers.

Suggested Remedy

Yes, we should!

Proposed Response: Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #454.
<table>
<thead>
<tr>
<th>CI 175</th>
<th>SC 175.2.4.6</th>
<th>P 174</th>
<th>L 42</th>
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<tr>
<td>Slavick, Jeff</td>
<td>Broadcom</td>
<td></td>
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</tbody>
</table>

**Comment Type**: T  **Comment Status**: D  **(bucket)**

- **tx_am_sf** doesn't allow but provides a way to communicate the mandatory degrade status.

**Suggested Remedy**

- Change "allows the local PCS to communicate the status of the FEC degraded feature to the remote PCS" to "communicates the local PCS FEC degraded status to the remote PCS".

**Proposed Response**  **Response Status**: W

**PROPOSED REJECT.** The draft is correct as written, and the proposed change does not improve clarity.

<table>
<thead>
<tr>
<th>CI 175</th>
<th>SC 175.2.4.6</th>
<th>P 175</th>
<th>L 22</th>
<th># 453</th>
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<td>Opsasnick, Eugene</td>
<td>Broadcom</td>
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</tbody>
</table>

**Comment Type**: T  **Comment Status**: D  **(bucket)**

- Sub-clause 172.2.4.6 has a reference to a text file containing the 800GBASE-R alignment marker values. CI 175 should add a similar note with a corresponding text file for the 1.6TBASE-R alignment markers.

**Suggested Remedy**

- Add text near line 22: "NOTE: A text file containing the alignment marker patterns, as shown in Table 175/01 is available at [https://standards.ieee.org/downloads/802.3/](https://standards.ieee.org/downloads/802.3/)."

- A presentation will be submitted with a corresponding text file containing the 1.6TBASE-R AM values.

**Proposed Response**  **Response Status**: W

**PROPOSED ACCEPT IN PRINCIPLE.** Implement the suggested remedy with editorial license.

<table>
<thead>
<tr>
<th>CI 175</th>
<th>SC 175.2.4.6</th>
<th>P 176</th>
<th>L 25</th>
<th># 466</th>
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<tr>
<td>Slavick, Jeff</td>
<td>Broadcom</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Comment Type**: T  **Comment Status**: D  **(bucket)**

- am_mapped_f0 and am_mapped_f1 aren't solely based on the 10b-distribution and we never talk about how this two variables are us splitting the alignment marker group up.

**Suggested Remedy**

- Change:

  - **6The variables am_mapped_f0 and am_mapped_f1 are then derived from 10-bit interleaving the group of 16 alignment markers, am_x, using the following procedure:**
  - **To:**

  - **6The alignment marker group is mapped into variables am_mapped_f0 and am_mapped_f1 as follows. First a 10-bit interleaving the group of 16 alignment markers, am_x, is done using the following procedure:**

**Proposed Response**  **Response Status**: W

**PROPOSED ACCEPT IN PRINCIPLE.** Implement the suggested remedy with editorial license.

**Proposed Response**  **Response Status**: W

**PROPOSED ACCEPT IN PRINCIPLE.** Implement the suggested remedy with editorial license.

**Proposed Response**  **Response Status**: W

**PROPOSED ACCEPT IN PRINCIPLE.** Implement the suggested remedy with editorial license.
<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
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<tbody>
<tr>
<td>175</td>
<td>175.2.4.6.2</td>
<td>177</td>
<td>6</td>
<td>467</td>
</tr>
</tbody>
</table>

- **Comment Type**: T
- **Comment Status**: D

**Proposed Response**

Add a intro to what tx_scrambled is.

**Suggested Remedy**

Change:

- "The variables tx_scrambled_am_f0<10279:0> and tx_scrambled_am_f1<10279:0> are constructed in one of two ways."
- "In each flow a 10280-bit block of data is formed with two FEC codewords worth of message data. tx_scrambled_am_f0<10279:0> in flow 0 and tx_scrambled_am_f1<10279:0> in flow 1 and they are constructed in one of two ways."

**Response Status**: W

**Proposed Accept in Principle**

Implement the suggested remedy with editorial license.

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<table>
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<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
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<td>175</td>
<td>175.2.5.3</td>
<td>182</td>
<td>9</td>
<td>469</td>
</tr>
</tbody>
</table>

- **Comment Type**: T
- **Comment Status**: D

**Proposed Response**

- The Note about tracking statistics across all 4 decoders is missing from the bin counter.

**Suggested Remedy**

- Add this to the definition of the FEC_codeword_error_bin_i

- "Note that this counter tracks codewords with errors across all four codewords."

**Response Status**: W

**Proposed Accept in Principle**

Implement the suggested remedy with editorial license.

---

**Comment Type**: T

**Comment Status**: D

**Proposed Response**

Annex 175A contains tabular data for an example created by the 1.6TBASE-R PCS TX functions, including the scrambler output, RS-FEC codeword generation, and PCS lane interleaving. The editor’s note on page 539 has a placeholder for a link to a text file that has the machine readable text data. That data file needs to be created.

**Suggested Remedy**

A presentation is planned to submit a data file which corresponds to the Annex 176A example and can be referenced in the editor’s note.

**Proposed Accept in Principle**

IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Has any thought been put into how to calculate the path data delay values (MII-MDI latencies for timestamping) for the SM-PMAs? For bit-mux PMAs, it is very simple - i.e. it is all implementation delay, since the intrinsic delay from bit muxing/demultiplexing is negligible. But at first glance, determining the latency across the Clause 176 PMA looks like more of a challenge.

a. I don't believe that the intrinsic (i.e. non-implementation) delay is deterministic, due to the partial deskew.

b. But apart from the partial deskew, the latency across the SM-PMA should be deterministic using the principles in Annex 90A.7 (max latency value used for Tx path data delay, min latency value used for Rx path data delay).

c. Traditionally, how to calculate the delays through the PHY layers has been an implementation concern, but this is because the calculation was straightforward at lower rates. At 200Gbps lanes, the standard does not have the luxury of being able to ignore this. If it is overly complicated or ambiguous, and opposite ends of a link do not implement it in the same fashion, the system Time Synchronization will be impaired.

Suggested Remedy

Consider a note in Clause 176 (or next to the PMA path data MDIO registers - 45.2.1.176, 45.2.1.177) that the path data delay values for the SM-PMA should be calculated via the method in Annex 90A.7.

I don't think it is necessary, but if a more detailed explanation is deemed useful, then a subclause could be added to Clause 90.7 spelling out explicitly how the path data delay values should be calculated for the SM-PMA.

Proposed Response

PROPOSED REJECT.

It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.

Comment refers to Figure 176.2.

The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols.

The intention is to delay the odd (Tx) and even (Rx) PCSLs by 136 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.

Same apply to Figure 176.9

Suggested Remedy

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 136 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 136 symbols"

Proposed Response

PROPOSED REJECT.

The function in Fig 176-2 uses the words "2 RS-FEC codewords" as opposed to "136 RS-FEC symbols" because the function aims to align the 2 codewords on even lanes with 2 different codewords on odd lanes by delaying odd lanes by 2 codewords. This enables symbol multiplexing across 4 codewords. Same applies to Fig 176-8, 176-11 and 176-13.

While it is not inaccurate to call it a "136 symbol delay", an advantage of using "2 RS-FEC codewords" as opposed to "136 symbols" is that the function name is equally applicable to both 200GE and 400GE SM-PMAs. Moreover, the first line of subclause 176.5.1.3.4 clearly specifies the delay as being 136 RS-FEC symbols, and the subsequent line shows this mathematically as "2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols." Similarly, subclause 176.6.1.2.4 (400GE 16:2 PMA) specifies the delay to be 68 symbols. Hence, the delay value is clearly specified and there is no room for misinterpretation.

The comment proposes an alternate description which is technically correct but does not improve the accuracy or readability of the standard.
Comment Type  | Comment Status | (bucket)  
--- | --- | ---
There is reference in the text to lock process in Figure 119-12. However, there are exceptions to Figure 119-12 as outlined in 176.5.1.6. It can be beneficial to refer to 176.5.1.6 which include both the reference to Figure 119-12 and the list of exceptions list
SuggestedRemedy
Add a reference to 176.5.1.6 instead of Figure 119-12
Proposed Response  | Response Status | W
PROPOSED ACCEPT IN PRINCIPLE.
Add note in parenthesis "(see 176.5.1.6.4)" after Fig 119-12.
Implement with editorial license.

Comment Type  | Comment Status | (bucket)  
--- | --- | ---
There is more details to the AM lock function add a reference
SuggestedRemedy
add a "(see 176.5.1.6.4)" after Table 119-1
Proposed Response  | Response Status | W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #534.
[Editor's note: Changed clause, subclause from 175, 175.5.1.3.1 to 176, 176.5.1.3.1]
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Comment: The sentence "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols)." can be misinterpreted:

Comment Type: TR
Comment Status: D
DelayOddPCSLs (bucket)

136 symbol delay x 4 odd PCS lanes = 544 symbols delay in total (not 2 RS-FEC codewords delay)

Suggested Remedy:
Remove "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols)."

Modify: "Adding the two codeword delay to odd numbered lanes enables the multiplexing of four consecutive RS-FEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."

To: "Adding the 136 symbol delay to odd numbered lanes enables the multiplexing of four consecutive RS-FEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."

Proposed Response: Response Status: W
PROPOSED REJECT.

The first line of subclause 176.5.1.3.4 clearly specifies that the odd lanes are delayed by 136 RS-FEC symbols, and the subsequent line describes mathematically that this (136 symbol delay) is equivalent to adding a delay of 2 codewords to the odd lanes by showing that "2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols". There is little room left for misinterpretation, since the delay in symbols is stated upfront.

Comment: For Figure 176-5, it has to be explained what AÆ/BÆ shall be.

Comment Type: T
Comment Status: D
Figures (bucket)

Suggested Remedy:
Add an explanation for AÆ/BÆ, e.g. "AÆ/BÆ are the symbols from previous 2 CWs that are delayed"

Proposed Response: Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.

Update the text referencing Fig 176-5 (in 176.5.1.3.4) to state that RS-FEC symbols A and A' belong to different codewords from FEC-A, and B and B' belong to different codewords from FEC-B.

Implement with editorial license.

Comment: In Figure 176-6, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols

Comment Type: T
Comment Status: D
Figures (bucket)

Suggested Remedy:
Change the direction of the arrow to follow the actual transmission order.

Proposed Response: Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Update Fig 176-6 to clarify the order of transmission on the output lane, with editorial license.
Is there anything preventing an implementation from performing a full deskew at the Rx PMA? It is not technically required, but does not cause any adverse functional effects. A full deskew at the Rx SM-PMA would NOT change end-to-end latency, since the skew is all ultimately undone at the Rx PCS. A deskew upstream would simply offload the deskew from the Rx PCS.

Implementations with a SM-PMA attached to an RxPCS will undoubtedly perform the Alignment marker lock only once (not once in the PMA and again in the PCS). AM-lock plus deskew is a very natural coupling of functions.

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):
After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before would not have and adverse functional effects.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):
After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before would not have and adverse functional effects.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Figure 119-12 uses functions and variables defined in CL119 but those aren't called out to be used, just that restart_lock_mux is used to replace restart_lock

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):
After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before would not have and adverse functional effects.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Counter _done needs to be at the end of the counter name.

Counter _done needs to be at the end of the counter name.

Counter _done needs to be at the end of the counter name.

Should there be an arc from ALIGNMENT_FAIL to LOSS_OF_ALIGNMENT?

If so, add the arc
The comment refers to Figure 176û11. The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols. The intention is to delay the odd (Tx) and even (Rx) PCSLs by 68 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs. Same apply to Figure 176û13.

**Suggested Remedy**

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 68 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 68 symbols".

**Proposed Response**

PROPOSED REJECT.

Resolve using the response to comment #533.

---

In Figure 176û12, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols.

**Suggested Remedy**

Change the direction of the arrow to follow the actual transmission order.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

---

In Figure 176-16 and Figure 176-17, the symbol pattern of the even PCSLs in the upper half (PCSL 16-31) is not shown. It would be easier to see the RS symbol patterns if the figures included at least one even PCSL in the range of 16-31.

**Suggested Remedy**

These two figures show PCSLs for lanes 0.1, 0.31. Suggest to show the PCSL symbol pattern for lanes 0.1,15, 16, 17,31.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

---

The 800GBASE-R PCS has 4 FEC engines, so figures 176û16, 176û17, 176û18 should use C,D to illustrate the symbols on PCSLs 16-31, rather than A',B'. The A',B' notation is used in 200GBASE-R and 400GBASE-R figures to denote CWs from engines A and B but with the 2CW delay.

**Suggested Remedy**

Amend Figures 176û16, 176û17, 176û18 to avoid the A',B' notation.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Clause 176 avoids using "C" or "D" for 800GBASE-R PMAs because Clause 172 (800GBASE-R PCS) does not use FEC-C and FEC-D. Whereas, "C" and "D" are used in 1.6TBASE-R PMAs because Clause 175 (1.6TBASE-R PCS) uses FEC-C and FEC-D. However, the clarity of the draft will be improved by defining what A, B, A', B' are in the figures Fig 176-16, 176-17 and 176-18. Therefore, implement the following:

Update the text referencing figures Fig 176-16, Fig 176-17 and 176-18 (in 176.7.1.2) to state the RS-FEC symbols A and B are from FEC-A and FEC-B in flow 0 of the 800GBASE-R PCS, while the RS-FEC symbols A' and B' are from flow 1 of the 800GBASE-R PCS.

Implement with editorial license.
In all Figures in the 800G PMA section, it is referred to AÆ/BÆ symbols, although we have 4 RS CWs.

**Suggested Remedy**

Change to use A, B, C, D for the 4 RS CWs, instead of A, B, AÆ, BÆ

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment # 593

---

In Figure 176-18, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols.

**Suggested Remedy**

Change the direction of the arrow to follow the actual transmission order.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Update Figure 176-18 to clarify the order of transmission on the output lane, with editorial license.

---

The first 'shall' statement in Annex 176A (normative) 'Control function and start-up protocol for electrical interfaces' is in 176A.2.3.1 'PRBS13 function'. It seems, however, that there should be 'shall' statements in relation to the entire Training frame structure.

**Suggested Remedy**

1. In subclause 176A.2.1, change 'The training frame marker is a run ...' to read 'The training frame marker shall be a run ...'.
2. In subclause 176A.2.2, change 'The control field comprises ...' to read 'The control field shall be comprised of ...'.
3. In subclause 176A.2.2, change 'The status field comprises ...' to read 'The status field shall be comprised of ...'.
4. In subclause 176A.2.3, change 'The training pattern is the result of a ...' to read 'The training pattern shall be the result of a ...'.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

---

The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0)

Some interfaces have 8 lanes.

The default mapping provided in Table 176A.1 can be used instead.

**Suggested Remedy**

Change to "The default identifier for each lane is the same as that of the PRBS13 function, as shown in Table 176A-1".

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Change: "The default identifier for each lane is its lane number"

To: "The default identifier for each lane is the same as that shown in Table 176A-1"
The PRBS gen should "stop" if training stops.

Suggested Remedy
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

Proposed Response
Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

The PRBS gen should "stop" if training stops.

Suggested Remedy
Add "while training is in progress while this mode is selected" after "is not stopped or reset".

Proposed Response
Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

The initial condition request bits are used to select one of the five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses.

Suggested Remedy
Remove the specificity of how many presets there are.

Proposed Response
Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "The initial condition request bits are used to select one of the five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses." to: "The initial condition request bits are used to select one of up to five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses."

You have self generated data you're sending but you don't have your self setup to send mission data yet.

Suggested Remedy
Remove the "No data is available." from the option 1 of Extend training bit

Proposed Response
Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.
<table>
<thead>
<tr>
<th>Cl</th>
<th>176A</th>
<th>SC 176A.4.3</th>
<th>P556</th>
<th>L4</th>
<th>#574</th>
</tr>
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<tbody>
<tr>
<td>Law, David</td>
<td>HPE</td>
<td><strong>Comment Type</strong>: T</td>
<td><strong>Comment Status</strong>: D</td>
<td><strong>ILT Frame (Bucket)</strong></td>
<td></td>
</tr>
</tbody>
</table>

176A.4.3 'Receiver frame lock' says that 'When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 176A.10 are met ...'. It then goes on to say 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.'.

176A.10 is 'Variables, functions, timers, counters, and state diagrams', so I wonder if the reference should be to 176A.8 'Handshake timing'? In addition, I don't believe the variables training and local_tf_lock are conditioned on the response time requirements specified in 176A.10 being met, at least I didn't see it in their descriptions.

**Suggested Remedy**
In 176A.4.3 change the text '... response time requirements specified in 176A.10 are met.' to read '... response time requirements specified in 176A.8 are met.' and the text '... and is not set to 1 until training and local_tf_lock are both true.' To read '... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.10 can be met.'

**Proposed Response**
Proposed ACCEPT IN PRINCIPLE.

<table>
<thead>
<tr>
<th>Cl</th>
<th>176A</th>
<th>SC 176A.4.8</th>
<th>P556</th>
<th>L37</th>
<th>#576</th>
</tr>
</thead>
<tbody>
<tr>
<td>Law, David</td>
<td>HPE</td>
<td><strong>Comment Type</strong>: T</td>
<td><strong>Comment Status</strong>: D</td>
<td><strong>ILT Frame (Bucket)</strong></td>
<td></td>
</tr>
</tbody>
</table>

176A.4.8 'Coefficient status' says 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' While it is correct that the coef_sts variable is updated by the UPDATE_C(k) function in 176A.6.3, I believe the OUT_OF_SYNC, NEW_INDEX, and WAIT states of the Coefficient update state diagram also update the coef_sts variable. Further, 176A.10.3.2 says that the ENCODE_STS function 'Encodes portions of the status field of transmitted training frames.' and that '... coef_sts is mapped to the coefficient status bits ...'.

**Suggested Remedy**
Since calls of the UPDATE_C(k) function and direct updates of the coef_sts variable all occur in the Coefficient update state diagram, suggest that 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' in 176A.4.8 should be changed to just read 'The acknowledge reflects the value of coef_sts generated by the Coefficient update state diagram'.

**Proposed Response**
Proposed ACCEPT IN PRINCIPLE.
This comment appears to address the same concern expressed in comment #564. Resolve using the response to comment #564.

<table>
<thead>
<tr>
<th>Cl</th>
<th>176A</th>
<th>SC 176A.4.8</th>
<th>P556</th>
<th>L37</th>
<th>#564</th>
</tr>
</thead>
<tbody>
<tr>
<td>Law, David</td>
<td>HPE</td>
<td><strong>Comment Type</strong>: T</td>
<td><strong>Comment Status</strong>: D</td>
<td><strong>ILT Frame (Bucket)</strong></td>
<td></td>
</tr>
</tbody>
</table>

176A.4.8 'Coefficient status' says 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' I don't see a procedure that sets coef_sts in 176A.6.3, but there is one in 176A.6.4. With that said, is it correct that it is just this procedure that sets coef_sts? On review of Figure 176A09 'Coefficient update state diagram', I see it directly sets coef_sts to 'not_upd' in the OUT_OF_SYNC state and indirectly sets coef_sts using the procedure described in 176A.6.4 through calls to the UPDATE_C(k) function in the NEW_REQUEST state. This seems to be confirmed by the first paragraph of 176A.6.4 which says 'The handling of incoming requests is specified by the coefficient update state diagram (Figure 176A09). The behavior of the UPDATE_C(k) function shall be consistent with the following algorithm.'.

**Suggested Remedy**
Change 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' to read 'The coefficient status bits reflect the value of coef_sts variable generated by the coefficient update state diagram (Figure 176A09)'.

**Proposed Response**
Proposed ACCEPT.
When the interface control state diagram (Figure 176A-6) is in the TRAIN_LOCAL state, the device may request its link partner to...

It is important to also note at which states requests from the link partner should be processed, and what happens in the other states - this may not be obvious.

Suggested Remedy

Insert the following paragraphs after the first one:

When the interface control state diagram is in either the TRAIN_LOCAL or TRAIN_REMOTE state, the device shall respond to requests received from the link partner.

When the interface control state diagram is in any state other than TRAIN_LOCAL or TRAIN_REMOTE, the device shall not send any requests to the link partner and shall ignore requests from the link partner.

Proposed Response Response Status W
PROPOSED ACCEPT.

PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add the local_pattern option to the data selector.
Add a Local pattern box as an input to the data selector.
The arrow pointing to the Interface A 'Driver' block and arrow pointing from the Interface B 'CDR' block both seem to be pointing in the wrong direction.

**Suggested Remedy**
Reverse the direction of both arrows.

**Proposed Response**
PROPOSED ACCEPT.

Subclause 176A.10.1 'State diagram conventions' says that 'The notation used in the state diagrams follows the conventions of 21.5.', however subclause 21.5 does not address the operation of timers.

**Suggested Remedy**
Suggest that the text 'All timers operate in the manner described in 14.2.3.2.' be inserted as the new second sentence of the second paragraph of subclause 176A.10.1.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.
Insert the text from clause 136.8.11.7.5: "State diagram timers follow the conventions of 14.2.3.2." as the new second sentence of the second paragraph of subclause 176A.10.1.

**tx_disable** is a per lane variable.

Implement the following with editorial license.
Move the definition of tx_disable to 176A.10.3.
Change the first sentence of the definition from: "Boolean variable that controls the transmitter's output on the interface." to: "Boolean variable that controls the transmitter's output on the lane."
Suggested Remedy

[1] Add 'When it is false, tx_mode controls the content of the transmitter's output on the interface.' or 'When it is false, tx_mode controls the content of the transmitter's output on all lanes of the interface.' depending on the response to my other comment, to the end of the tx_disable variable description.

[2] Change the text ‘... of the interface.’ in the first sentence of the tx_mode variable description to read ‘... of the interface when tx_disable is false.’.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Add the following sentence at the end of the tx_disable definition:

"When it is false, tx_mode controls the content of the transmitter's output on the lane."

Move the definition of tx_mode to 176A.10.3.1 and change the definition of tx_mode... from: "Enumerated variable that controls the content of the transmitter's output of the interface." to: "Enumerated variable that controls the content of the transmitter's output of the lane when tx_disable is false."

Suggested Remedy

The description of the local_tf_lock variable in 176A.10.3.1 says that 'The value of this variable is encoded as the "training lock" bit in the status field of transmitted training frames.', however, there isn’t a "training lock" bit defined for the training frames. Since 176A.4.3 'Receiver frame lock' says 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.' it seems that local_tf_lock is encoded in the 'Receiver frame lock' bit.

Proposed Response  Response Status  W
PROPOSED ACCEPT.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Comment Type: T  Comment Status: D  ILT Diagrams (Bucket)

There should be an underscore between the timer name and 'done'.

SuggestedRemedy

'Suggest that 'recovery_timer done' should be changed to read 'recovery_timer done'.'

Proposed Response  Response Status: W  PROPOSED ACCEPT.

Comment Type: T  Comment Status: D  ILT Diagrams (Bucket)

The WAIT_ADJACENT to SWITCH_CLOCK transition condition uses the variable

mr_training_enabled, however subclause 176A.10.2.1 'Variables' defines the variable

mr_training_enable, not mr_training_enabled.

SuggestedRemedy

'Change the transition condition ' (!mr_training_enabled + segment_ready) * ...' to read ' (!mr_training_enable + segment_ready) * ...'.'

Proposed Response  Response Status: W  PROPOSED ACCEPT.

Comment Type: T  Comment Status: D  ILT Diagrams (Bucket)

C2C loss is TBD

SuggestedRemedy

'Assuming 28 dB budget and package A length ~300 mm and ~125 mm for package B

Proposed Response  Response Status: W  PROPOSED REJECT.

The comment addresses an open TBD, but the suggested remedy is unclear.

Also, the suggested remedy assumes the budget is 28 dB, but consensus on that has not been shown.

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Clause, Subclause, page, line
<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.3</th>
<th>P 597</th>
<th>L 33</th>
<th># 423</th>
</tr>
</thead>
</table>
| Li, Tobey | MediaTek | **Comment Type**: TR **Comment Status**: D **(bucket)**  
Signaling rate of 106.255 ± 50 ppm in Table 176D-1 is incorrect  
**Suggested Remedy**: Change "106.255 ± 50 ppm" to "106.25 ± 50 ppm" **Response Status**: W  
PROPOSED ACCEPT IN PRINCIPLE. Resolve using the response to comment #361. |

<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.4.4</th>
<th>P 603</th>
<th>L 30</th>
<th># 426</th>
</tr>
</thead>
</table>
| Li, Tobey | MediaTek | **Comment Type**: TR **Comment Status**: D **(bucket)**  
"Insertion loss at 26.5625 GHz" in Nyquest frequency in Table 176D-4 is incorrect  
**Suggested Remedy**: Change "26.5625 GHz" to "53.125 GHz" **Response Status**: W  
PROPOSED ACCEPT. |

<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.4.4</th>
<th>P 603</th>
<th>L 31</th>
<th># 451</th>
</tr>
</thead>
</table>
| Healey, Adam | Broadcom Inc. | **Comment Type**: T **Comment Status**: D **(bucket)**  
Typo.  
**Suggested Remedy**: Change "106.255" to "106.25". **Response Status**: W  
PROPOSED ACCEPT. |

<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.4.5</th>
<th>P 604</th>
<th>L 1</th>
<th># 428</th>
</tr>
</thead>
</table>
| Li, Tobey | MediaTek | **Comment Type**: TR **Comment Status**: D **(bucket)**  
Reference to ERL methodology is missing  
**Suggested Remedy**: Add reference to 176D.4.3. **Response Status**: W  
PROPOSED ACCEPT. |

<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.4.5</th>
<th>P 604</th>
<th>L 1</th>
<th># 428</th>
</tr>
</thead>
</table>
| Simms, William | NVIDIA | **Comment Type**: TR **Comment Status**: D **(bucket)**  
Moot point maybe given table is all TBD, but the frequency should be 53.125GHz  
**Suggested Remedy**: change to 53.125GHz **Response Status**: W  
PROPOSED ACCEPT IN PRINCIPLE. Resolve using the response to comment #426. |

<table>
<thead>
<tr>
<th>Cl 176D</th>
<th>SC 176D.3.4.5</th>
<th>P 604</th>
<th>L 1</th>
<th># 428</th>
</tr>
</thead>
</table>
| Li, Tobey | MediaTek | **Comment Type**: TR **Comment Status**: D **(bucket)**  
Reference to test procedure is missing  
**Suggested Remedy**: Add reference to 176D.3.4.4 **Response Status**: W  
PROPOSED ACCEPT. |
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type** TR | **Comment Status** D | TR | **Suggested Remedy**
--- | --- | --- | ---
Table reference is missing. | Add reference of ERL to 176D.4.3. | Add reference of differential-mode to common-mode return loss to 176D.4.4.

**Proposed Response** PROPOSED ACCEPT.

**Comment Type** T | **Comment Status** D | T | **Suggested Remedy**
--- | --- | --- | ---
In "Table 176D.6" class A package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Proposed Response** PROPOSED ACCEPT IN PRINCIPLE.

**Comment Type** T | **Comment Status** D | T | **Suggested Remedy**
--- | --- | --- | ---
The note "The electrical specifications of C2C components are not equivalent to those of the corresponding PMD's. Specifically the test points at which module compliance is defined are different isn't helpful. What does "not equivalent" mean?. Which corresponding PMD's? Although the module test points are different those for the host are the same as Clause 179.

**Proposed Response** Delete the note.

**Comment Type** T | **Comment Status** D | T | **Suggested Remedy**
--- | --- | --- | ---
In "Table 176D.6" class B package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Proposed Response** PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #118.

**Comment Type** T | **Comment Status** D | T | **Suggested Remedy**
--- | --- | --- | ---
In "Table 176D.6" class B package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Proposed Response** PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #118.

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn
SORT ORDER: Clause, Subclause, page, line
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Comment Type T  Comment Status D  Channel ILdd (bucket)

Figure depicts loss should be bump-bump

Suggested Remedy

...application and the associated ILdd bump-bump budget at 53.125 GHz
To make it more clear Host C2M Component should be changed to Host C2M Device and Module C2M Device

Proposed Response

PROPOSED ACCEP IN PRINCIPLE.
The C2M loss budget is currently TBD, but it is expected that it will be inclusive of packages.
However, the suggested remedy does not significantly clarify this fact.
It is preferable to align the diagram with Figure 179-2, where the paths between TP0d and TP1 and between TP4 and TP5d are shown to include the package.
In figure 176E-2, change "Host ILdd" to "Host package and PCB ILdd", and "Module ILdd" to "Module package and PCB ILdd".

Comment Type T  Comment Status D  Channel ILdd (bucket)

Loss is TBD

Suggested Remedy

See Ghiasi C2M May-24 Contribution for background on the numbers
Bump-bump Insertion loss at Nyquist frequency (53.125 GHz) is less than or equal to 28 dB

Proposed Response

PROPOSED REJECT.
The loss in the text is TBD because equation 176E-3 has TBDs. When an equation is provided, the text can be changed accordingly, but the commend does not propose values for the equation.
The following presentation was reviewed by the task force in the May 2024 interim meeting: https://www.ieee802.org/3/dj/public/24_05/ghiasi_3dj_02_2405.pdf
The presentation does not include a proposa equation 176E-3.

[Editor's note: changed page from 621 to 632]

Comment Type TR  Comment Status D  Channel ILdd (bucket)

"within the time interval t_s +/-0.05 UI and with accumulated probability for each sample weighted by the function w(t) defined by Equation (176E-4)": this makes the measurement too tolerant to jitter.

Suggested Remedy

Remove the Gaussian weighting function w(t), increase +/-0.05 to +/-0.07, same as TDECQ. This will make VEC look worse, but will be a better measurement to protect the link. Use this method for CR also, with "software channel" ("far end eye measurement") as appropriate.

Proposed Response

PROPOSED REJECT.
The comment does not provide sufficient justification to support the suggested remedy. The suggested remedy does not provide sufficient detail to implement.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Cl 177 SC 177.1.3 P249 L10 # 81
Huber, Thomas  
Comments Type T  
Comment Status D (bucket)

The second bullet could be written more clearly

Suggested Remedy
Revise to read “Distributing (collecting) the convolutional interleaved data to (from) eight Inner FEC flows

Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 177 SC 177.1.3 P249 L14 # 82
Huber, Thomas  
Comments Type T  
Comment Status D (bucket)

The fifth bullet could be written more clearly

Suggested Remedy
Revise to read “8:1 interleaving (1:8 deinterleaving) the eight Inner FEC flows to (from) a single flow”

Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 177 SC 177.14 P250 L32 # 543
Rechtman, Zvi  
Comments Type T  
Comment Status D (bucket)

PAM4 decoding (bucket)

The comment refers to Figure 177.2.
There is a footnote that PAM4 decoding is optional in case of soft decoding. However, the DataPath is defined using bit streams, also the FEC:IS_UNITDATA_i.indication primitives has two value of 0 or 1, therefore PAM4 decoding must to take place

Suggested Remedy
Either remove the footnote, or elaborate on the intention of this footnote.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 83.

Cl 177 SC 177.4.1 P251 L36 # 505
de Koos, Andras  
Comments Type T  
Comment Status D (bucket)

timesync (bucket)

Due primarily to the convolutional interleaver/deinterleaver, there is a large variation in the input-to-output latency of the Inner FEC sublayer. As such, there is concern that the method to properly calculate the path data delay for the Inner FEC sublayer should be explained in Clause 90, similarly to what is done for the variation from FEC codewords and PCS-lane distribution in clause 90.7.1.

Suggested Remedy
Do nothing.
Using the general method in Clause 90A, allocating the maximum value of the intrinsic delay to the transmit PHY and the minimum value of the intrinsic delay to the receive PHY, there is no ambiguity.
So it should not be necessary to add to Clause 90 for every new PHY type. The principles laid out in Annex 90A.7 should apply.
If anything, a general note could be added in Clause 177 (in Clause 45 with the MDIO registers for path data delay values) explaining that the Tx/Rx path data delay values should be calculated following the guidelines in Annex 90A.7, where the maximum latency value is used for the Tx path data delay, and the minimum latency value is used for Rx path data delay.

Proposed Response Response Status W
PROPOSED REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy. It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

Page 34 of 57 5/30/2024 4:14:18 PM
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment Type:** T  **Comment Status:** D  **Cl (bucket):**

"The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay" is correct only if the Q values are 544/272/136/68 for 200G/400G/800G/1.6T. However, the Q values should be 192/96/48/24 as shown in slides 6-11 of he_3dj_01_2307 for 200G/400G/800G/1.6TbE.

**Suggested Remedy:**
Suggest to modify Line 50-51 in page 251 as follows:
The convolutional interleaver is composed of three parallel delay lines (numbered 0 to 2), as illustrated in Figure 177-3. Each delay operator ôDö represents a storage element of 40 bits. From one delay line to the next higher delay line, Q delay operators are deleted. Modify the Q values to 192/96/48/24 for 200G/400G/800G/1.6T.

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

---

**Comment Type:** TR  **Comment Status:** D  **Cl (bucket):**

The values of Q and the description of the Convolutional interleaver functionality doesnÆt match the adopted values in he_3dj_01_2307.pdf. The values should be:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

**Suggested Remedy:**
Modify the Q values to: 200G BASE-R: Q = 192 400G BASE-R: Q = 96 800G BASE-R: Q = 48 1.6T BASE-R: Q = 24

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

---

**Comment Type:** TR  **Comment Status:** D  **Cl (bucket):**

According to the adopted baseline, change the Q values as follows:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

**Response Status:** W

---

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

---

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.
Cl 177 SC 177.4.1 P 252 L 19 # 388
Slavick, Jeff Broadcom

Comment Type T Comment Status D CI (bucket)
The delay line for Cl177 starts with feeding data into the longest delay line while Cl184 sends it to the delay line with the shortest delay.

SuggestedRemedy
Change Cl177 to have the Delay Line 0 be the minimal delay and the Delay Line 2 to be the longest delay.

Proposed Response Response Status W
PROPOSED REJECT.
This is consistent with the adopted baseline. It is correct as documented.

Cl 177 SC 177.4.1 P 256 L 50 # 545
Rechtman, Zvi Nvidia

Comment Type TR Comment Status D CI - Editorial (bucket)
The description in "The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay" seems to represent block interleave and not convolutional interleave.

SuggestedRemedy
Modify to:
"The convolutional interleaver is composed of 3 delay lines.
For 200GBASE-R the first line (line0) delays the PHYs data by 4x2x192 = 1,536 RS-FEC symbols, the second line (line1) by 4x1x192 = 768 RS-FEC symbols and the last line (line3) adds no delay.
For 400GBASE-R the first line (line0) delays the PHYs data by 4x2x96 = 768 RS-FEC Symbols, the second line (line1) by 4x1x96 = 384 RS-FEC symbols and the last line (line3) adds no delay.
For 800GBASE-R the first line (line0) delays the PHYs data by 4x2x48 = 384 RS-FEC Symbols, the second line (line1) by 4x1x48 = 192 RS-FEC symbols and the last line (line3) adds no delay.
For 1.6TBASE-R the first line (line0) delays the PHYs data by 4x2x24 = 192 RS-FEC Symbols, the second line (line1) by 4x1x24 = 96 RS-FEC symbols and the last line (line3) adds no delay.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.
I'm not convinced that the circular shift really adds any robustness. Yes, it distances bit-pairs belonging to the same RS-FEC codeword, but without the shift, the consecutive bit pairs (after 8:1 multiplexing) belonging to the same RS-FEC code words would each protected by different Inner FEC code words, would they not?

So is the circular shift just protecting against uncorrected inner-FEC codewords that would all land on the same RS-FEC codeword? Seems overkill. Are there simulations/models showing the benefit of including circular shift?

Suggested Remedy
Consider removing the circular shift if it does not offer any worthwhile benefit.

PROPOSED REJECT.
This is consistent with the baseline adopted. The comment does not provide sufficient justification to support the suggested remedy.

The systematic Hamming code is most naturally defined in terms of its parity-check matrix, as pointed out in many textbooks and standard documents. One famous example is the systematic double-extended Hamming(128,119) code in OIF-400ZR and ITU-T G.709.3.

Suggested Remedy
Suggest to include the construction process and parity-check matrix of the adopted Hamming(68,60) code to enhance the completeness of the document. A Supporting Presentation will be provided.

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

A figure illustrating the pad bits and their interval for each inner FEC flow would be useful. I always find myself referring to the equivalent RS-FEC Figures (Figure 119-6 and Figure 119-8).

Suggested Remedy
Consider adding a figure illustrating the pad insertion and interval, in the same style as Figure 119-6.

PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment Status:** D
**Response Status:** W

**Comment:** Phase of inner FEC pad bits vs outer FEC parity bits:
- An inaccuracy in the path data delay of up to 12ps due to arbitrary phase between the output FEC parity bits and the inner FEC pad bits of the phase is not accounted for.
- This arbitrary phase would affect the path data delay values.
- Almost negligible, if my math is correct.

**Suggested Remedy:**
3 possible ways to address:

a. Impose a phase relationship between the RS FEC code word boundaries and the inner FEC pad bits, which would mean large-scale changes to the draft.
b. Specify (in clause 90, perhaps) that the path data delay contribution through the inner FEC sublayer shall be strictly additive to the path data delay contribution through the PCS and PMA layers.
c. Ignore. Based on 90A.7, the effect here is small enough to not address specifically.

"Whether the potential delay difference between the aggregated delay and the sum of the individual function delays is small enough to satisfy the timing requirements is up to the individual application."

I prefer option (c). It should not be necessary to add specific text or impose new logical rules to the Inner FEC pad bits to address a potential 12ps path data delay impairment.

**Proposed Response:** PROPOSED REJECT.

The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01a_2405.pdf

It appeared that there was no consensus to make any related changes to the draft.

**Comment:** It is not declared when the first pad insertion should happen.

**Suggested Remedy:** Indicate in the text that the first pad insertion will happen right at the beginning of CWs, same as in the test vectors.

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.

**Comment:** The details of how to use the IBSF are beyond the scope of this standard. Does it mean this is vendor discretionary? Or will it be defined in other standard?

**Suggested Remedy:** Clarify in the text where the use of the IBSF will be defined.

**Proposed Response:** PROPOSED ACCEPT IN PRINCIPLE.
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type:** T  **Comment Status:** D  **Inner FEC Sync (bucket)**

This subclause is confusing and seems to be prescribing a specific implementation. The goal of the process is to find codeword boundaries and remove the pad. If we simply reverse the processes of the tx, this process would (in a logical sense) be performed on the interleaved stream, and would search for the (interelaved) FS pattern.

**Suggested Remedy:**
Rewrite the text to describe searching for the FS pattern and finding it at the expected interval.

**Proposed Response**  **Response Status:** W
PROPOSED REJECT.
The comment does not provide sufficient justification to support the suggested remedy.
The existing text is consistent with the adopted baseline.

**Comment Type:** T  **Comment Status:** D  **Inner FEC Sync (bucket)**

Monitor and drop says you monitor on all flows. But Figure 177-7 is a per flow state diagram. So is each Flow checking for 140 bad out of 150? And 150 is not a multiple of 8 for it to span across all flows evenly.

**Suggested Remedy:**
Change:
"keeps monitoring 150 consecutive codewords on all flows, if at least 140 codewords are invalid, drop sync and restart from step a)."

To:
"each flow counts the number of invalid codewords seen in consecutive non-overlapping 150 codeword windows, if at least 140 codewords are invalid, drop sync and restart from step a)."

**Proposed Response**  **Response Status:** W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

**Comment Type:** T  **Comment Status:** D  **counters (bucket)**

177.5.3 lists a few counter to be supported by the inner FEC. The defintion for some of these could be improved. Further, additional counters should be included provides bins of error counts to help estimate quality of the link.

**Suggested Remedy:**
A contribution with more details will be provided.

**Proposed Response**  **Response Status:** W
PROPOSED ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting: https://www.ieee802.org/3/dj/public/24_05/brown_3dj_05a_2405.pdf.
Implement slides 7, 9 and 10 with editorial license.
Comment Type: T
Comment Status: D
Inner FEC decode (bucket)

Defining how a miscorrected codeword can occur could be phrased more clearly.

**Suggested Remedy**

Change:

ôNote that for soft-decision decoded Inner FEC codewords, when there is more than one bit error in a codeword, there is always a non-zero chance that miscorrection could happen.ô

To:

ôNote that when there is more than one bit error in a codeword there is a chance that the soft decision decoder could miscorrect the codeword.ô

**Proposed Response**

Implement the suggested remedy with editorial license.

---

Comment Type: T
Comment Status: D
Inner FEC Sync (bucket)

Counters defined here do not seem consistent with those defined in Table 177-4.

**Suggested Remedy**

Please make definitions of counters consistent with status variables shown on Table 177-4, page 263

**Proposed Response**

Resolve using the response to comment # 183.

---

Annex title unnecessarily uses the acronym IMDD. Not clear what purpose is achieved that cannot be achieved simply by omitting the use of the acronym IMDD.

**Suggested Remedy**

Delete the acronym IMDD.

**Proposed Response**

Resolve using the response to comment # 183.

---

The Annex 176A control function is required and should be included in Table 178-1 (as is done in Table 179-1).

**Suggested Remedy**

Add “176A - Control” as “Required” in Tables 178-1, 178-2, 178-3, and 178-4.

**Proposed Response**

Implement the suggested remedy with editorial license.
<table>
<thead>
<tr>
<th>Cl 178</th>
<th>SC 178.9</th>
<th>P275</th>
<th>L33</th>
<th># 363</th>
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<td>Healey, Adam</td>
<td>Broadcom Inc.</td>
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<tr>
<td>Comment Type</td>
<td>T</td>
<td>Comment Status</td>
<td>D</td>
<td>(bucket)</td>
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<tr>
<td>The reference to 179.8.9 seems inappropriate here since that subclause contains cross-references specific to the Clause 179.</td>
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<tr>
<td>Replicate the content of 179.8.9 here, replacing references to Clause 179 electrical requirements to the corresponding references in Clause 178.</td>
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<td>Implement the suggested remedy with editorial license.</td>
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<th>P276</th>
<th>L18</th>
<th># 452</th>
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<td>Simms, William</td>
<td>NVIDIA</td>
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<td>Comment Status</td>
<td>D</td>
<td>TX AC CM (bucket)</td>
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<tr>
<td>SCMR may need to be relaxed for 200Gb/s. Measure of 15dB full band at TP0v given full band Vcm noise of 80mVpp at TP2.</td>
<td></td>
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<tr>
<td>SuggestedRemedy</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Likely need to tighten 80mV Vcm in table 179-7 for 200Gb/s</td>
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<tr>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
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<td></td>
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<tr>
<td>PROPOSED REJECT.</td>
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<tr>
<td>The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not a valid request.</td>
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<table>
<thead>
<tr>
<th>Cl 178</th>
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<th>P282</th>
<th>L45</th>
<th># 401</th>
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<tr>
<td>Li, Tobey</td>
<td>MediaTek</td>
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<td>Comment Type</td>
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<td>Comment Status</td>
<td>D</td>
<td>RX ITOL/JTOL (bucket)</td>
</tr>
<tr>
<td>&quot;The test channel COM, calculated per items 3) through 7) in 93C.2, is at least 3 dB&quot;</td>
<td></td>
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</tr>
<tr>
<td>The reference to the test channel COM is wrong.</td>
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<tr>
<td>SuggestedRemedy</td>
<td></td>
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</tr>
<tr>
<td>Change it to &quot;The test channel COM, calculated peritem e) through h)&quot; in 178.9.3.3, is at least 3 dB&quot; to be correct</td>
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<tr>
<td>Proposed Response</td>
<td>Response Status</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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<tr>
<td>Implement the suggested remedy with editorial license.</td>
<td></td>
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<table>
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<tr>
<th>Cl 178</th>
<th>SC 178.10</th>
<th>P284</th>
<th>L12</th>
<th># 118</th>
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<tr>
<td>Mellitz, Richard</td>
<td>Samtec</td>
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<td></td>
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<td>Comment Type</td>
<td>TR</td>
<td>Comment Status</td>
<td>D</td>
<td>Channel ILdD (bucket)</td>
</tr>
<tr>
<td>reference is wrong and IldD should reflect tp0d to tp05d.</td>
<td></td>
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<tr>
<td>SuggestedRemedy</td>
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<tr>
<td>change reference to 178.10.2 and TBD to 40 dB or eliminate the reference to IldD</td>
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<tr>
<td>Proposed Response</td>
<td>Response Status</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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</tr>
<tr>
<td>The objective this clause is addressing is 40 dB die-to-die. Change the reference to 178.10.2 and the TBD to 40 dB with additional text to state that it is specified from TP0d to TP5d.</td>
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<tr>
<td>Implement with editorial license.</td>
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<table>
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<tr>
<th>Cl 178</th>
<th>SC 178.10.1</th>
<th>P285</th>
<th>L18</th>
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<tbody>
<tr>
<td>Sakai, Toshiaki</td>
<td>Socionext</td>
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<tr>
<td>Comment Type</td>
<td>T</td>
<td>Comment Status</td>
<td>D</td>
<td>COM pkg tau (bucket)</td>
</tr>
<tr>
<td>COM reference parameter value. (transmission line parameter tau)</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>In &quot;Table 178D12&quot; class A package model Transmission line parameter τ(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141_e-3. The value should be 6.141e-3 ns/mm.</td>
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<tr>
<td>SuggestedRemedy</td>
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<td></td>
</tr>
<tr>
<td>Change τ(tau) value in Table 178-12 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm. Or simply delete this row, as the τ(tau) value in table 93A-3 is 6.141e-3 ns/mm.</td>
<td></td>
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<tr>
<td>Proposed Response</td>
<td>Response Status</td>
<td>W</td>
<td></td>
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<tr>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
<td></td>
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</tr>
<tr>
<td>The value in D1.0 is a typo. Change 6.141e-4 to 6.141e-3 in Table 178–12, Table 179–15, and Table 178D–6 (twice in each table).</td>
<td></td>
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</tr>
</tbody>
</table>
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Cl 178 SC 178.10.1 P285 L19 # 355
Healey, Adam Broadcom Inc.

Comment Type T Comment Status D COM pkg tau (bucket)

In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

Suggested Remedy
Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl 178 SC 178.10.1 P285 L28 # 356
Sakai, Toshiaki Socionext

Comment Type T Comment Status D COM pkg tau (bucket)

"Table 178u12" class B package model Transmission line parameter (tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, liim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

Suggested Remedy
Change (tau) value in Table 178-12 (class B package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the (tau) value in table 93A-3 is 6.141e-3 ns/mm.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl 178 SC 178.10.1 P285 L31 # 357
Healey, Adam Broadcom Inc.

Comment Type T Comment Status D COM ref pkg (bucket)

In Table 178-12, the transmission line parameters for the "Class B package model" do not match the adopted baseline proposal li_3dj_01a_2311 slide 9.

Suggested Remedy
Replace the characteristic impedance for stage 1 with 92 Ohms, and the length/characteristic impedances for stage 2 through 4 with 70 Ohms/1 mm, 80 Ohm/1 mm, and 100 Ohm/0.5 mm respectively. Similarly in Table 179-15 and Table 176D-6.

Proposed Response Response Status W
PROPOSED ACCEPT.
## IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

<table>
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<tr>
<th>Cl 178A</th>
<th>SC 178A.1.8</th>
<th>P654</th>
<th>L42</th>
<th># 209</th>
<th>Shakiba, Hossein</th>
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<td>D</td>
<td>Reference to the wrong section 178A.1.6.4</td>
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<td></td>
<td>Change reference to section 178A.1.8.1</td>
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<tr>
<th>Cl 178A</th>
<th>SC 178A.1.9</th>
<th>P657</th>
<th>L51</th>
<th># 210</th>
<th>Shakiba, Hossein</th>
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<td>Comment Status</td>
<td>D</td>
<td>Reference to the wrong section 178A.1.6.4</td>
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<tr>
<td>Suggested Remedy</td>
<td></td>
<td></td>
<td></td>
<td>Add a case to define h_ISI(n) = 0 for n = d+1</td>
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</tr>
<tr>
<td>Proposed Response</td>
<td></td>
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<tr>
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<th>SC 178A.1.11.1</th>
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<th>L52</th>
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<th>Huawei Technologies Canada</th>
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<td>D</td>
<td>Reference to the wrong section 178A.1.6.4</td>
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<tr>
<td>Suggested Remedy</td>
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<td></td>
<td></td>
<td>Either mention that after convolution, the result should be normalized, or add a normalization coefficient of 1/(1-b1) in font of conv.</td>
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<tr>
<td>Proposed Response</td>
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<th>L44</th>
<th># 511</th>
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<td>Comment Type</td>
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<td>D</td>
<td>AC common-mode voltages are not as large as this in practice, even at 200G/lane</td>
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<td></td>
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<tr>
<td>Suggested Remedy</td>
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<td>Reduce both AC common-mode voltage limits for CR, KR, C2C and C2M.</td>
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<td>AC common-mode voltages are not as large as this in practice, even at 200G/lane</td>
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<tr>
<td>Suggested Remedy</td>
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<td></td>
<td></td>
<td>Reduce 1200 mV to e.g. 1000 mV, here, in the receiver Table 179-10 and in the text in 179.9.5.2. Reduce the steady-state voltage Vf max from 0.6 V to 0.5 V. Similarly for KR and C2C.</td>
<td></td>
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<tr>
<td>Proposed Response</td>
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<td>PROPOSED REJECT.</td>
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### TYPE: TR/technical required ER/editorial required G/general required T/technical E/editorial G/general
### COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
### SORT ORDER: Clause, Subclause, page, line

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Dawe, Piers | Nvidia |

Dawe, Piers | Nvidia |

Dawe, Piers | Nvidia |

Shakiba, Hossein | Huawei Technologies Canada |

Shakiba, Hossein | Huawei Technologies Canada |

Shakiba, Hossein | Huawei Technologies Canada |

Shakiba, Hossein | Huawei Technologies Canada |

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**Comment Type**
- **T**: technical
- **E**: editorial
- **G**: general

**Comment Status**
- **D**: dispatched
- **A**: accepted
- **R**: rejected

**Response Status**
- **O**: open
- **W**: written
- **C**: closed
- **Z**: withdrawn

**Sort Order**: Clause, Subclause, page, line
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<td>Tx jitter, Tx SNDR (bucket)</td>
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<tr>
<td></td>
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</tr>
<tr>
<td>Our way of measuring jitter doesn't work well enough with the increased max host loss over 3ck. It is not clear that it can or should be fixed. Our way of defining SNDR doesn't work correctly over host loss either. This can be fixed, but &quot;vertical and horizontal noise&quot; act together to degrade BER: more of one goes with less of the other.</td>
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<tr>
<td>SuggestedRemedy</td>
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</tr>
<tr>
<td>Delete the SNDR and jitter specs. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.</td>
<td></td>
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<tr>
<td>PROPOSED REJECT.</td>
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<tr>
<td>The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not valid. In addition, the comment includes a claim that measurements are not feasible, which is not substantiated and is contrasted by existing contributions, e.g. <a href="https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf">https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf</a>.</td>
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<td>Tx jitter, Tx SNDR (bucket)</td>
</tr>
<tr>
<td></td>
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<tr>
<td>As explained in other comments, up to 3ck the SNDR spec acted together with the jitter spec to protect the link performance - but we don't have a satisfactory way of measuring jitter at today's speeds and losses, and separating the two things out &quot;leaves margin on the table&quot;.</td>
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<tr>
<td>SuggestedRemedy</td>
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<tr>
<td>Delete the SNDR section. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.</td>
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<td>PROPOSED REJECT.</td>
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<tr>
<td>The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not valid. In addition, the comment includes a claim that measurements are not feasible, which is not substantiated and is contrasted by existing contributions, e.g. <a href="https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf">https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf</a>.</td>
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<th>P326</th>
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<td>Comment Type</td>
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<td>Nominal impedance (bucket)</td>
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<tr>
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<tr>
<td>Nominal characteristic impedance of the cable assembly is &quot;100-ohm&quot;</td>
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<td>SuggestedRemedy</td>
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<tr>
<td>Contributions to the task force have demonstrated the nominal characteristic impedance of the cable assembly is ~92-ohm</td>
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<tr>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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</tr>
<tr>
<td>It is understood that the suggested remedy is to change the nominal impedance from 100 to 92 Ohm. However, as noted in comment #216, there is no need to specify a nominal impedance. Resolve with using the response to comment #216.</td>
<td></td>
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</table>

Note that the importance of controlling jitter separately from other impairment has been addressed in https://www.ieee802.org/3/dj/public/24_05/ran_3dj_03_2405.pdf.
<table>
<thead>
<tr>
<th>Cl 179</th>
<th>SC 179.11.1</th>
<th>P 326</th>
<th>L 27</th>
<th># 216</th>
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<td>Google</td>
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<td>Comment Status: D</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>Comment: There is no test method or definition for the nominal characteristic impedance of the cable assembly. The components (eg paddle card, twinax) within a cable assembly may have different nominal characteristic impedances. There is no need to specify the nominal characteristic impedance of the cable assembly, since the performance of the cable assembly is determined by cl 179.11.2-7.</td>
<td></td>
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<tr>
<td></td>
<td>Proposed Remedy: Remove &quot;The nominal characteristic impedance of the cable assembly is 100 ohms&quot;</td>
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<td></td>
<td>Proposed Response: Remove &quot;The nominal characteristic impedance of the cable assembly is 100 ohms&quot;</td>
<td>Response Status: W</td>
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<th>L 18</th>
<th># 120</th>
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<td>Sakai, Toshiaki</td>
<td>Socionext</td>
<td>Comment Type: T</td>
<td>COM pkg tau (bucket)</td>
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<td>Comment Status: D</td>
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| | | Comment: COM reference package parameter values. (transmission line parameter tau)
In "Table 179015" class A package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, (llim_3dj_01a_2311.pdf (page8-9), the value is 6.14e-3. The value should be 6.14e-3 ns/mm. |
| | Proposed Remedy: Change t(tau) value in Table 179-15 (class A package) from 6.14e-4 ns/mm to 6.14e-3 ns/mm. 
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.14e-3 ns/mm. |
| | Proposed Response: Change t(tau) value in Table 179-15 (class A package) from 6.14e-4 ns/mm to 6.14e-3 ns/mm. 
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.14e-3 ns/mm. | Response Status: W |
| | | PROPOSED ACCEPT IN PRINCIPLE. |

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<th>Cl 179</th>
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<td></td>
<td></td>
<td>Comment Status: D</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Comment: &quot;Nominal impedance&quot; is something for a datasheet not a spec. If someone wants to build a cable assembly with 95 ohm bulk cable and it passes the spec - that's OK.</td>
<td></td>
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<tr>
<td></td>
<td>Proposed Remedy: Delete &quot;The nominal differential characteristic impedance of the cable assembly is 100 [ohm]&quot;. Move the one remaining sentence into 179.11.</td>
<td></td>
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<tr>
<td></td>
<td>Proposed Response: Delete &quot;The nominal differential characteristic impedance of the cable assembly is 100 [ohm]&quot;. Move the one remaining sentence into 179.11.</td>
<td>Response Status: W</td>
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| | | Comment: COM reference package parameter values. (transmission line parameter tau)
In "Table 179015" class B package model Transmission line parameter t(tau) value is 6.14e-4 ns/mm, but based on the adopted motion#10, Nov/2024, (llim_3dj_01a_2311.pdf (page8-9), the value is 6.14e-3. The value should be 6.14e-3 ns/mm. |
| | Proposed Remedy: Change t(tau) value in Table 179-15 (class B package) from 6.14e-4 ns/mm to 6.14e-3 ns/mm. 
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.14e-3 ns/mm. |
| | Proposed Response: Change t(tau) value in Table 179-15 (class B package) from 6.14e-4 ns/mm to 6.14e-3 ns/mm. 
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.14e-3 ns/mm. | Response Status: W |
| | | PROPOSED ACCEPT IN PRINCIPLE. |

<table>
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<tr>
<th>Cl 179</th>
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<th># 122</th>
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<td>Comment Status: D</td>
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<tr>
<td></td>
<td></td>
<td>Comment: ERL requirement for cable assembly that have COM less than &quot;4dB&quot;</td>
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<tr>
<td></td>
<td>Proposed Remedy: Change &quot;4dB&quot; to &quot;TBD&quot;. Historical precedent may not be relevant for this specification</td>
<td></td>
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<tr>
<td></td>
<td>Proposed Response: PROPOSED REJECT. The comment does not provide sufficient justification to support the suggested remedy. Note that any content of the draft can be changed if there is consensus, but changes from a number to TBD does not move us forward.</td>
<td>Response Status: W</td>
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</table>

**Type:** TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general  
**Comment Status:** D/dispatched  A/accepted  R/rejected  
**Response Status:** O/open  W/written  C/closed  Z/withdrawn  
**Sort Order:** Clause, Subclause, page, line  
**Date:** 5/30/2024 4:14:18 PM
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<th>Comment</th>
<th>Suggested Remedy</th>
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<td>179B</td>
<td>179B</td>
<td>669</td>
<td>17</td>
<td>T</td>
<td>D</td>
<td>HCB and MCB (bucket)</td>
<td>Missing reference to Module compliance at TP1 and TP4</td>
<td>Add <em>Module measurements for Modules specified in Annex 176E are made at TP1 and TP4 with test fixtures as specified in 179B.3.</em></td>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
</tr>
<tr>
<td>179B</td>
<td>179B</td>
<td>676</td>
<td>24</td>
<td>T</td>
<td>D</td>
<td>HCB and MCB (bucket)</td>
<td>SFPxxx is unclear</td>
<td>Replace &quot;The SFPxxx mated test fixture&quot; with &quot;The single-lane mated test fixture&quot;</td>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
</tr>
<tr>
<td>179B</td>
<td>179B</td>
<td>676</td>
<td>26</td>
<td>T</td>
<td>D</td>
<td>HCB and MCB (bucket)</td>
<td>Incorrect Annex reference 120G</td>
<td>Replace 120G with 120E</td>
<td>PROPOSED ACCEPT.</td>
</tr>
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</table>

**Comment Type: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general**

**COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn**

**SORT ORDER: Clause, Subclause, page, line**
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Cl 179C SC 179C.1 P680 L15 # 525
Dawe, Piers Nvidia
Comment Type T Comment Status D MDI references (bucket)
MDIs are mechanical entities. For 106.25 GbD operation, there are SFP2 (SFF-TA-1031) and QSFP2 (SFF-TA-1027). Any "SFP224" would be an SFP2 module or cable end with 200G-capable circuitry. But this annex is for the MDI, not the circuitry. Similarly for "QSFP224" and QSFP2.

SuggestedRemedy
Correct the names. Add references to SFF-TA-1011 which relates the names and specs for the SNIA-SFF modules, and SFF-8665, which defines the components of a QSFPx "solution".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
There was broad consensus to use names of MDI types (part of baseline proposal) currently in the draft as follows: SFP224, SFP-DD224, QSFP224, QSFP-DD1600, OSFP1600.
Resolve using the response to comment #506, which addresses the normative references.

Cl 179C SC 179C.1 P680 L17 # 525
Dawe, Piers Nvidia
Comment Type TR Comment Status D MDI references (bucket)
Refer to the specification for each connector type where each is first mentioned.
See another comment against 1.3 for the reference docs.

SuggestedRemedy
Per comment
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl 179C SC 179C.2.4 P689 L35 # 528
Dawe, Piers Nvidia
Comment Type T Comment Status D MDI references (bucket)
There is no QSFP-DD1600 TBD MSA document. QSFP-DD1600 is defined in the singular QSFP-DD MSA document

SuggestedRemedy
Change "the QSFP-DD1600 TBD MSA" to "the QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl 179C SC 179C.2.5 P690 L21 # 529
Dawe, Piers Nvidia
Comment Type T Comment Status D MDI references (bucket)
There is no OSFP1600 TBD MSA document. OSFP1600 is defined in the singular OSFP MSA document, particularly section 4.

SuggestedRemedy
Change "the OSFP1600 TBD MSA" to "the OSFP Octal Small Form Factor Pluggable Module specification" or "section 4 of the OSFP Octal Small Form Factor Pluggable Module specification".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl 180 SC 180.4.1 P350 L13 # 160
Yu, Rang-chen InnoLight
Comment Type ER Comment Status D Editorial (bucket)
A typo of 'L3' in figure 180-2, right side, 3rd channel output label.

SuggestedRemedy
It should be 'L2'.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

Page 47 of 57
### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

<table>
<thead>
<tr>
<th>Cl 180 SC 180.10</th>
<th>P 368</th>
<th>L 11</th>
<th># 521</th>
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<td>Nvidia</td>
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<tr>
<td>Change 1.9.4 to 1.9.n. Below, change 1.10.4 to 1.10.n. Similarly in other clauses.</td>
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**Proposed Response**

- **Response Status**: W
- **Proposed Accept in Principle.**
- Implement the suggested remedy with editorial license.

<table>
<thead>
<tr>
<th>Cl 181 SC 181.1</th>
<th>P 372</th>
<th>L 16</th>
<th># 4</th>
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<tr>
<td><strong>Suggested Remedy</strong></td>
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<tr>
<td>Shorten the PHY bracket to exclude the MDI layer.</td>
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**Proposed Response**

- **Response Status**: W
- **Proposed Accept in Principle.**
- Implement the suggested remedy with editorial license.

<table>
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<th>P 386</th>
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<tr>
<td><strong>Suggested Remedy</strong></td>
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<tr>
<td>Replace the reference to 121.8.5.2 with reference to 181.8.5.1.</td>
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**Proposed Response**

- **Response Status**: W
- **Proposed Accept in Principle.**
- Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Cl 182 SC 182.1 P 394 L 50 # 304**

Maki, Jeffery

Juniper Networks

**Comment Type TR**

**Comment Status D**

IMDD acronym (bucket)

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of “Coherent” to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

**Suggested Remedy**

Delete the acronym IMDD.

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT.

**Cl 182 SC 182.1 P 395 L 21 # 5**

Johnson, John

Broadcom

**Comment Type T**

**Comment Status D**

Editorial (bucket)

The PHY bracket in Figure 182-1 does not encompass the PMD layer, which isn't consistent with previous PMDs.

**Suggested Remedy**

Lengthen the PHY bracket to include the PMD layer.

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

**Cl 183 SC 183.1 P 418 L 39 # 505**

Maki, Jeffery

Juniper Networks

**Comment Type TR**

**Comment Status D**

IMDD acronym (bucket)

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of “Coherent” to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

**Suggested Remedy**

Delete the acronym IMDD.

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT.

**Cl 184 SC 184.1.1 P 441 L 8 # 808**

Bruckman, Leon

Huawei

**Comment Type TR**

**Comment Status D**

General (Bucket)

The Inner FEC as defined, includes the PMA. Shall make this clear to the reader.

**Suggested Remedy**

Either add sentence: “This Inner FEC sublayer includes functionality often associated with the PMA sublayer”, or split the PMA function

**Proposed Response**

**Response Status W**

PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Add sentence: “This Inner FEC sublayer includes functionality often associated with the PMA sublayer at the PMD service interface”.

Add similar text to the appropriate sub clause in clause 177

[Editor's note: CC 184, 177]

**Cl 184 SC 184.2 P 443 L 7 # 87**

Huber, Thomas

Nokia

**Comment Type T**

**Comment Status D**

General (Bucket)

Other diagrams of this type do not have dashed boxes around the transmit and received processes.

**Suggested Remedy**

For consistency with the rest of the document, remove the dashed boxes

**Proposed Response**

**Response Status W**

PROPOSED REJECT.

The dashed boxes clearly denote the transmit and receive functions. Removing the dashed boxes does not improve clarity of the draft.
### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

#### 184.2 Functional (Bucket)

**Comment**
The second sentence of the paragraph (discussing the distribution to 32 lanes by the permutation function) seems to imply that the 32 lanes were interleaved into a serial stream after they were reordered and deskewed, but the text doesn’t actually say that is done.

**Suggested Remedy**
If the intent is that the 32 lanes are re-interleaved, and then the permutation function distributes the symbols back to 32 lanes (in something other than a round-robin manner), change the end of the first sentence to say “are ordered, deskewed, and serialized”. If the intent is that the permutation process just moves symbols around among the 32 lanes, change the second sentence to say "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function."

**Proposed Response**
**Response Status** W

**Proposed Accept in Principle.**
Implement the following with editorial license.

Change "The RS-FEC symbols are then distributed over the 32 lanes by a permutation function. *to* "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function.".

#### 184.4.1 Functional (Bucket)

**Comment**
The Inner FEC transmit (184.4) and receive (184.5) functions provide a BCH encoder/decoder and other functions to be performed on each PCS lane. Although there is one per PCS lane, these should be called "flows" rather than "lanes" to be consistent with other FEC clauses and to differentiate between "lanes" that go between sublayers.

**Suggested Remedy**
When describing the process applied to each PCS lane in each direction, use the word "flow" rather than "lane".

**Proposed Response**
**Response Status** W

**Proposed Accept in Principle.**
Implement the suggested remedy with editorial license.

**Proposed Accept in Principle.**
Implement the following with editorial license.

In the first paragraph of clause 184.4.1 delete ", when implemented," and delete the second paragraph.

**Proposed Remedy**
Delete "when implemented" from the first sentence, and delete the second paragraph.

**Proposed Response**
**Response Status** W

**Proposed Accept in Principle.**
Comment #299 response implements suggested remedy.
Resolve using the response to comment #299

#### 184.4 Reorder (Bucket)

**Comment**
The Inner FEC transmit (184.4) and receive (184.5) functions provide a BCH encoder/decoder and other functions to be performed on each PCS lane. Although there is one per PCS lane, these should be called "flows" rather than "lanes" to be consistent with other FEC clauses and to differentiate between "lanes" that go between sublayers.

**Suggested Remedy**
When describing the process applied to each PCS lane in each direction, use the word "flow" rather than "lane".

**Proposed Response**
**Response Status** W

**Proposed Accept in Principle.**
Implement the suggested remedy with editorial license.

**Proposed Remedy**
Either explain why this mapping process is needed, or delete it.

**Proposed Response**
**Response Status** W

**Proposed Accept in Principle.**
Add text to explain the purpose of this mapping.
Implement with editorial license.
The process provided in 184.4.1 "Alignment lock and deskew" merely maps bits on the FEC service interface to vectors; it does not include RS-FEC symbol alignment. The process in 184.4.2 remaps the vectors such that there is alignment to the RS-FEC symbols and the lanes are properly ordered.

**Suggested Remedy**

Either combine the two subclauses and process into one subclause or move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

**Proposed Response**

Implement the following with editorial license.

Move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

Lane reordering is not optional; the lanes have to be put in the correct order. If they happen to arrive in the correct order, it's a simple process.

**Suggested Remedy**

Change the second sentence to say "The lane reorder process shall order the PCS lanes according to the PCS lane number."

**Proposed Response**

Resolve using the response to comment #300.

**Proposed Accept in Principle.**

The lane reorder process is stated as being optional, however, that is not the case. It is not required (or optional) if the lanes are already in order (e.g., connected to a PCS above) and mandatory if the lanes may not be in order (e.g., connected to an 8:32 PMA above), thus it is conditional, rather than optional.

**Suggested Remedy**

Change the first 2 sentences in 184.4.2 to "If the sublayer above the Inner FEC does not provide the PCS lanes in order at the service interface, the lane reorder function shall reorder the PCS lanes according to the PCS lane number."

**Proposed Response**

Resolve using the response to comment #300.

**Proposed Accept.**

It is not clear why this description is needed. Other clauses about reordering don't have this.

**Suggested Remedy**

Delete the last paragraph.

**Proposed Response**

Resolve using the response to comment #178.
This figure is not clear, nor is the relationship of the figure to the pseudocode beneath it. I think the columns 0-3 are just numbers that relate to the post-FEC distribution process. I have no idea why there are 32 sets of 4 symbols, as the algorithm doesn't do anything on a four-symbol basis. The function is simply reversing flow1 and flow0 every two columns, so that each lane has interleaved symbols from all four codewords. This could be described more simply by using blocks of 16 symbols in the figure (i.e., block 0 would be lanes 0-15 in column 0, block 1 would be lanes 16-31 in column 0, etc.).

Suggested Remedy
Revise the figure as suggested. The input side would look like this (where each row here is corresponding to 16 PCS lanes in the figure):

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>5</td>
<td>7</td>
</tr>
</tbody>
</table>

and the output would be

<p>| | | | |</p>
<table>
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<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>2</td>
<td>5</td>
<td>7</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>4</td>
<td>6</td>
</tr>
</tbody>
</table>

This will remove any confusion about whether the 32 blocks are supposed to be somehow related to the 32 PCS lanes, and it will be easier to see what is changing between the figures.

Proposed Response
Implement the suggested remedy with editorial license.

The algorithm is unnecessarily complex. There is no need for bit-level detail since the operation is performed on 10-bit symbols - though really it seems to be performed on 160-bit entities. Per figure 184-3, it's essentially receiving as input alternating sets of 160 bits from flow0 and flow1, and changing the order from 0, 1, 0, 1, 0, 1, 0, 1 to 0, 1, 0, 1, 1, 0, 1, 0.

Suggested Remedy
A minimal change would be to state that the algorithm operates on 10-bit symbols, delete the for loop and its terminator, and replace "10i+j" with "i" in the statement that describes the permutation.

Another option would be to rewrite the description around the 160-bit entities as described, and perhaps also change the figure to show those instead of 40-bit entities (which as noted in a previous comment seem to have no relevance to this process, or to the convolutional interleaver process that follows it).

Proposed Response
Implement the suggested remedy with editorial license.

The description of the convolutional interleaver process could be improved. The variable i is used in the first part of the subclause as an index for the delay lines and as an indication of time within a sequence. Then at the bottom of page 447 it's used a symbol index.

Suggested Remedy
Revise the list above the figure to read as follows, eliminating the overloading of the index i and improving the clarity a bit (and change the figure to label the lines as b=0, b=1, b=2):

a) The input and output switches are always aligned to the same row b, where b = 0 to 2
b) A block of 40 bits is read from row b
c) The contents of row b are shifted to the right by 40 bits
d) A block of 40 bits is written to row b
e) The switch position is updated to (b+1) mod 3

Proposed Response
Implement the suggested remedy with editorial license.
Since the convolutional interleaver operates separately on each PCS lane, there's no value in having an algorithm that includes the PCS lanes. Since it operates on 40-bit units, there's also no need to include bit-level description.

**Suggested Remedy**
State that the algorithm describes the operation on the 40 bit entities and is run on each PCS lane independently. This allows elimination of the p and j variables.

**Proposed Response**  
**Response Status**: W  
**PROPOSED REJECT.**  
This is correct as written. Removing the lanes and bits does not seem to add clarity, better have the detailed function as described in the adopted baseline.

---

The variable p is being overloaded - it is used at line 35 as a lane index, and at line 40 as the parity polynomial. Since the BCH encoding is done per lane, there is really no need to have a variable related to the lane number. The text can simply state that the algorithm is applied to each lane individually.

**Suggested Remedy**
Change the line above the dashed list to say "The BCH encoding is done separately on each lane. The encoding of each BCH codeword is defined as follows:"

1. At the top of page 449, remove the "for p\[n\]" loop from the pseudocode.

**Proposed Response**  
**Response Status**: W  
**PROPOSED ACCEPT IN PRINCIPLE.**  
Implement the following with editorial license:  
"The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

---

The first statement should not be a 'shall' (which indicates a PICS item of conformance). The second sentence is correct, in that there are 32 encoders, but what's actually required is that each lane has an encoder.

**Suggested Remedy**
Revise the paragraph to read: The BCH encoder works in conjunction with the RS(544,514) FEC to increase the FEC coding gain. There is a BCH encoder process for each PCS lane.

**Proposed Response**  
**Response Status**: W  
**PROPOSED ACCEPT IN PRINCIPLE.**  
Implement the following with editorial license:  
"The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

---

Clarify that the circular shift is applied per lane.

**Suggested Remedy**
Make similar changes to what was suggested in previous sections - remove the unnecessary variable p and associated for loop in the pseudocode, and add a sentence stating that the circular shift process is performed on each lane individually.

**Proposed Response**  
**Response Status**: W  
**PROPOSED ACCEPT IN PRINCIPLE.**  
Implement with editorial license:  
"The BCH encoder shall work in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. There are 32 BCH encoder functions." to: "The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."
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Cl 184 SC 184.4.7.1 P 450 L 12 # 101
Huber, Thomas
Nokia
Comment Type T Comment Status D Order (Bucket)
The DSP frame should probably be a level 3 clause of its own, rather than a sub-clause under BCH interleaver.
SuggestedRemedy
Change to a level 3 heading

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
The "BCH interleaver" function includes the pilot insertion. Change clause 184.4.7 title to: BCH interleaver and pilot insertion
Implement with editorial license.

Cl 184 SC 184.4.7.1 P 450 L 14 # 571
He, Xiang
Huawei
Comment Type TR Comment Status D DSP (Bucket)
It is said "4-bit pilot symbols (PS) are inserted every 64 4-bit blocks (one 4-bit PS, 63 4-bit message blocks)."
But in Figure 184-5, message blocks m<0:63>, m<64-127>, åbetween pilot symbols has 64 4-bit blocks.
SuggestedRemedy
Change Figure to match the text, i.e., change m<0:63> to m<0:62>, change m<64:127> to m<63:125>, etc.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl 184 SC 184.4.9 P 452 L 50 # 104
Huber, Thomas
Nokia
Comment Type T Comment Status D Interface (Bucket)
The editor's note suggesting that the mapping to analog signals probably belongs in the PMD clause seems to make sense, in which case this clause is really not "DP-16QAM mapping", it's really just mapping to 4-level signals, which the PMD will then turn into DP-16QAM.
SuggestedRemedy
Change the title to "4-level signal mapper", and make the corresponding change in 184.5.3.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
After the first sentence of subclause 184.4.9 add: "This four-level signals are used by the 800GBASE-LR1 PMD to generate a single optical DP-16QAM signal with orthogonal polarizations (see 185.4.2)."
Implement with editorial license.
The overall flow would be improved if it went BCH interleaver, 4-level signal mapping, DSP frame, with all the pilot symbol details then in the DSP frame clause.

**Suggested Remedy**

Revise so the flow is like this:

1. **184.4.7** BCH interleaver
2. **184.4.8** Four-level signal mapping (current 184.4.9, without subclauses)
3. **184.4.9** DSP frame generation (current 184.4.7.1)
4. **184.4.9.1** Pilot sequence (current 184.4.7.2 and 184.4.9.1)

**Proposed Response**

- Proposed Reject.

The text is correct as written. The actual order is the right one. It describes the bit blocks generation and handling, then the mapping to four levels.

---

The paragraph that begins with "the signals Rx Xi, Rx XQ, a" doesn't seem to make sense. The Tx and Rx signals are not guaranteed to be the same (i.e., Tx Xi can be received as any of the four components), but the contents of Tx Xi aren't distributed to all the Rx signals.

**Suggested Remedy**

Revise to say: The signals Rx Xi, Rx XQ, Rx Yi, and Rx YQ each represent one of the corresponding Tx Xi, Tx XQ, Tx Yi, Tx YQ signals from the transmitting PMD. The association between Tx and Rx components is arbitrary (e.g., Rx Xi can be any of the 4 Tx components).

**Proposed Response**

- Proposed ACCEPT.

---

The LOCK_INIT state in Figure 184û9 'DSP lock state diagram' includes the action 'test_sym <= false', however the test_sym variable isn't defined in subclause 184.6.2 'Variables' and isn't used anywhere else in Figure 184û9.

**Suggested Remedy**

Change 'test_sym <= false' to read 'test_ps <= false'.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Table 185-1, Figure 185-1, Figure 185-2 does not reflect the PHY type and clause correlation in Table 169-3a. There is no mention of 800GBASE-R BM-PMA, 800GAU-I8 2C2, 800GAU-I8 2C2M, 800GBASE SM-PMA, 800GAU-I4 2C2, and 800GAU-I4 2C2M.


Suggested Remedy
Clause 185 needs to be updated to reflect these layers. Table 185-1 needs the following entries -
800GBASE-R BM-PMA - conditional
800GAU-I8 2C2 - optional
800GAU-I8 2C2M - optional
800GBASE SM-PMA - conditional
800GAU-I4 2C2 - optional
800GAU-I4 2C2M - optional
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAU-I8 2C2/2C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAU-I4 2C2/2C2M"

Figure 185-1 should include a PMA sublayer in the diagram and be added to legend below
Figure 185-2 needs to be updated to show the 800GBASE-R PMA Sublayer and service interface between the PCS and Inner FEC

Proposed Response  Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Some optional and conditional sublayers are missing from Table 185-1 and the conditions for include the SM-PMA and BM-PMA should be included in this table.
Regarding Figure 185-1 and Figure 185-2, no PMA is shown because the 800GBASE-LR1 Inner FEC sublayer connects directly with the PCS; a PMA is not required between the PCS and 800GBASE-LR1 Inner FEC. Note that the 800GBASE-LR1 Inner FEC subsumes some functions/services normally provided by a PMA for the PMD.
Add the following rows in Table 185-1:
800GBASE-R BM-PMA - conditional
800GAU-I8 2C2 - optional
800GAU-I8 2C2M - optional
800GBASE SM-PMA - conditional
800GAU-I4 2C2 - optional
800GAU-I4 2C2M - optional
Resolve the concern about conditional SM-PMA and BM-PMA related to Table 185-1 using the response to comment #317.
Implement with editorial license.

The scrambled idle test pattern for 800GBASE-R PCS is defined in 172.2.4.11, not 175.2.4.11.

Suggested Remedy
Change "175.2.4.11" to "172.2.4.11" and format as external reference.

Proposed Response  Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

The baseline for the 800GBASE-ER[1-20] PCS has issues with PTP accuracy when an extender sublayer is used.

Suggested Remedy
Update the baseline per presentations in the May meeting proposing a mechanism to reduce the PTP inaccuracy.

Proposed Response  Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the proposal in https://www.ieee802.org/3/dj/public/24_05/sluyski_3dj_01a_2405.pdf, which was presented in the May interim meeting. Implement the suggested remedy in sluyski_3dj_01a_2405 with editorial license.
Comment Type: T  Comment Status: D

ER1 PCS: Planting the seed for when the PCS is ready to be properly reviewed.
How to calculate the path data delay across the ER1 PCS/PMA? Clause 90 and Annex 90A give general rules, like how to calculate the rx/tx path data delay when there are functions within the PHY that introduce cyclical delay.
But the path data delay in the ER1 PCS is very different from anything that has been imagined in Clause 90 - an Ethernet stream that floats within a GMP frame will present unique challenges; it is not immediately clear how to determine the min/max latency across such a PCS.
This might be worse than the Alignment marker issue!

Suggested Remedy

PROPOSED REJECT.
The suggested remedy does not provide sufficient detail to implement.