Many state diagrams in this draft as well as in the base standard use the operator "++" to indicate that the variable be incremented by 1. However, this operator is never defined.

Suggested Remedy

Add and update connector references as necessary. This is what is in 1.3:


PROPOSED ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.
### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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<td><strong>800BASE-ER1 is defined as using 800BASE-R encoding, but per 802.3df-2024, 1.4.184e - &quot;The term 800BASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation.&quot; This PHY as noted in Table 169-3a, uses PCS encoding as defined in Clause 186.</strong></td>
<td><strong>Suggested Remedy</strong></td>
<td>Define new name for family / encoding based on Clause 186 encoding. Modify definition of entry for 800GBASE-ER1 to reflect new family name.</td>
<td><strong>Proposed Response</strong></td>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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<td><strong>MLSD</strong> is used numerous times in Annex 178A to reference Maximum Likelihood Sequence Detection and should be added to the abbreviations list.</td>
<td><strong>Proposed Response</strong></td>
<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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<td>**Add MLSD</td>
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**TYPE: TR/technical required ER/editorial required GR/general required T/technical  E/editorial  G/general**

**COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn**

**SORT ORDER: Clause, Subclause, page, line**

**Page 2 of 58**
### EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

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He, Xiang
Huawei

**Comment Type**: TR
**Comment Status**: D
timesync (bucket)

Add TimeSync entity managed object classes for Inner FEC sublayers defined in Clause 177 and 184.

**Suggested Remedy**

(Presentation will be prepared for this comment.)

**Proposed Response**
Response Status: W

PROPOSED REJECT.
The following related presentation was reviewed by the 802.3dj task force during the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf
This presentation does not provide sufficient detail to describe the requested change in Clause 30.

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Huber, Thomas
Nokia

**Comment Type**: T
**Comment Status**: D
timesync (bucket)

There should also be an entry for 800GBASE-ER1 since it is a different PCS

**Suggested Remedy**
Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R (or before the entry for 800GBASE-R).

**Proposed Response**
Response Status: W

PROPOSED ACCEPT.

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Huber, Thomas
Nokia

**Comment Type**: T
**Comment Status**: D
timesync (bucket)

There should also be an entry for 800GBASE-ER1 since it is a different PCS

**Suggested Remedy**
Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R (or before the entry for 800GBASE-R).

**Proposed Response**
Response Status: W

PROPOSED ACCEPT.

---

**de Koos, Andras**
Microchip Technology

**Comment Type**: T
**Comment Status**: D
timesync (bucket)

Inner FEC (Clause 177 or Clause 184) needs MDIO registers for TimeSync. They should look like the PMA/PMD clause registers.

**Suggested Remedy**
Add the following MDIO registers for the Inner FEC, in the same style as the equivalent PMA/PMD MDIO registers
- TimeSync capability
- TimeSync transmit path data delay register
- TimeSync receive path data delay register

**Proposed Response**
Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.
The following related presentation was reviewed by the 802.3dj task force during the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf
The register bits and names described on page 8 of the presentation will be used with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement the register bits and names described on page 8 of the presentation and with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement with editorial licence.
<table>
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**Comment Type**: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

**SORT ORDER**: Clause, Subclause, page, line  
**COMMENT STATUS**: D/dispatched  A/accepted  R/rejected  
**RESPONSE STATUS**: O/open  W/written  C/closed  Z/withdrawn

---

**Comment Type**: TR  **Comment Status**: D  
Add MDIO interface registors for Inner FEC sublayers defined in Clause 177 and 184.

**Suggested Remedy**
Add definitions for the new register set defined for the Inner FEC sublayers in 30.3.1.1 - 30.1.1.14.

(Presentation will be prepared for this comment.)

**Proposed Response**  **Response Status**: W  
PROPOSED REJECT.

The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting:  
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf

This presentation concerns TimeSync management and refers to the register set "30.13.1.1 – 30.13.1.14" rather than "30.3.1.1 – 30.1.1.14".

A different comment (#603) addresses adding registers for inner FEC TimeSync.

Another comment (#183) concerns adding additional status counters for the inner FEC which will require new registers.

There is insufficient detail given in this comment (#370) and comment #183 to make a change to Clause 45 for inner FEC register definitions at this time.

---

**Comment Type**: T  **Comment Status**: D  
800GBASE-DR4-2 has longer reach than 800GBASE-FR4-500

**Suggested Remedy**  
Swap them

**Proposed Response**  **Response Status**: W  
PROPOSED ACCEPT.

---

**Comment Type**: TR  **Comment Status**: D  
Table 73-5 is missing the indication of highest priority.

**Suggested Remedy**  
change 1.6Tb/s 8lane in the capability column to 1.6Tb/s 8 lane, highest priority.

**Proposed Response**  **Response Status**: W  
PROPOSED REJECT.

Table 73-5 already indicates "lowest priority" and 73.7.6 contains this text "priority as defined in Table 73–5 (listed from highest priority to lowest priority)". So adding "highest priority" in the Table 73-5 is redundant.
In table 90A-1, the column titled “Alignment marker/ codeword marker insertion/removal” has a value of 2.56ns for 1.6T in the last row. This value should be the xMII time (at MAC data rate) of one Alignment marker block. The 1.6TE PCS lanes are now running at 100G vs 25G for slower speeds, so this number does not scale directly from the other entries. The value for the 1.6T row should be 1.28ns (a full AM group = 8 256b/257b blocks, so the MII time = 8 * 256 / 1600 = 1.28ns). Note that this column has correct values for 25G, 40G, 50G, and 100G. However, the value listed for 200G, 400G and 800G of 2.56ns should be 5.12ns and should also be fixed in maintenance.

Suggested Remedy
Change the accuracy impairment value of 2.56 ns to 1.28 ns for the 1.6T Ethernet rate in Table 90A-1.

Proposed Response
PROPOSED ACCEPT.

In table 116-3a, the last two column, missusage of PMD names.

Suggested Remedy
change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 200GBASE-KR1 and 200GBASE-CR1

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type**: TR  Comment Status: D

200GBASE-R SM PMA delay constraint is missing

**Suggested Remedy**

PROPOSED REJECT.

A suggested remedy is not provided.

200GBASE-R 8:1, 1:8, and 1:1 PMA types, all SM-PMA types are listed. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.

**Comment Status**: D

**Response Status**: W

**Proposed Response**

PROPOSED ACCEPT

Mi, Guangcan  
Huawei Technologies Co., Ltd

---

**Comment Type**: TR  Comment Status: D

In Table 116-9, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

**Suggested Remedy**

change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

**Proposed Response**

PROPOSED ACCEPT

Mi, Guangcan  
Huawei Technologies Co., Ltd

---

**Comment Type**: TR  Comment Status: D

200/400G BASE-R BM-PMA and 200/400G BASE-R-SM-PMA are noted as optional in Tables 116-3, 116-4, and 116-4a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not.

**Suggested Remedy**

For 100Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R SM PMA is "C" / conditional if either 200GAUI-1 is implemented.
For 200/400G BASE-R SM-PMA are noted as optional in Tables 116-3, 116-4, and 116-4a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not.

PROPOSED ACCEPT IN PRINCIPLE.

For 200Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R BM PMA is "C" / conditional if either 200GAUI-2 is implemented.

For 100Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE R SM PMA is "C" / conditional if either 400GAUI-2 is implemented.

For 200Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE R BM PMA is "C" / conditional if either 400GAUI-2 is implemented.

Change entries as described above in Tables 116-3, 116-4 and 116-4a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C / with notes as stated above.

Modify entry in Table 178-1 to 2000BASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C is implemented.

Modify entry in Table 178-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C is implemented.

Modify entry in Table 179-1 to 2000BASE-R SM PMA to Conditional. Add note "c" A 200GBASE-R SM PMA must be implemented if a 200GAUI-1 C2C is implemented.

Modify entry in Table 179-2 to 400GBASE-R SM PMA to Conditional. Add note "c" A 400GBASE-R SM PMA must be implemented if a 400GAUI-2 C2C is implemented.

Modify entry in Table 181-1 to 2000BASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented.

Modify entry in Table 180-2 to 2000BASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-2 C2C/C2M is implemented.

Modify entry in Table 182-1 to 2000BASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C is implemented.

Modify entry in Table 182-2 to 2000BASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #317.
The comment refers to Table 116.3.


It will be beneficial to add a note about the conditions which allow/require implementation of BM_PMA and SM_PMA. Same apply to Table 116.3a, Table 116.4, Table 169.2

**Suggested Remedy**

Add a footnote labeled æbÆ next to the æOÆ marking for 200GBASE-R SM-PMA in the entries for 200GBASE-KR2, 200GBASE-KR4, 200GBASE-CR2, and 200GBASE-CR4. The footnote æbÆ should state: æApplicable only when 200GAUI-1 C2C interface is used within the PHY.

**Provisional Accept in Principle.**

Resolve using the response to comment #312.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

Conditional PMA (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #312.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

Implement the following with editorial license:

Replace the second sentence in 116.2.4 with appropriate editorial instructions to the following:

200GBASE-R and 400GBASE-R PMAs that use bit multiplexing (BM-PMA) are specified in Clause 120.

200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176.

Implement with editorial license.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

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200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176.

Implement with editorial license.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

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200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176.

Implement with editorial license.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

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Implement with editorial license.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

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Implement with editorial license.

**Comment Type:** TR

**Comment Status:** D

**Comment:**

PMA introduction (bucket)

**Response Type:** W

**Response Status:**

PROPOSED ACCEPT IN PRINCIPLE.

The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.

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200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176.

Implement with editorial license.
I understand why the use of the stateless encoder decoder is restricted to 200GBASE-R, and 400GBASE-R over 200Gbps lanes. Allowing it on other PMDs/AUIs would be out-of-scope for the 802.3dj project. 

However, shouldn't common sense prevail, here? The stateless encoder/decoder was designed such that it is all-but-identical to the stateful encoder, only differing in their treatment of /E/ blocks. Since the 200GBASE-R and 400GBASE-R links are always protected by FEC, it is not as if /E/ blocks can occur at random causing divergent behaviour of the two encoder/decoder types. There is absolutely no danger of causing backward-compatibility issues, because the stateless encoder/decoder are still allowed for all PMDs. The stateless encoder/decoder was added to the standard to allow greater implementation flexibility (removing long timing paths). But any new PCS implementation that may attach to either 100Gbps/lane or 200Gbps/lane PMDs would have to implement the stateful encoder/decoder! With the stateless encoder, the standard is offering more implementation flexibility that implementors cannot actually use.

## Proposed Remedy
Consider removing the restriction on PMD type when using the stateless encoder and decoder in subclauses 119.2.4.1 and 119.2.5.8, respectively.

## Proposed Response
Response Status: W

PROPOSED REJECT.

As stated in the comment itself, adding an option to support stateless encoding/decoding for PHYs that are not part of the 802.3dj project is out-of-scope.

Table 116-1 and Table 116-2 include the 200Gb/s per lane PMDs which require the symbol muxing PMA. This bit muxing PMA would only be used for lower speed AUIs. Saying it supports any of the PMDs in the tables is confusing.

## Proposed Remedy
Change to "The 200GBASE-R PMA(s) can support any of the two, or four lane 200Gb/s PMDs in Table 116-1 and the 400GBASE-R PMA(s) can support any of the four, or 8 lane 400Gb/s PMDs in Table 116-2". As a less preferred approach PMA's could be changed to PHY's in the original sentence and an additional sentence could be added saying "The single lane 200Gb/s PMDs in Table 116-1 and the two lane 400Gb/s in table 115-2 require the symbol-muxing PMAs described in clause 176."

## Proposed Response
Response Status: W

PROPOSED ACCEPT IN PRINCIPLE.

Indeed, the PMA defined in Clause 120 can support only PMDs with per-lane signaling rates of 100 Gb/s or less. The referenced paragraph should therefore be corrected.

In Clause 116... Remove 200GBASE-KR1/CR1 from Table 116-3 and change table title to: "PHY type and clause correlation (200GBASE copper with 2 or 4 lanes)" Remove 400GBASE-KR2/CR2 from Table 116-3a and change table title to: "PHY type and clause correlation (200GBASE copper with 4 lanes)" Create new Table 116-3c with title "PHY type and clause correlation (200GBASE copper with 1 lanes)" Include 200GBASE-KR1/CR1 in this table.

Create new Table 116-3d with title "PHY type and clause correlation (400GBASE copper with 2 lanes)" Include 400GBASE-KR2/CR2 in this table.

In Clause 120... Change the referenced sentence to: "The 200GBASE-R PMA(s) can support any of the 200Gb/s PMDs in Table 116–3 and Table 116-4, and the 400GBASE-R PMA(s) can support any of the 400Gb/s PMDs in Table 116–3a and Table 116-5." Implement with editorial license.

[Editor's note: CC 116, 120]
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

<table>
<thead>
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</tbody>
</table>

Clause 176 is for the symbol mux PMA it should not be used for Annex 120F

Suggested Remedy

Remove the reference to 176.9.1.2

Proposed Response

Response Status W

PROPOSED REJECT.

Annex 120F is amended to include 1.6TAUI-16.

176.8.4 defines the 1.6TBASE-R 16:16 PMA, which has a 16-lane interface that can use 1.6TAUI-16 as a physical interface.

176.9.1.2 describes the precoding function for all symbol-muxing PMAs, which can also be used in the aforementioned PMA.

<table>
<thead>
<tr>
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<td>PHY descriptions (bucket)</td>
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</table>

In Table 169-3, Phy type and clause correlation was marked incorrectly for the columns of 800GBASE-DR8 PMD and 800GBASE-DR8-2 PMD

Suggested Remedy

remove the unnecessary M in the following rows for 800GBASE-DR8 PMD: 800GBASE-DR4, 800GBASE-FR4-500. remove the unnecessary M in the following rows for 800GBASE-DR8-2 PMD: 800GBASE-DR4-2, 800GBASE-FR4, and 800GBASE-LR4.

Proposed Response

Response Status W

PROPOSED ACCEPT.

<table>
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<td>PHY descriptions (bucket)</td>
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</tbody>
</table>

In Table 169-4, the delay constraints on 800GBASE-R BM-PMA and 800GBASE-R SM-PMA are missing

Suggested Remedy

add appropriate rows with TBD if no consensus has been built.

Proposed Response

Response Status W

PROPOSED REJECT.

800GBASE-R 32:4, 4:32, and 4;4, all SM-PMA types are listed in Table 169-4. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.

<table>
<thead>
<tr>
<th>Cl</th>
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<tr>
<td>PHY descriptions (bucket)</td>
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</table>

In Table 169-1, Row of 800GBASE-CR4 was described as 800Gb/s PHY using 800GBASE-R encoding over four lanes of twinaxial copper cable, which is inconsistent with the description in page 49, 1.4.184aa

Suggested Remedy

make the language consistent.

Proposed Response

Response Status W

PROPOSED REJECT.

The language used here is consistent with other similar PHY types in this table. There are similar differences between the PHYs described in this table and the definitions in 1.4.

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<thead>
<tr>
<th>Cl</th>
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<td>PHY descriptions (bucket)</td>
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</tbody>
</table>

In Table 116-6, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

Suggested Remedy

change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

Proposed Response

Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

It is assumed that the comment is referring to Table 169-6 rather than the referenced Table 116-6. Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

800GBASE-ER1-20 and 800GBASE-ER1 are both defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - “The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation.” These two PHYs as noted in Table 169-3a, they use PCS encoding as defined in Clause 186.

**Suggested Remedy**
- Define new name for family / encoding based on Clause 186 encoding.
- Eliminate table entries for ER1-20 and ER1 from Table 169-3a.
- Create new table for PHY type and clause correlation for new family based on Clause 186 encoding.
- Modify description of entry for 800GBASE-ER1-20 in Table 169-1 to reflect new family name.
- Modify description of entry for 800GBASE-ER1 in Table 169-1 to reflect new family name.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
This table lists ALL 800 Gb/s Ethernet PHY types (i.e., 800GBASE), not specifically 800GBASE-R PHY types. The description for 800GBASE-ER1 and 800GBASE-ER1-20 is deceiving and should be updated in line with the definitions in Clause 1. Table 169-3a, lists 800GBASE optical coherent PHY types (not specifically 800GBASE-R), so a separate nomenclature table is not required for 800GBASE-ER1/ER1-20.

Note that comments 111, 310, and 311 propose changes to the definitions in Clause 1.
In Table 169-1, change the definitions as follows:
- 800GBASE-ER1-20 | 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 20 km (see Clause 187)
- 800GBASE-ER1 | 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 40 km (see Clause 187)

Implement with editorial license.
**Suggested Remedy**

For 100Gb/s based PHYs the 800GBASE-R BM-PMA is mandatory, all AUIs are optional, and 800GBASE-R SM PMA is "C" / conditional if either 800GAUI-4 is implemented. For 200Gb/s based PHYs the 800GBASE-R SM-PMA is mandatory, all AUIs are optional, and 800GBASE-R BM PMA is "C" / conditional if either 800GAUI-8 is implemented.

Change entries as described above in Tables 169-2, 169-3 and 169-3a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C / with notes as stated above.

Proposed Response

Modify entry in Table 178-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 179-3 to 800GBASE-R SM PMA to Conditional. Add note "c" A 800GBASE-R SM PMA must be implemented if a 800GAUI-4 C2C is implemented. Modify entry in Table 183-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R-BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 182-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 181-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Some guidance as to when the two PMA types are used would be helpful. However, it is not as simple as proposed in the suggested remedy. Guidance is required for all PMAs used within the various xAUIs. Annex 176B provides all of the necessary guidance. Each of the tables listing physical layer clauses associated with PMD types (e.g., Table 180-3 for 800GBASE-DR4) already include a reference to Annex 176B for the AUIs, but not for the two PMAs. Additional guidance in these tables would be helpful.

In the nomenclature tables in Clause 169 it is not necessary to repeat all of these details nor is there any space in these already crowded tables; instead it would be sufficient, efficient, and future-proof to point back to the PMD clauses for guidance.

For each new PMD (Clauses 178, 179, 180 to 183, 185, 186), update the PMD tables in the PMD clause and the associated nomenclature table in Clause 116, 169, and 174, similar to the following for the 800GBASE-DR4 defined in Clause 180.

In Table 180-1, for the 800BASE-R BM-PMA row, change "Optional" to "Conditional" with the following for the 800GBASE-R BM-PMA column:

"If one or two 800GAUI-n is implemented in a PHY, additional 800GBASE-R BM-PMA or SM-PMA sublayers are required according to the guidelines in Annex 176B.6.1."

**Suggested Remedy**

Delete the offending "M"s.

Proposed Response

PROPOSED ACCEPT.

There are errors in Table 169-3. 800BASE-DR8-PMD is not needed for 800BASE-DR4 or 800BASE-DR8-500. 800BASE-DR8-2 PMD is not needed for 800BASE-DR4-2, 800BASE-DR4-2, or 800BASE-LR4.

**Suggested Remedy**

Attach the same footnote to "Required" in the row for 800GBASE-R SM-PMA.

In Table 169-3... In the cell (800GBASE-DR4 row, 800BASE-R BM-PMA column), change "O" to "C". In footnote "a" add ", C = Conditional (refer to PMD clause for details)."

**Type:** TR/technical required

**Comment Type:** TR/technical required

**Comment Status:** D<trademark>raft

**Comment Status:** D<trademark>raft

**Response Status:** W<br applications="software" content="text/html">

**Response Status:** W<br applications="software" content="text/html">

**Response Status:** W<br applications="software" content="text/html">

**Response Status:** PROPOSED ACCEPT IN PRINCIPLE.

The terms BM-PMA and SM-PMA are defined in 120.1.1 and 176.1.1. The same terms are listed in 176.2, but the items in this larger list are terms for use only within Clause 176. The definition of BM-PMA and SM-PMA should remain in the subclauses listed above. But they should also be introduced Clause 169.

**Suggested Remedy**

Move definitions of 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA from 176.2 to 169.1.3 Nomenclature.
Comment Type: T  COMMENT STATUS: D  PROPOSED ACCEPT.

There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800BASE-FR4-500. 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800BASE-LR4.

Suggested Remedy
Delete the offending "M"s

Proposed Response
PROPOSED ACCEPT.

Comment Type: TR  COMMENT STATUS: D  PROPOSED ACCEPT IN PRINCIPLE.

For 800BASE-LR1 in Table 169-3a:
- 800BASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
- 800BASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M

Suggested Remedy
- Change entries for 800BASE-LR1 to C for 800BASE-R BM-PMA and 800BASE-R SM-PMA
- Add note "C= Conditional, 800BASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
- 800BASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #317.

[Editor's note: Changed subclause from 169.1.3 to 169.1.4]
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

In support of 200 Gb/s per lane signaling - 800GBASE-R BM-PMA, Clause 176 was developed. No addition was made to 169.2 Summary of 800 GbE architecture

Suggested Remedy
Modify 169.2.4 to read -
The PMA sublayer provides a medium-independent means to support the use of a range of physical media.
The 800GBASE-R PMA, which supports bit multiplexing, is specified in Clause 173.
The 800GBASE-R PMA, which supports symbol multiplexing, is specified in Clause 176.
Note that "PMA" is used as a general term to represent both types of PMAs.

PROPOSED ACCEPT IN PRINCIPLE.
The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.
Implement the following with editorial license:
Replace the second sentence in 169.2.4 with appropriate editorial instructions to the following:
The 800GBASE-R PMA that uses bit multiplexing (BM-PMA) is specified in Clause 173.
The 800GBASE-R PMA that uses symbol multiplexing (SM-PMA) is specified in Clause 176.
Implement with editorial license.

A new 800GBASE-ER1 PCS is defined in clause 186. It should be mentioned in the introduction clause, 169.2.3 ("Physical Coding Sublayer (PCS)" in 802.3df) which currently only refers to the 800GBASE-R PCS.

Suggested Remedy
Bring 169.2.3 into the draft and amend it to include the clause 186 PCS.

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #319.
### Comment: There is no figure describing 800GBASE-ER1/-20 describing inter-sublayer service interfaces including 800GBASE-ER1 PCS/PMA

**Comment Type:** TR  
**Comment Status:** D  
**ER1 PHY (bucket)**  
**Suggested Remedy:** Add placeholder text for future text.  
**PROPOSED REJECT.** Resolve using the response to comment #78.

### Comment: The comment refers to Table 169-4. The Inner-FEC delay appears to be missing from the table

**Comment Type:** TR  
**Comment Status:** D  
**Suggested Remedy:** add 800GBASE-R inner FEC (values are TBDs)  
**PROPOSED ACCEPT IN PRINCIPLE.** Implement the suggested remedy with editorial license.

### Comment: The title of Clause 173 does include BM.

**Comment Type:** T  
**Comment Status:** D  
**Suggested Remedy:** Remove the BM- from Table 171-1 for the Clause 173 entry and footnote A  
**PROPOSED REJECT.** The term BM-PMA is used in Table 171-1, because this table includes reference to both BM and SM PMAs, and the convention we agreed on was in such cases to call out both PMAs explicitly. The same convention is used in tables 178-1, 179-1, 180-1, 181-1 and 183-1. This is explained in 173.1.1 as follows: "When necessary for disambiguation, to differentiate the bit-multiplexing PMA (BM-PMA) types defined in this clause from the symbol-multiplexing PMA (SM-PMA) types defined in Clause 176, the term BM-PMA is used. Within this clause the term PMA refers specifically to the BM-PMA."

### Comment: In tables 171-3 and 171-5, it is not clear what has changed in the rows that are shown.

**Comment Type:** T  
**Comment Status:** D  
**Suggested Remedy:** Indicate the changes with revision marks  
**PROPOSED REJECT.** Although it may be hard to see, the draft is following 802.3 editing guidelines. The thing that changed in tables 171-3 and 171-5 is that an "_" was added between "FEC_symbol_error_counter" and "<0:31>" in the status variable column. Being added text, the "_" is underlined in keeping with 802.3 editing convention. The missing underscore was missed in the 802.3df draft, including during the final publication review.
In Table 174-4, the notes for 1.6TBASE-KR8 and 1.6TBASE-CR8 says includes the
medium in one direction. No length of the medium was provided, nor any explicit delay due
to the medium was provided. While In Table 169-4, a definitive of 14ns allocated for one
direction through cable medium was provided for 800GBASE-CR4. One would assume
1.6TBASE-CR8 would be consistent with 800GBASE-CR4. The same problem applies to
1.6TBASE-KR8.

**Suggested Remedy**

Put in explicit allocation of delay constraints for the medium used in 1.6TBASE-CR8 and
1.6TBASE-KR8. Align with that of 800GBASE-CR4 and 800GBASE-KR4, if technically
feasibly.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Use the same text used for 800GBASE-KR8/CR8 in IEEE Std 802.3df-2024.

For the 800GBASE-KR4 row change the text in the note column to:
"Includes allocation of 14 ns for one direction through backplane medium. See 178.6."

For 800GBASE-CR4 row change the text in the note column to:
"Includes allocation of 14 ns for one direction through backplane medium. See 179.6."

---

Has any thought been given to how to calculate the latency through the 1.6TBASE-R PCS,
i.e. the path data delay values for the purposes of TimeSync?

I do not see anything within the 1.6TBASE-R PCS that would prevent proper calculation of
the path data delay values.

Clause 90.7.1 is instructive here, explaining that the path data delays should be "reported
as if the DDMP is at the start of the FEC codeword". However, the existing language in
90.7.1 is awkward for PCSs with more than one FEC engine like the 1.6TBASE-R PCS,
which has four FEC codewords in parallel.

**Suggested Remedy**

No proposed change to Clause 175.

Clause 90.7.1 could be cleaned up to account for when there are multiple FEC codewords
in parallel, but I assume that is out-of-scope for the 802.3dj project? I'll submit a
maintenance request.

**Proposed Response**

PROPOSED REJECT.

The suggested remedy does not propose an actionable (within the draft) remedy.
The last sentence is giving the transcoded blocks sent to each flow a name. So it's not really making a flow of blocks. If anything it's making a series or stream of blocks.

**SuggestedRemedy**

Change the last sentence to read: "The transcoded blocks sent to flow 0 are referred to as \(\text{tx\_xcoded\_f0<256:0>}\) and the ones sent to flow 1 as \(\text{tx\_xcoded\_f1<256:0>}\)."

**Proposed Response**

Implement the following with editorial license.

Change:

"This creates two flows of transcoded blocks, \(\text{tx\_xcoded\_f0<256:0>}\) to flow 0, and \(\text{tx\_xcoded\_f1<256:0>}\) to flow 1."

to:

"This creates two streams of transcoded blocks, \(\text{tx\_xcoded\_f0<256:0>}\) to flow 0, and \(\text{tx\_xcoded\_f1<256:0>}\) to flow 1."

---

Different scrambler seeds for the two flows are NOT strictly necessary for the 1.6TBASE-R PCS. The output PCSLs are never bit muxed, so having identical outputs from FEC A and FEC C, for example, should never have any adverse effect on "clock content" of the SerDes output.

It doesn't hurt to have the scramblers be seeded differently, however.

**SuggestedRemedy**

Consider changing the last sentence on page 173 from:

When reset is asserted, the two scramblers shall be initialized to a value other than zero and different from each other.

to:

When reset is asserted, the two scramblers shall be initialized to values other than zero.

(snuck in an editorial correction there, too!)

**Proposed Response**

Resolve using the response to comment #454.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Comment Type T  Comment Status D  (bucket)

Slavick, Jeff  Broadcom

Comment: tx_am_sf doesn't allow but provides a way to communicate the mandatory degrade status.

SuggestedRemedy

Change "allows the local PCS to communicate the status of the FEC degraded feature to the remote PCS" to "communicates the local PCS FEC degraded status to the remote PCS".

Proposed Response  Response Status W

PROPOSED REJECT.
The draft is correct as written, and the proposed change does not improve clarity.

Comment Type T  Comment Status D  (bucket)

Opsasnick, Eugene  Broadcom

Comment: Sub-clause 172.2.4.6 has a reference to a text file containing the 800GBASE-R alignment marker values. CL 175 should add a similar note with a corresponding text file for the 1.6TBASE-R alignment markers.

SuggestedRemedy

Add text near line 22: "NOTE: A text file containing the alignment marker patterns, as shown in Table 175/1 is available at https://standards.ieee.org/downloads/802.3/.'

A presentation will be submitted with a corresponding text file containing the 1.6TBASE-R AM values.

Proposed Response  Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Improve the suggested remedy with editorial license.

Comment Type T  Comment Status D  (bucket)

Slavick, Jeff  Broadcom

Comment: am_mapped_f0 and am_mapped_f1 aren't solely based on the 10b-distribution and we never talk about how this two variables are us splitting the alignment marker group up.

SuggestedRemedy

Change:

- The variables am_mapped_f0 and am_mapped_f1 are then derived from 10-bit interleaving the group of 16 alignment markers, am_x, using the following procedure:
- The alignment marker group is mapped into variables am_mapped_f0 and am_mapped_f1 as follows. First a 10-bit interleaving of the group of 16 alignment markers, am_x, is done using the following procedure:

Proposed Response  Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

Comment Type T  Comment Status D  (bucket)

Slavick, Jeff  Broadcom

Comment: am_mapped_f0 and am_mapped_f1 contain data that is sent into flow 0/1 and through codewords AB and CD.

SuggestedRemedy

Change:

- Note that am_mapped_f0 contains the 10-bit symbols of FEC codewords A and B, and am_mapped_f1 contains the 10-bit symbols of FEC codewords C and D.
- Note that am_mapped_f0 is sent to flow 0 which produces FEC codewords A and B, and am_mapped_f1 is sent to flow 1 which produces FEC codewords C and D.

Proposed Response  Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.
## IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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**Comment Type**: T  **Comment Status**: D  **(bucket)**

**Comment**: Add a intro to what tx_scrambled is.

**SuggestedRemedy**: Change:

> "The variables tx_scrambled_am_f0<10279:0> and tx_scrambled_am_f1<10279:0> are constructed in one of two ways."

To:

> "In each flow a 10280-bit block of data is formed with two FEC codewords worth of message data. tx_scrambled_am_f0<10279:0> in flow 0 and tx_scrambled_am_f1<10279:0> in flow 1 and they are constructed in one of two ways."

**Proposed Response**: PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

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**Comment Type**: T  **Comment Status**: D  **(bucket)**

**Comment**: The Note about tracking statistics across all 4 decoders is missing from the bin counter.

**SuggestedRemedy**: Add this to the definition of the FEC_c codeword_error_bin_i.

> "Note that this counter tracks codewords with errors across all four codewords."

**Proposed Response**: PROPOSED ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

---

**Opasnick, Eugene**

**Comment Type**: T  **Comment Status**: D  **(bucket)**

**Comment**: Annex 175A contains tabular data for an example created by the 1.6TBASE-R PCS TX functions, including the scrambler output, RS-FEC codeword generation, and PCS lane interleaving. The editor's note on page 539 has a placeholder for a link to a text file that has the machine readable text data. That data file needs to be created.

**SuggestedRemedy**: A presentation is planned to submit a data file which corresponds to the Annex 176A example and can be referenced in the editor's note.

**Proposed Response**: PROPOSED ACCEPT IN PRINCIPLE.


Implement with editorial license.

---

**Slavick, Jeff**

**Comment Type**: T  **Comment Status**: D  **(bucket)**

**Comment**: Annex 175A contains tabular data for an example created by the 1.6TBASE-R PCS TX functions, including the scrambler output, RS-FEC codeword generation, and PCS lane interleaving. The editor's note on page 539 has a placeholder for a link to a text file that has the machine readable text data. That data file needs to be created.

**SuggestedRemedy**: A presentation is planned to submit a data file which corresponds to the Annex 176A example and can be referenced in the editor's note.

**Proposed Response**: PROPOSED ACCEPT IN PRINCIPLE.


Implement with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Has any thought been put into how to calculate the path data delay values (MII-MDI latencies for timestamping) for the SM-PMAs? For bit-mux PMAs, it is very simple - i.e. it is all implementation delay, since the intrinsic delay from bit-muxing/demultiplexing is negligible. But at first glance, determining the latency across the Clause 176 PMA looks more like a challenge.

a. I don't believe that the intrinsic (i.e. non-implementation) delay is deterministic, due to the partial deskew.

b. But apart from the partial deskew, the latency across the SM-PMA should be deterministic using the principles in Annex 90A.7 (max latency value used for Tx path data delay, min latency value used for Rx path data delay).

c. Traditionally, how to calculate the delays through the PHY layers has been an implementation concern, but this is because the calculation was straightforward at lower rates. At 200Gbps lanes, the standard does not have the luxury of being able to ignore this. If it is overly complicated or ambiguous, and opposite ends of a link do not implement it in the same fashion, the system Time Synchronization will be impaired.

**Suggested Remedy**
Consider a note in Clause 176 (or next to the PMA path data delay MDIO registers - 45.2.1.176, 45.2.1.177) that the path data delay values for the SM-PMA should be calculated via the method in Annex 90A.7.

I don't think it is necessary, but if a more detailed explanation is deemed useful, then a subclause could be added to Clause 90.7 spelling out explicitly how the path data delay values should be calculated for the SM-PMA.

**Proposed Response**
PROPOSED REJECT.

It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.

---

The comment refers to Figure 176û2. The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols.

The intention is to delay the odd (Tx) and even (Rx) PCSLs by 136 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs. Same apply to Figure 176û9

**Suggested Remedy**
Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 136 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 136 symbols"

**Proposed Response**
PROPOSED REJECT.
The function in Fig 176-2 uses the words "2 RS-FEC codewords" as opposed to "136 RS-FEC symbols" because the function aims to align the 2 codewords on even lanes with 2 different codewords on odd lanes by delaying odd lanes by 2 codewords. This enables symbol multiplexing across 4 codewords. Same applies to Fig 176-9, 176-11 and 176-13.

While it is not inaccurate to call it a "136 symbol delay", an advantage of using "2 RS-FEC codewords" as opposed to "136 symbols" is that the function name is equally applicable to both 200GE and 400GE SM-PMAs. Moreover, the first line of subclause 176.5.1.3.4 clearly specifies the delay as being 136 RS-FEC symbols, and the subsequent line shows this mathematically as "2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols." Similarly, subclause 176.6.1.2.4 (400GE 16:2 PMA) specifies the delay to be 68 symbols. Hence, the delay value is clearly specified and there is no room for misinterpretation.

The comment proposes an alternate description which is technically correct but does not improve the accuracy or readability of the standard.
There is reference in the text to lock process in Figure 119-12. However, there are exceptions to Figure 119-12 as outlined in 176.5.1.6. It can be beneficial to refer to 176.5.1.6 which include both the reference to Figure 119-12 and the list of exceptions list.

**Suggested Remedy**

Add a reference to 176.5.1.6 instead of Figure 119-12.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Add note in parenthesis "(see 176.5.1.6.4)" after Fig 119-12.

Implement with editorial license.

---

There is more details to the AM lock function add a reference

**Suggested Remedy**

add a "(see 175.5.1.6.4)" after Table 119-1

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #534.

[Editor's note: Changed clause, subclause from 175, 175.5.1.3.1 to 176, 176.5.1.3.1]
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Cl 176  SC 176.5.1.3.4  P202  L51  # 537
Rechtman, Zvi  Nvidia

Comment Type: TR  Comment Status: D  DelayOddPCSLs (bucket)
The sentence “This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords 1544 symbols per codeword / 8 PCS lanes = 136 symbols).” can be misinterpreted:

136 symbol delay x 4 odd PCS lanes = 544 symbols delay in total (not 2 RS-FEC codewords delay)

Suggested Remedy:
- Remove "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords 1544 symbols per codeword / 8 PCS lanes = 136 symbols)."

Modify: “Adding the two codeword delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer.”

To: “Adding the 136 symbol delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer.”

Proposed Response: Response Status: W
PROPOSED REJECT.
The first line of subclause 176.5.1.3.4 clearly specifies that the odd lanes are delayed by 136 RS-FEC symbols, and the subsequent line describes mathematically that this (136 symbol delay) is equivalent to adding a delay of 2 codewords to the odd lanes by showing that “2 codewords x 544 symbols per codeword / 8 PCS lanes = 136 symbols”. There is little room left for misinterpretation, since the delay in symbols is stated upfront.

Cl 176  SC 176.5.1.3.4  P203  L4  # 293
Galan, Jose Vicente  Maxlinear Inc

Comment Type: T  Comment Status: D  Figures (bucket)
For Figure 176-5, it has to be explained what AÆ/BÆ shall be.

Suggested Remedy:
- Add an explanation for AÆ/BÆ, e.g., “AÆ/BÆ are the symbols from previous 2 CWs that are delayed”

Proposed Response: Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Update the text referencing Fig 176-5 in (176.5.1.3.4) to state that RS-FEC symbols A and A’ belong to different codewords from FEC-A, and B and B’ belong to different codewords from FEC-B.

Implement with editorial license.

Cl 176  SC 176.5.1.3.5  P204  L1  # 291
Galan, Jose Vicente  Maxlinear Inc

Comment Type: T  Comment Status: D  Figures (bucket)
In Figure 176-6, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols.

Suggested Remedy:
- Change the direction of the arrow to follow the actual transmission order.

Proposed Response: Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Update Fig 176-6 to clarify the order of transmission on the output lane, with editorial license.
Is there anything preventing an implementation from performing a full deskew at the Rx PMA? It is not technically required, but does not cause any adverse functional effects.

A full deskew at the Rx SM-PMA would NOT change end-to-end latency, since the skew is all ultimately undone at the Rx PCS. A deskew upstream would simply offload the deskew from the Rx PCS.

Implementations with a SM-PMA attached to an RxPCS will undoubtedly perform the Alignment marker lock only once (not once in the PMA and again in the PCS). AM-lock plus deskew is a very natural coupling of functions.

Suggested Remedy

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):

After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before the would not have and adverse functional effects.

Suggested Remedy

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):

After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before the would not have and adverse functional effects.

Suggested Remedy

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Comment Type T

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.

An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implementation choice, and should not be called out in the standard.

Slavick, Jeff

Proposed Response

PROPOSED REJECT.
Comment Type: TR/technical required
Comment Status: D/dispatched

Comment
The comment refers to Figure 176û11.
The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols.
The intention is to delay the odd (Tx) and even (Rx) PCSLs by 68 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.

Suggested Remedy
Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 68 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 68 symbols"

Proposed Response
PROPOSED REJECT.
Resolve using the response to comment #533.

Comment
In Figure 176û12, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols

Suggested Remedy
Change the direction of the arrow to follow the actual transmission order.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Update Fig 176-12 to clarify the order of transmission on the output lane, with editorial license.

Comment
The 800GBASE-R PCS has 4 FEC engines, so figures 176û16, 176û17, 176û18 should use C,D to illustrate the symbols on PCSLs 16-31, rather than A',B'. The A',B' notation is used in 200GBASE-R and 400GBASE-R figures to denote CWs from engines A and B but with the 2CW delay.

Suggested Remedy
Amend Figures 176û16, 176û17, 176û18 to avoid the A',B' notation

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Update the text referencing figures Fig 176-16, Fig 176-17 and 176-18 (in 176.7.1.2) to state the RS-FEC symbols A and B are from FEC-A and FEC-B in flow 0 of the 800GBASE-R PCS, while the RS-FEC symbols A' and B' are from flow 1 of the 800GBASE-R PCS. Implement with editorial license.
Comment Type: T  Comment Status: D Figures (bucket)  
In all Figures in the 800G PMA section, it is referred to AÆ/BÆ symbols, although we have 
4 RS CWs

SuggestedRemedy  
Change to use A, B, C, D for the 4 RS CWs, instead of A, B, AÆ, BÆ

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 593

Comment Type: T  Comment Status: D Figures (bucket)  
In Figure 176-18, the output lane arrow is indicated in the opposite direction than the actual 
transmission order of the output PCSL symbols

SuggestedRemedy  
Change the direction of the arrow to follow the actual transmission order.

PROPOSED ACCEPT IN PRINCIPLE.

Comment Type: T  Comment Status: D Figures (bucket)  
In clause 176A.2.2, 'Control and status fields' says that 'The control field comprises 16 bits 
with the structure defined in 176A.3.', yet figure 176A-1 'Training frame structure' above 
shows the control field comprising of 16 cells. It, therefore, appears that the field is 
comprised of 16 cells that convey 16 bits.

SuggestedRemedy  
[1] Change the first paragraph of 176A.2.2 to read 'The control field is comprised of 16 cells 
which convey 16 bits with the structure defined in 176A.3. The status is comprised of 16 cells 
which convey 16 bits with the structure defined in 176A.4.'

[2] Change the last sentence of the penultimate paragraph of 176A.2.2 to read 'Within each 
field, the order of transmission is from bit 15 to bit 0, conveyed by cell 15 to cell 0 respectively.'

PROPOSED REJECT.

The cell concept is described in detail in the following paragraph (second paragraph of 
176A.2.2). Note that the text is identical to the text in 136.8.11.1.2.

Text is correct as written, proposed remedy does not improve the clarity of the draft.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Comment Type: TR  Comment Status: D  ILT Pattern (Bucket)

"The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0)"

Some interfaces have 8 lanes.

The default mapping provided in Table 176Aû1 can be used instead.

Suggested Remedy
Change to "The default identifier for each lane is the same as that shown in Table 176A-1".

Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "The default identifier for each lane is its lane number"
To: "The default identifier for each lane is the same as that shown in Table 176A-1"

Comment Type: T  Comment Status: D  ILT Pattern (Bucket)

The PRBS gen should "stop" if training stops.

Suggested Remedy
Add "while training is in progress while this mode is selected" after "is not stopped or reset".

Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

ILT Coefficients (Bucket)

The comment refers to Table 176Aû3ûStatus field structure.
The field in bit 14 - "One" require some explanation. ItÆs unclear whether it refers to the support of the newly adopted test patterns, the support of multi-segment operation, or both.

Suggested Remedy
Define the purpose of this bit

Proposed Response  Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Add new section after the Receiver Ready section:
"176A.4.2 One
The one bit is set to 1 to signal the local receiver that the link partner supports the multi-segment control function."

Note that comment #196 proposes to change "multi-segment control function" to "inter-sublayer link training". If necessary, adjust the text to reflect the new terminology.
Suggested Remedy

Remove the "No data is available." from the option 1 of Extend training bit

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

Suggested Remedy

In 176A.4.3 change the text '... response time requirements specified in 176A.10 are met.' to read '... response time requirements specified in 176A.8 are met.' and the text '... and is not set to 1 until training and local_tf_lock are both true.' To read '... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.10 can be met.'

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Change: "... response time requirements specified in 176A.10 are met.

To: "... response time requirements specified in 176A.8 are met.

Change: "... and is not set to 1 until training and local_tf_lock are both true.

To: "... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.8 can be met."
Comment Type: TR/technical required
Comment Status: D/dispatched
ILT Coefficients (Bucket)

When the interface control state diagram (Figure 176A6) is in the TRAIN_LOCAL state, the device may request its link partner to...

It is important to also note at which states requests from the link partner should be processed, and what happens in the other states - this may not be obvious.

Suggested Remedy

Insert the following paragraphs after the first one:

When the interface control state diagram is in either the TRAIN_LOCAL or TRAIN_REMOTE state, the device shall respond to requests received from the link partner.

When the interface control state diagram is in any state other than TRAIN_LOCAL or TRAIN_REMOTE, the device shall not send any requests to the link partner and shall ignore requests from the link partner.

Proposed Response

Response Status: W
PROPOSED ACCEPT.

Comment Type: TR/technical required
Comment Status: D/dispatched
ILT Coefficients (Bucket)

"When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 2 ms"

This requirement was defined in 802.3cd when training was limited in time (to 3 seconds) in order to prevent limiting the number of change requests due to delayed responses.

The new training scheme is not limited in time, and a receiver can use as many requests as it needs.

In some multi-tasking implementations, a hard 2 ms maximum may be challenging to meet. To avoid real-time requirements, it would be sufficient to have 2 ms as the average response time (and it does not need to be normative). The maximum response time can be relaxed without impact to the protocol.

Suggested Remedy

Change to

"When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 20 ms. It is recommended that the average response time is less than 2 ms".

Proposed Response

Response Status: W
PROPOSED ACCEPT.

Comment Type: T/technical
Comment Status: D/dispatched
ILT (Bucket)

Figure 176A5 ‘Retimer reference model’ shows the data multiplexer driven by the tx_mode value, with the multiplexer select set to 0 when tx_mode = training and set to 1 when tx_mode = data. Subclause 176A.10.2.1 ‘Variables’, however, defines three values for tx_mode, training, local_pattern and data. Figure 176A5, therefore, does not define the multiplexer select value for when tx_mode = local_pattern.

Suggested Remedy

Update the figure to reflect the third value of tx_mode and the local pattern generator for each interface.

Proposed Response

Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add the local_pattern option to the data selector.
Add a Local pattern box as an input to the data selector.
The arrow pointing to the Interface A 'Driver' block and arrow pointing from the Interface B 'CDR' block both seem to be pointing in the wrong direction.

**Suggested Remedy**
Reverse the direction of both arrows.

**Proposed Response**

**Proposed Accept.**
The last sentence of the tx_disable variable description says that the '... output on the lane is disabled.' Is this correct, the first sentence says that tx_disable '... controls the transmitter's output on the interface.' and tx_disable is defined under subclause 176A.10.2 'Per-interface variables, functions and timers'. Suggest that the reference to 'lane' is changed to 'interface', or use 'all lanes of the interface' in the variable description to reflect the segment_ready variable description immediately above.

**Suggested Remedy**

- Either
  - [a] Change the text '... output on the lane is disabled.' in the last sentence of the tx_disable variable description to read '... output on the interface is disabled.'.
  - [b] Change [1] the text '... the transmitter's output on the interface.' in the first sentence of both the tx_disable and tx_mode variable descriptions to read '... the transmitter output on all lanes of the interface.'; and [2] the text '... output on the lane is disabled.' in the last sentence of the tx_disable variable description to read '... output on all lanes of the interface is disabled.'.

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.

The Interface control state diagram in Figure 176A-6 is implemented per lane, only the RTS update state diagram in Figure 176A-7 is implemented per interface.

It would be helpful to separate the state diagrams into the per-interface and per-lane subclasses.

Implement the following with editorial license.

- Change the first sentence of 176A.10.2...
  - from: "A device implements one instance of each of the interface control state diagrams"...
  - to: "A device implements one instance of the RTS update state diagram".

Break subclause 176A.10.4 (State diagrams) into two subclauses, one in 176A.10.2 (Per-interface variables, functions and timers) and one in 176A.10.3 (Per-lane variables, functions, timers and counters).

Change the title of Figure 176A–6 from "Interface control state diagram" to Figure 176A–6 from "Training control state diagram".

**Suggested Remedy**

- Change "The device implements one instance of each of the interface control state diagrams ..." to read 'The device implements one instance of each of the frame lock and coefficient update state diagrams ...'.

**Proposed Response**

**Response Status** W

PROPOSED ACCEPT IN PRINCIPLE.

tx_disable is a per lane variable.

Implement the following with editorial license.

- Move the definition of tx_disable to 176A.10.3.
- Change the first sentence of the definition...
  - from: "Boolean variable that controls the transmitter's output on the interface."
  - to: "Boolean variable that controls the transmitter's output on the lane."
The variables local_tf_lock, remote_tf_lock, local_rx_ready and remote_rx_ready are all defined in 176A.10.3 ‘Per-lane variables, functions, timers and counters’ and are related to a lane, yet they are used by figure 176A-6 ‘Interface control state diagram’. 176A.10.2 ‘Per-interface variables, functions and timers’ says ‘A device implements one instance of each of the interface control state diagrams independently for each of its interfaces (see 176A.9).’.

**Suggested Remedy**
Perhaps figure 176A-6 ‘Interface control state diagram’ should use a ‘interface’ version of each of these variables that are a logical AND of the respective lane variable in the case of a multi-lane interface.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the responses to comments #566, #567 and #571.

---

The description of the local_tf_lock variable in 176A.10.3.1 says that ‘The value of this variable is encoded as the “training lock” bit in the status field of transmitted training frames.’, however, there isn’t a “training lock” bit defined for the training frames. Since 176A.4.3 ‘Receiver frame lock’ says ‘Receiver frame lock … is not set to 1 until training and local_tf_lock are both true.’ it seems that local_tf_lock is encoded in the ‘Receiver frame lock’ bit.

**Suggested Remedy**
Change the text ‘… is encoded as the “training lock” bit …’ in the local_tf_lock variable description to read ‘… is encoded in the “Receiver frame lock” bit …’.

**Proposed Response**
PROPOSED ACCEPT.
There is a spurious '<' within the transition condition from the state TRAIN_LOCAL to the state TRAIN_REMOTE.

**Suggested Remedy**

Suggest that 'local_tf_lock<* local_rx_ready' should read 'local_tf_lock * local_rx_ready'.

**Proposed Response**

Response Status: W

PROPOSED ACCEPT.

---

The WAIT_ADJACENT to SWITCH_CLOCK transition condition uses the variable mr_training_enabled, however subclause 176A.10.2.1 'Variables' defines the variable mr_training_enable, not mr_training_enabled.

**Suggested Remedy**

Change the transition condition ' (!mr_training_enabled + segment_ready) * ...' to read ' (!mr_training_enable + segment_ready) * ...'.

**Proposed Response**

Response Status: W

PROPOSED ACCEPT.

---

C2C loss is TBD

**Suggested Remedy**

Assuming 28 dB budget and package A length ~300 mm and ~125 mm for package B

**Proposed Response**

Response Status: W

PROPOSED REJECT.

The comment addresses an open TBD, but the suggested remedy is unclear.

Also, the suggested remedy assumes the budget is 28 dB, but consensus on that has not been shown.
Cl 176D SC 176D.3.3  P597  L33  # 398
Wu, Mau-Lin   MediaTek
  Comment Type   TR   Comment Status   D
  The value of '106.255 +/- 50 ppm' is not correct.
  SuggestedRemedy
  Change '106.255' to '106.25'.
  Proposed Response   Response Status   W
  PROPOSED ACCEPT IN PRINCIPLE.
  Resolve using the response to comment #361.

Cl 176D SC 176D.3.3  P597  L33  # 423
Li, Tobey   MediaTek
  Comment Type   TR   Comment Status   D
  Signaling rate of 106.255 +/- 50 ppm in Table 176Dûû is incorrect.
  SuggestedRemedy
  Change "106.255 +/- 50 ppm" to "106.25 +/- 50 ppm".
  Proposed Response   Response Status   W
  PROPOSED ACCEPT IN PRINCIPLE.
  Resolve using the response to comment #361.

Cl 176D SC 176D.3.4.4  P602  L47  # 424
Li, Tobey   MediaTek
  Comment Type   TR   Comment Status   D
  Reference to ERL methodology is missing.
  SuggestedRemedy
  Add reference to 176D.4.3.
  Proposed Response   Response Status   W
  PROPOSED ACCEPT.

Cl 176D SC 176D.3.4.4  P603  L30  # 426
Li, Tobey   MediaTek
  Comment Type   TR   Comment Status   D
  "Insertion loss at 26.5625 GHz"
  Nyquest frequency in Table 176Dûû is incorrect.
  SuggestedRemedy
  Change "26.5625 GHz" to "53.125 GHz".
  Proposed Response   Response Status   W
  PROPOSED ACCEPT.
  Resolve using the response to comment #426.

Cl 176D SC 176D.3.4.4  P603  L31  # 451
Simms, William   NVIDIA
  Comment Type   TR   Comment Status   D
  Moot point maybe given table is all TBD, but the frequency should be 53.125GHz.
  SuggestedRemedy
  change to 53.125GHz.
  Proposed Response   Response Status   W
  PROPOSED ACCEPT IN PRINCIPLE.
  Resolve using the response to comment #426.

Cl 176D SC 176D.3.4.5  P604  L1  # 428
Li, Tobey   MediaTek
  Comment Type   TR   Comment Status   D
  Reference to test procedure is missing.
  SuggestedRemedy
  Add reference to 176D.3.4.4
  Proposed Response   Response Status   W
  PROPOSED ACCEPT.

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected     RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Clause, Subclause, page, line
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<td>COM reference package parameter value. (transmission line parameter tau)</td>
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<tr>
<td>In &quot;Table 176D.6&quot; class A package model Transmission line parameter (t(tau)) value is 6.141e-4 ns/mm, but based on the adopted motion#10. Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.</td>
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<td>SuggestedRemedy</td>
<td>Change (t(tau) value in Table 176D-6 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm. Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.</td>
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<td>An insertion loss of only 20dB is less than desirable and the equation is TBD. We shouldn't specify the loss at this time</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE. The value 20 dB was not adopted, and its appearance here is unintended. Slide 18 of <a href="https://www.ieee802.org/3/dj/public/24_01/ran_3dj_01a_2401.pdf">https://www.ieee802.org/3/dj/public/24_01/ran_3dj_01a_2401.pdf</a> states explicitly that the interconnect length is TBD. Implement suggested remedy with editorial license.</td>
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<tr>
<td>176E</td>
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<td>20</td>
<td>The note &quot;The electrical specifications of C2C components are not equivalent to those of the corresponding PMD's. Specifically the test points at which module compliance is defined are different isn't helpful. What does &quot;not equivalent&quot; mean?. Which corresponding PMD's? Although the module test points are different those for the host are the same as Clause 179.</td>
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<td>SuggestedRemedy</td>
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<td>The note &quot;The electrical specifications of C2C components are not equivalent to those of the corresponding PMD's. Specifically the test points at which module compliance is defined are different isn't helpful. What does &quot;not equivalent&quot; mean?. Which corresponding PMD's? Although the module test points are different those for the host are the same as Clause 179.</td>
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<td>Proposed Response</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE. The corresponding PMDs are noted in the third paragraph of 176E.2, which states that a C2M component is functionally equivalent to a PMD. The note appears after the paragraph about the electrical characteristics, and highlights the essential difference between a C2M component and a PMD. It is specific about the test point difference for the module. The description of the C2M component's similarity to a PMD is new, and noting the differences is useful for readers. However, the term &quot;corresponding PMDs&quot; can be clarified. In 176E.2, change &quot;the corresponding PMDs&quot; to &quot;the corresponding PMDs defined in Clause 179&quot;. In 176D.2, change &quot;The electrical specifications of C2C components are not equivalent to those of the corresponding PMDs&quot; to &quot;The electrical specifications of C2C components are not identical to those of the corresponding PMDs defined in Clause 178&quot;.</td>
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<td>COM reference package parameter value. (transmission line parameter tau)</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE. Resolved using the response to comment #118.</td>
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EEC P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

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<td>Suggested Remedy</td>
<td>Figure depicts loss should be bump-bump</td>
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<td>Suggested Remedy</td>
<td>To make it more clear Host C2M Component should be changed to Host C2M Device and Module C2M Device</td>
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**Proposed Response**

**Response Status** W

The C2M loss budget is currently TBD, but it is expected that it will be inclusive of packages. However, the suggested remedy does not significantly clarify this fact. It is preferable to align the diagram with Figure 179-2, where the paths between TP0d and TP1 and between TP4 and TP5d are shown to include the package. In figure 176E-2, change "Host ILdd" to "Host package and PCB ILdd", and "Module ILdd" to "Module package and PCB ILdd".

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**Proposed Response**

**Response Status** W

The loss in the text is TBD because equation 176E-3 has TBDs. When an equation is provided, the text can be changed accordingly, but the commend does not propose values for the equation. The following presentation was reviewed by the task force in the May 2024 interim meeting: https://www.ieee802.org/3/dj/public/24_05/ghiasi_3dj_02_2405.pdf

The presentation does not include a proposa equation 176E-3.

[Editor's note: changed page from 621 to 632]
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<td>The second bullet could be written more clearly</td>
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**Suggested Remedy**

Revise to read "Distributing (collecting) the convolutional interleaved data to (from) eight Inner FEC flows"  

**Proposed Response**

PROPOSED ACCEPT.

<table>
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<td>The fifth bullet could be written more clearly</td>
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**Suggested Remedy**

Revise to read "8:1 interleaving (1:8 deinterleaving) the eight Inner FEC flows to (from) a single flow"

**Proposed Response**

PROPOSED ACCEPT.

<table>
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<td>PAM4 decoding (bucket)</td>
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<td>The comment refers to Figure 177.2. There is a footnote that PAM4 decoding is optional in case of soft decoding. However, the DataPath is defined using bit streams, also the FEC:IS_UNITDATA_i.indication primitives has two value of 0 or 1, therefore PAM4 decoding must to take place</td>
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**Suggested Remedy**

Either remove the footnote, or elaborate on the intention of this footnote.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE. Resolve using the response to comment # 83.

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<td>177.4.1</td>
<td>250</td>
<td>36</td>
<td>505</td>
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<tr>
<td>de Koos, Andras</td>
<td>Microchip Technology</td>
<td></td>
<td></td>
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<tr>
<td>Comment Type</td>
<td>T</td>
<td>Comment Status</td>
<td>D</td>
<td>timesync (bucket)</td>
<td></td>
</tr>
<tr>
<td>Due primarily to the convolutional interleaver/deinterleaver, there is a large variation in the input-to-output latency of the Inner FEC sublayer. As such, there is concern that the method to properly calculate the path data delay for the Inner FEC sublayer should be explained in Clause 90, similarly to what is done for the variation from FEC codewords and PCS-lane distribution in clause 90.7.1.</td>
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</tbody>
</table>

**Suggested Remedy**

Do nothing. Using the general method in Clause 90A, allocating the maximum value of the intrinsic delay to the transmit PHY and the minimum value of the intrinsic delay to the receive PHY, there is no ambiguity. So it should not be necessary to add to Clause 90 for every new PHY type. The principles laid out in Annex 90A.7 should apply. If anything, a general note could be added in Clause 177 (or in Clause 45 with the MDIO registers for path data delay values) explaining that the Tx/Rx path data delay values should be calculated following the guidelines in Annex 90A.7, where the maximum latency value is used for the Tx path data delay, and the minimum latency value is used for Rx path data delay.

**Proposed Response**

PROPOSED REJECT. The suggested remedy does not propose an actionable (within the draft) remedy. It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.
<table>
<thead>
<tr>
<th>CI</th>
<th>SC</th>
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<tr>
<td>177</td>
<td>177.4.1</td>
<td>T</td>
<td>D</td>
<td>&quot;The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay&quot; is correct only if the Q values are 544/272/136/68 for 200G/400G/800G/1.6T. However, the Q values should be 192/96/48/24 as shown in slides 6-11 of he_3dj_01_2307 for 200G/400G/800G/1.6TbE.</td>
<td>SuggestedRemedy</td>
<td>W</td>
</tr>
<tr>
<td>177</td>
<td>177.4.1</td>
<td>TR</td>
<td>D</td>
<td>The Q values are not the same as the baseline adopted.</td>
<td>SuggestedRemedy</td>
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<td>177</td>
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</table>
Comment Type | Comment Status | CI (bucket) | Cl 177 | SC 177.4.1 | P 252 | L 19 | # 488
--- | --- | --- | --- | --- | --- | --- | ---
Slavick, Jeff | Broadcom | The delay line for Cl177 starts with feeding data into the longest delay line while Cl184 sends it to the delay line with the shortest delay.

Suggested Remedy
- Change Cl177 to have the Delay Line 0 be the minimal delay and the Delay Line 2 to be the longest delay.

Proposed Response | Response Status | W
PROPOSED REJECT.
This is consistent with the adopted baseline. It is correct as documented.

Comment Type | Comment Status | CI - Editorial (bucket) | Cl 177 | SC 177.4.1 | P 256 | L 50 | # 545
--- | --- | --- | --- | --- | --- | --- | ---
Rechtman, Zvi | Nvidia | The input and output round-robin operation is defined relatively to the delay/buffering size of each lane. However, there are lines index that represent the delay and simplify the definition.

Suggested Remedy
- Modify to:
  "The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay"

Seems to represent block interleave and not convolutional interleave.

Proposed Response | Response Status | W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Comment Type | Comment Status | CI - Editorial (bucket) | Cl 177 | SC 177.4.3 | P 252 | L 37 | # 507
--- | --- | --- | --- | --- | --- | --- | ---
de Koos, Andras | Microchip Technology | Was there not a proposal to make the circular shift optional, in order to minimize latency?

Suggested Remedy
- Consider removing the circular shift if it does offer no worthwhile benefit.

Proposed Response | Response Status | W
PROPOSED REJECT.
This is consistent with the baseline adopted. The comment does not provide sufficient justification to support the suggested remedy.
I'm not convinced that the circular shift really adds any robustness. Yes, it distances bit-pairs belonging to the same RS-FEC codeword, but
Without the shift, the consecutive bit pairs (after 8:1 multiplexing) belonging to the same RS-FEC code words would each protected by different Inner FEC code words, would they not?
So is the circular shift just protecting against uncorrected inner-FEC codewords that would all land on the same RS-FEC codeword? Seems overkill. Are there simulations/models showing the benefit of including circular shift?

Suggested Remedy
Consider removing the circular shift if it does not offer any worthwhile benefit.

Proposed Response Response Status W
This is consistent with the baseline adopted. The comment does not provide sufficient justification to support the suggested remedy.

The systematic Hamming code is most naturally defined in terms of its parity-check matrix, as pointed out in many textbooks and standard documents. One famous example is the systematic double-extended Hamming(128,119) code in OIF-400ZR and ITU-T G.709.3.

Suggested Remedy
Suggest to include the construction process and parity-check matrix of the adopted Hamming(68,60) code to enhance the completeness of the document. A Supporting Presentation will be provided.

Proposed Response Response Status W
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting
https://www.ieee802.org/3/dj/public/24_05/huang_3dj_01a_2405.pdf
Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Cl 177  SC 177.4.6  P254  L31  # 604

de Koos, Andras  Microchip Technology

Comment Type  T  Comment Status  D  timesync(bucket)

Phase of inner FEC pad bits vs outer FEC parity bits:
- An inaccuracy in the path data delay of up to 12ps due to arbitrary phase between the output FEC parity bits and the inner FEC pad bits of the phase is not accounted for.
- This arbitrary phase would affect the path data delay values.
- Almost negligible, if my math is correct.

SuggestedRemedy
3 possible ways to address:
a. Impose a phase relationship between the RS FEC code word boundaries and the inner FEC pad bits, which would mean large-scale changes to the draft.
b. Specify (in clause 90, perhaps) that the path data delay contribution through the inner FEC sublayer shall be strictly additive to the path data delay contribution through the PCS and PMA layers.
c. Ignore. Based on 90A.7, the effect here is small enough not to address specifically.
"Whether the potential delay difference between the aggregated delay and the sum of the individual function delays is small enough to satisfy the timing requirements is up to the individual application."
I prefer option (c). It should not be necessary to add specific text or impose new logical rules to the Inner FEC pad bits to address a potential 12ps path data delay impairment.

Proposed Response  Response Status  W
PROPOSED REJECT.
The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting. https://www.ieee802.org/3/dj/public/24_05/he_3dj_01a_2405.pdf
It appeared that there was no consensus to make any related changes to the draft.

Cl 177  SC 177.4.6  P254  L44  # 64

Slavick, Jeff  Broadcom

Comment Type  T  Comment Status  D  pad insertion (bucket)

The last paragraph describing options for how the pad insertion could be done is unnecessary. The requirement that it occurs every 8704 CW and follows the Figure 177-6 is sufficient.

SuggestedRemedy
Remove the last paragraph of 177.4.6

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 177  SC 177.4.6  P254  L44  # 64

Huber, Thomas  Nokia

Comment Type  T  Comment Status  D  pad insertion (bucket)

The last paragraph on p254 is not necessary - implementations are always free to do things in different orders, as long as the end result matches the specified behavior.

SuggestedRemedy
Delete the paragraph.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 177  SC 177.4.6  P255  L49  # 397

Galan, Jose Vicente  Maxlinear Inc

Comment Type  T  Comment Status  D  pad insertion (bucket)

It is not declared when the first pad insertion should happen.

SuggestedRemedy
Indicate in the text that the first pad insertion will happen right at the beginning of CWs, same as in the test vectors.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
This subclause is confusing and seems to be prescribing a specific implementation. The goal of the process is to find codeword boundaries and remove the pad. If we simply reverse the processes of the tx, this process would (in a logical sense) be performed on the interleaved stream, and would search for the (interleaved) FS pattern.

**Suggested Remedy**
Rewrite the text to describe searching for the FS pattern and finding it at the expected interval.

**Proposed Response**
PROPOSED REJECT.
The comment does not provide sufficient justification to support the suggested remedy.
The existing text is consistent with the adopted baseline.

**Suggested Remedy**
Consider adding a figure illustrating how the position of the 1 bit-pair of skew determines the Inner FEC flow number.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggestion remedy with editorial license.

**Suggested Remedy**
A contribution with more details will be provided.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting: https://www.ieee802.org/3/dj/public/24_05/brown_3dj_05a_2405.pdf.
Implement slides 7, 9 and 10 with editorial license.
Cl 177  SC 177.5.3.1  P257  L45  # 393
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D  Inner FEC decode (bucket)
Defining how a miscorrected codeword can occur could be phrased more clearly.

Suggested Remedy

Change:
ôNote that for soft-decision decoded Inner FEC codewords, when there is more than one bit error in a codeword, there is always a non-zero chance that miscorrection could happen.ô
To:
ôNote that when there is more than one bit error in a codeword there is a chance that the soft decision decoder could miscorrect the codeword.ô

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 177  SC 177.6.2.1  P258  L52  # 392
Slavick, Jeff  Broadcom
Comment Type  T  Comment Status  D  Inner FEC Sync (bucket)
Counters automatically have a _done variable created for them, so no need to define fc_cnt_done

Suggested Remedy

Remove fc_cnt_done definition

Proposed Response  Response Status  W
PROPOSED ACCEPT.

Cl 177  SC 177.6.2.3  P260  L3  # 175
Ramesh, Sridhar  Maxlinear Inc
Comment Type  TR  Comment Status  D  counters (bucket)
Add a counter for uncorrectable codewords (detected with additional one bit parity)

Suggested Remedy

uncorr_cw_cnt
Counts the number of inner FEC codewords considered uncorrectable by inner FEC decoder

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 183.

Cl 177A  SC 177A  P643  L5  # 606
Maki, Jeffery  Juniper Networks
Comment Type  T  Comment Status  D  (bucket)
Annex title unnecessarily uses the acronym IMDD. Not clear what purpose is achieved that cannot be achieved simply by omitting the use of the acronym IMDD.

Suggested Remedy
Delete the acronym IMDD.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Change title to “Test vectors for 200GBASE-R, 400GBASE-R, 800GBASE-R, and 1.6TBASE-R Inner FEC”

Cl 178  SC 178.1  P268  L45  # 564
Healey, Adam  Broadcom Inc.
Comment Type  T  Comment Status  D  (bucket)
The Annex 176A control function is required and should be included in Table 178-1 (as is done in Table 179-1).

Suggested Remedy

Add "176A - Control" as "Required" in Tables 178-1, 178-2, 178-3, and 178-4.

Proposed Response  Response Status  W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Healey, Adam
Broadcom Inc.

Comment Type: T  Comment Status: D

The reference to 179.8.9 seems inappropriate here since that subclause contains cross-references specific to the Clause 179.

Suggested Remedy
Replicate the content of 179.8.9 here, replacing references to Clause 179 electrical requirements to the corresponding references in Clause 178.

Proposed Response:PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Simms, William
NVIDIA

Comment Type: T  Comment Status: D

SCMR may need to be relaxed for 200Gb/s. Measure of 15dB full band at TP0v given full band Vcm noise of 80mVpp at TP2.

Suggested Remedy
Likely need to tighten 80mV Vcm in table 179-7 for 200Gb/s

Proposed Response:PROPOSED REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not a valid request.

Li, Tobey
MediaTek

Comment Type: TR  Comment Status: D

"The test channel COM, calculated per items 3) through 7) in 93C.2, is at least 3 dB"

The reference to the test channel COM is wrong.

Suggested Remedy
Change it to "The test channel COM, calculated per item e) through h) in 178.9.3.3, is at least 3 dB" to be correct

Proposed Response:PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

**Suggested Remedy**
Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

**Proposed Response**
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

---

**Comment Type:** T  **Comment Status:** D  **Comment:** COM pkg tau (bucket)

In Table 178-12, the transmision line parameters for the "Class B package model" do not match the adopted baseline proposal li_3dj_01a_2311 slide 9.

**Suggested Remedy**
Replace the characteristic impedance for stage 1 with 92 Ohms, and the length/characterstic impedances for stage 2 through 4 with 70 Ohms/1 mm, 80 Ohm/1 mm, and 100 Ohm/0.5 mm respectively. Similarly in Table 179-15 and Table 176D-6.

**Proposed Response**
PROPOSED ACCEPT.

---

**Comment Type:** T  **Comment Status:** D  **Comment:** COM ref pkg (bucket)

In Table 178-12, the transmission line parameters for the "Class B package model" do not match the adopted baseline proposal li_3dj_01a_2311.

**Suggested Remedy**
Replace the characteristic impedance for stage 1 with 92 Ohms, and the length/characterstic impedances for stage 2 through 4 with 70 Ohms/1 mm, 80 Ohm/1 mm, and 100 Ohm/0.5 mm respectively. Similarly in Table 179-15 and Table 176D-6.

**Proposed Response**
PROPOSED ACCEPT.
|----|----|---|---|---|---------------|---------------|---------|------------------|----------------|-----------------|----------------|----------------|-----------------|-----------------|----------------|-----------------|----------------|----------------|-----------------|----------------|
Our way of measuring jitter doesn't work well enough with the increased max host loss over 3ck. It is not clear that it can or should be fixed. Our way of defining SNDR doesn't work correctly over host loss either. This can be fixed, but "vertical and horizontal noise" act together to degrade BER: more of one goes with less of the other.

Suggested Remedy
Delete the SNDR and jitter specs. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.

Proposed Response Response Status: W
PROPOSED REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not valid.
In addition, the comment includes a claim that measurements are not feasible, which is not substantiated and is contrasted by existing contributions, e.g. https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf.

Measuring jitter separately to other impairments relies on a better slew rate to noise ratio than we have at the observation point, and better than what is needed to make good links.

Suggested Remedy
Delete the jitter section. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.

Proposed Response Response Status: W
PROPOSED REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy. A question or call to action is not valid.
In addition, the comment includes a claim that measurements are not feasible, which is not substantiated and is contrasted by existing contributions, e.g. https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf.

Note that the importance of controlling jitter separately from other impairment has been addressed in https://www.ieee802.org/3/dj/public/24_05/ran_3dj_03_2405.pdf.

Nominal characteristic impedance of the cable assembly is "100-ohm"

Contributions to the task force have demonstrated the nominal characteristic impedance of the cable assembly is ~92-ohm

Suggested Remedy
Contributions to the task force have demonstrated the nominal characteristic impedance of the cable assembly is ~92-ohm.

Proposed Response Response Status: W
PROPOSED ACCEPT IN PRINCIPLE.
It is understood that the suggested remedy is to change the nominal impedance from 100 to 92 Ohm.
However, as noted in comment #216, there is no need to specify a nominal impedance.
Resolve with using the response to comment #216.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type**: T
**Comment Status**: D
**Nominal impedance (bucket)**

There is no test method or definition for the nominal characteristic impedance of the cable assembly. The components (eg paddle card, twinax) within a cable assembly may have different nominal characteristic impedances. There is no need to specify the nominal characteristic impedance of the cable assembly, since the performance of the cable assembly is determined by cl 179.11.2-7.

**Suggested Remedy**

Remove "The nominal characteristic impedance of the cable assembly is 100 ohms"

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

It is important to define the reference impedance for return loss specifications etc., but as the comment correctly suggests, there is no need to specify a nominal value.

Implement the suggested remedy.

---

**Comment Type**: T
**Comment Status**: D
**Nominal impedance (bucket)**

"Nominal impedance" is something for a datasheet not a spec. If someone wants to build a cable assembly with 95 ohm bulk cable and it passes the spec - that's OK.

**Suggested Remedy**

Delete "The nominal differential characteristic impedance of the cable assembly is 100 [ohm]". Move the one remaining sentence into 179.11.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Resolve the response to comment #216.

---

**Comment Type**: T
**Comment Status**: D
**ERL (bucket)**

ERL requirement for cable assembly that have COM less than "4dB".

**Suggested Remedy**

Change "4dB" to "TBD". Historical precedent may not be relevant for this specification.

**Proposed Response**

PROPOSED REJECT.

The comment does not provide sufficient justification to support the suggested remedy.

Note that any content of the draft can be changed if there is consensus, but changing from a number to TBD does not move us forward.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Cl 179A SC 179A.2 P662 L6710 # 56
Mellitz, Richard Samtec
Comment Type TR Comment Status D 93B (bucket)
Reference to a diagram with TP0d and TP5d is required.

SuggestedRemedy
Add TP0d and TP5d to figure 93B-1 and table 93B-1.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Annex 93B is irrelevant for CR.
Also, Annex 93B is not referenced anywhere in the draft, nor in previous backplane PMD clauses 163 and 137.
A diagram with the new test points exists in Figure 179–2 and can be referenced instead.
Add a reference in 179A.2 to Figure 179-2. Implement with editorial license.

Cl 179B SC 179B.1 P669 L17 # 223
Noujeim, Leesa Google
Comment Type T Comment Status D HCB and MCB (bucket)
Missing reference to Module compliance at TP1 and TP4.

SuggestedRemedy
Add "Module measurements for Modules specified in Annex 176E are made at TP1 and TP4 with test fixtures as specified in 179B.3."

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Insert the sentence:
Module measurements for modules specified in Annex 176E are made at module compliance points TP1 and TP4 (see Figure 176E–4) with test fixtures as specified in 179B.3.

Cl 179B SC 179B.4.6 P676 L26 # 224
Noujeim, Leesa Google
Comment Type T Comment Status D HCB and MCB (bucket)
SFPxxx is unclear.

SuggestedRemedy
Replace "The SFPxxx mated test fixture" with "The single-lane mated test fixture".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
In 179B replace SFPxxx with SFP112.

Cl 179B SC 179B.4.26 P676 L41 # 59
Mellitz, Richard Samtec
Comment Type TR Comment Status D HCB and MCB (bucket)
At least the symbol rate is known.

SuggestedRemedy
Set fb to 106.25 GBd.

Proposed Response Response Status W
PROPOSED ACCEPT.
MDIs are mechanical entities. For 106.25 GBd operation, there are SFP2 (SFF-TA-1031) and QSFP2 (SFF-TA-1027). Any "SFP224" would be an SFP2 module or cable end with 200G-capable circuitry. But this annex is for the MDI, not the circuitry. Similarly for "QSFP224" and QSFP2.

Suggested Remedy

Correct the names. Add references to SFF-TA-1011 which relates the names and specs for the SNIA-SFF modules, and SFF-8665, which defines the components of a QSFPx "solution".

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

There was broad consensus to use names of MDI types (part of baseline proposal) currently in the draft as follows: SFP224, SFP-DD224, QSFP224, QSFP-DD1600, OSFP1600.

Resolve using the response to comment #506, which addresses the normative references.

Comment Type: TR/technical required
Comment Status: A/accepted
几率: 680 P680 L15 #525

Suggested Remedy

Refer to the specification for each connector type where each is first mentioned.

See another comment against 1.3 for the reference docs.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #506.

Comment Type: T/technical
Comment Status: A/accepted
几率: 688 P688 L17 #525

Suggested Remedy

This says "the mechanical interface". The mechanical spec is SFF-TA-1027, QSFP2. It is a standard, not an MSA.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #506.

Comment Type: T/technical
Comment Status: A/accepted
几率: 688 P688 L35 #527

Suggested Remedy

Change "the TBD MSA" to "SFF-TA-1027".

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Resolve using the response to comment #506.

Comment Type: TR/technical required
Comment Status: A/accepted
几率: 350 P350 L13 #160

Suggested Remedy

It should be 'L2'.

Proposed Response

PROPOSED ACCEPT IN PRINCIPLE.

Implement with editorial license and discretion.
521

Cl 180 SC 180.10 P 368 L 11 # 521
Dawe, Piers
Nvidia
Comment Type T Comment Status D Bit number should match number of lanes
Suggested Remedy
Change 1.9.4 to 1.9.n. Below, change 1.10.4 to 1.10.n. Similarly in other clauses.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 181 SC 181.1 P 372 L 16 # 4
Johnson, John
Broadcom
Comment Type T Comment Status D Bit number (bucket)
Suggested Remedy
The PHY bracket in Figure 181-1 is shown encompassing the MDI layer, which isn't consistent with previous PMDs.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 181 SC 181.8.5 P 386 L 41 # 4
Johnson, John
Broadcom
Comment Type T Comment Status D Reference (bucket)
Suggested Remedy
The TDECOQ methods reference channel requirements in 121.8.5.2 instead of the channel requirements in local clause 181.8.5.1.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl 182 SC 182.1 P 392 L 44 # 392
Maki, Jeffery
Juniper Networks
Comment Type TR Comment Status D IMDD acronym (bucket)
Suggested Remedy
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 182 SC 182.1 P 393 L 29 # 393
Maki, Jeffery
Juniper Networks
Comment Type TR Comment Status D IMDD acronym (bucket)
Suggested Remedy
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.
Proposed Response Response Status W
PROPOSED ACCEPT.

Cl 182 SC 182.1 P 394 L 23 # 393
Maki, Jeffery
Juniper Networks
Comment Type TR Comment Status D IMDD acronym (bucket)
Suggested Remedy
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.
Proposed Response Response Status W
PROPOSED ACCEPT.
<table>
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<tr>
<th>Cl 182</th>
<th>SC 182.1</th>
<th>P 394</th>
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<td>The PHY bracket in Figure 182-1 does not encompass the PMD layer, which isn't consistent with previous PMDs.</td>
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<td>Suggested Remedy</td>
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<td>Lengthen the PHY bracket to include the PMD layer.</td>
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<td>Implement the suggested remedy with editorial license.</td>
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<td>Delete the acronym IMDD.</td>
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<th>SC 184.1.1</th>
<th>P 441</th>
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<td>General (Bucket)</td>
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<tr>
<td>The Inner FEC as defined, includes the PMA. Shall make this clear to the reader</td>
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<td>Suggested Remedy</td>
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<td>Either add sentence: “This Inner FEC sublayer includes functionality often associated with the PMA sublayer”, or split the PMA function</td>
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<td>PROPOSED ACCEPT IN PRINCIPLE.</td>
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<tr>
<td>Implement the following with editorial license.</td>
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<tr>
<td>Add sentence: “This Inner FEC sublayer includes functionality often associated with the PMA sublayer at the PMD service interface”.</td>
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<td>Add similar text to the appropriate sub clause in clause 177</td>
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<tr>
<td>[Editor's note: CC 184, 177]</td>
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<td>Huber, Thomas</td>
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<td>General (Bucket)</td>
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<td>Other diagrams of this type do not have dashed boxes around the transmit and received processes.</td>
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<td>Suggested Remedy</td>
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<tr>
<td>For consistency with the rest of the document, remove the dashed boxes</td>
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<td>Proposed Response</td>
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<td>Response Status</td>
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<tr>
<td>PROPOSED REJECT.</td>
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<tr>
<td>The dashed boxes clearly denote the transmit and receive functions. Removing the dashed boxes does not improve clarity of the draft.</td>
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The second sentence of the paragraph (discussing the distribution to 32 lanes by the permutation function) seems to imply that the 32 lanes were interleaved into a serial stream after they were reordered and deskewed, but the text doesn't actually say that is done.

Suggested Remedy
If the intent is that the 32 lanes are re-interleaved, and then the permutation function distributes the symbols back to 32 lanes (in something other than a round-robin manner), change the end of the first sentence to say "are ordered, deskewed, and serialized." If the intent is that the permutation process just moves symbols around among the 32 lanes, change the second sentence to say "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function."

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change "The RS-FEC symbols are then distributed over the 32 lanes by a permutation function." to "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function."

Comment Type: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
Comment Status: D/dispatched A/accepted R/rejected
RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Clause, Subclause, page, line

The Inner FEC transmit (184.4) and receive (184.5) functions provide a BCH encoder/decoder and other functions to be performed on each PCS lane. Although there is one per PCS lane, these should be called "flows" rather than "lanes" to be consistent with other FEC clauses and to differentiate between "lanes" that go between sublayers.

Suggested Remedy
When describing the process applied to each PCS lane in each direction, use the word "flow" rather than "lane".

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

What is the purpose of this mapping? There are 32 lanes being received; this process is simply aligning them based on the RS FEC frame, so it doesn't seem like a mapping is needed.

Suggested Remedy
Either explain why this mapping process is needed, or delete it.

Proposed Response
PROPOSED ACCEPT IN PRINCIPLE.
Add text to explain the purpose of this mapping.
Implement with editorial license.
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

178

Brown, Matt
Alphawave Semi

Comment Type T  Comment Status D  Functional (Bucket)

The process provided in 184.4.1 "Alignment lock and deskew" merely maps bits on the FEC service interface to vectors; it does not include and RS-FEC symbol alignment. The process in 184.4.2 remaps the vectors such that there is alignment to the RS-FEC symbols and the lanes are properly ordered.

SuggestedRemedy
Either combine the two subclauses and process into one subclause or move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

300

Loewenthal, Arnon
alphawave semi

Comment Type T  Comment Status D  Reorder (Bucket)

Need to further define the lanes reorder requirement. For now it is defined as optional. In practice full lanes reorder is optional, but partial reorder, meaning having flow-0 on lanes 0-15 and flow-1 on lanes 16-31 is required. Not doing that would impact end to end FEC performance and margins.

SuggestedRemedy
Two options:
1. remove the word 'optional' from line 22.
2. Define the restriction of having flow-0 on lanes 0-15 and flow-1 on lanes 16-31.

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "If that is the case, the optional lane reorder function shall order the PCS lanes according to the PCS lane number." to: "The lane reorder function shall order the PCS lanes according to the PCS lane number."

92

Huber, Thomas
Nokia

Comment Type T  Comment Status D  Reorder (Bucket)

It is not clear why this description is needed. Other clauses about reordering don't have this.

SuggestedRemedy
Delete the last paragraph

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #178
This figure is not clear, nor is the relationship of the figure to the pseudocode beneath it. I think the columns 0-3 are just numbers that relate to the post-FEC distribution process. I have no idea why there are 32 sets of 4 symbols, as the algorithm doesn’t do anything on a four-symbol basis. The function is simply reversing flow1 and flow0 every two columns, so that each lane has interleaved symbols from all four codewords. This could be described more simply by using blocks of 16 symbols in the figure (i.e., block 0 would be lanes 0-15 in column 0, block 1 would be lanes 16-31 in column 0, etc.).

Suggested Remedy
Revising the figure as suggested. The input side would look like this (where each row here is corresponding to 16 PCS lanes in the figure):

| 0 2 4 6 |
| 1 3 5 7 |
and the output would be

| 0 2 5 7 |
| 1 3 4 6 |

This will remove any confusion about whether the 32 blocks are supposed to be somehow related to the 32 PCS lanes, and it will be easier to see what is changing between the figures.

Proposed Response: Revising the suggested figure with editorial license.

---

The algorithm is unnecessarily complex. There is no need for bit-level detail since the operation is performed on 10-bit symbols - though really it seems to be performed on 160-bit entities. Per figure 184-3, it's essentially receiving as input alternating sets of 160 bits from flow0 and flow1, and changing the order from 0, 1, 0, 0, 1, 0, 1, 0 to 0, 1, 0, 1, 0, 0, 1, 0.

Suggested Remedy
A minimal change would be to state that the algorithm operates on 10-bit symbols, delete the for jà loop and its terminator, and replace “10i+j” with “I” in the statement that describes the permutation.

Another option would be to rewrite the description around the 160-bit entities as described, and perhaps also change the figure to show those instead of 40-bit entities (which as noted in a previous comment seem to have no relevance to this process, or to the convolutional interleaver process that follows it).

Proposed Response: Revising the algorithm as suggested with editorial license.
Since the convolutional interleaver operates separately on each PCS lane, there's no value in having an algorithm that includes the PCS lanes. Since it operates on 40-bit units, there's also no need to include bit-level description.

**Suggested Remedy**
State that the algorithm describes the operation on the 40 bit entities and is run on each PCS lane independently. This allows elimination of the p and j variables.

**Proposed Response**

**Response Status:** W

- PROPOSED REJECT.
- This is correct as written.
- Removing the lanes and bits does not seem to add clarity, better have the detailed function as described in the adopted baseline.

The first statement should not be a 'shall' (which indicates a PICS item of conformance).

**Proposed Response**

**Response Status:** W

- PROPOSED ACCEPT IN PRINCIPLE.
- Implement the following with editorial license .
- Change: "The BCH encoder shall work in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. There are 32 BCH encoder functions." to: "The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

**Proposed Response**

**Response Status:** W

- PROPOSED ACCEPT IN PRINCIPLE.
- Implement with editorial license .
- Change: "The BCH encoder shall work in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. There are 32 BCH encoder functions." to: "The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

**Proposed Response**

**Response Status:** W

- PROPOSED ACCEPT IN PRINCIPLE.
- Implement with editorial license .
- Change: "The BCH encoder shall work in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. There are 32 BCH encoder functions." to: "The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

**Proposed Response**

**Response Status:** W

- PROPOSED ACCEPT IN PRINCIPLE.
- Implement with editorial license .
The DSP frame should probably be a level 3 clause of its own, rather than a sub-clause under BCH interleaver.

Suggested Remedy
Change to a level 3 heading

PROPOSED ACCEPT IN PRINCIPLE.
The "BCH interleaver" function includes the pilot insertion. Change clause 184.4.7 title to: "BCH interleaver and pilot insertion"
Implement with editorial license.

It is said "4-bit pilot symbols (PS) are inserted every 64 4-bit blocks (one 4-bit PS, 63 4-bit message blocks)."
But in Figure 184-5, message blocks m<0:63>, m<64:127>, etc., between pilot symbols has 64 4-bit blocks.

Suggested Remedy
Change Figure to match the text, i.e., change m<0:63> to m<0:62>, change m<64:127> to m<63:125>, etc.

PROPOSED ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

The first sentence of the second paragraph could be written more clearly.

Suggested Remedy
Replace with "Two streams of DSP frames, one for each polarization, are generated by the inner FEC."

PROPOSED ACCEPT.

It is not clear what "192 bits that are complemented with zeros" is intended to mean.
Based on what is in Table 184-2, I think the intent is that a zero is inserted after each bit of the PRBS9 output to form the bit-pairs that become the PS symbols. Also, the text talks about 4-bit PS symbols, but Table 184-2 is showing bit-pairs for each component rather than 4-bit symbols without explaining that outputs 0 and 1 are for the X polarization (so the X PRBS is spread across outputs 0 and 1) and outputs 2 and 3 are for the Y polarization.

Suggested Remedy
Revise the two paragraphs above Table 184-1 to read as follows:
For both DSP frame_0 and DSP frame_1, the generator is initialized using the seed at the start of every DSP frame. The generator produces a sequence of 192 bits. A zero bit inserted after each bit to generate the bit-pairs that form the pilot symbols, which use the outer points of the 16QAM constellation.
The generator polynomial and seed values are shown in Figure 184-6 and listed in Table 184-1. The complete pilot sequence is shown in Table 184-2. The bit-pairs for the X polarization are distributed in a round-robin manner to outputs 0 and 1. The bit-pairs for the Y polarization are distributed in a round-robin manner to outputs 2 and 3.

PROPOSED ACCEPT.

The editor's note suggesting that the mapping to analog signals probably belongs in the PMD clause seems to make sense, in which case this clause is really not "DP-16QAM mapping", it's really just mapping to 4-level signals, which the PMD will then turn into DP-16QAM.

Suggested Remedy
Change the title to "4-level signal mapper", and make the corresponding change in 184.5.3.

PROPOSED ACCEPT IN PRINCIPLE.
After the first sentence of subclause 184.4.9 add: "This four-level signals are used by the 800GBASE-LR1 PMD to generate a single optical DP-16QAM signal with orthogonal polarizations (see 185.4.2)."
Implement with editorial license.
The overall flow would be improved if it went BCH interleaver, 4-level signal mapping, DSP frame, with all the pilot symbol details then in the DSP frame clause.

**Suggested Remedy**
Revise so the flow is like this:
184.4.7 BCH interleaver
184.4.8 Four-level signal mapping (current 184.4.9, without subclauses)
184.4.9 DSP frame generation (current 184.4.7.1)
184.4.9.1 Pilot sequence (current 184.4.7.2 and 184.4.9.1)

**Proposed Response**

The text is correct as written. The actual order is the right one. It describes the bit blocks generation and handling, then the mapping to four levels.

The paragraph that begins with "the signals Rx_XI, Rx_XQ, à" doesn't seem to make sense. The Tx and Rx signals are not guaranteed to be the same (i.e., Tx_XI can be received as any of the four components), but the contents of Tx_XI aren't distributed to all the Rx signals.

**Suggested Remedy**
Revise to say: The signals Rx_XI, Rx_XQ, Rx_XI, and Rx_XQ each represent one of the corresponding Tx_XI, Tx_XQ, Tx_XI, Tx_XQ signals from the transmitting PMD. The association between Tx and Rx components is arbitrary (e.g., Rx_XI can be any of the 4 Tx components).

**Proposed Response**

Similar changes should be made in the convolutional de-interleaver as were requested for the convolutional interleaver in earlier comments.

**Suggested Remedy**
Revise the items in the lettered list and the algorithm to align with whatever changes are agreed for the convolutional interleaver.

**Proposed Response**

Set TBD values of N and M.

**Proposed Response**

The LOCK_INIT state in Figure 184û9 'DSP lock state diagram' includes the action 'test_sym <= false', however the test_sym variable isn't defined in subclause 184.6.2 'Variables' and isn't used anywhere else in Figure 184û9.

It seems that this should have been 'test_ps <= false' as the test_ps variable isn't initialised during reset in the LOCK_INIT state but used to control the GET_SYMBOL to FIND_1ST transition below.

**Suggested Remedy**
Change 'test_sym <= false' to read 'test_ps <= false'.

**Proposed Response**

Set N=12, M=8. See contribution bruckman_3dj_01_241205

**Proposed Response**

The following presentation (referenced in the suggested remedy) was reviewed by the 802.3dj task force at the May Interim meeting: https://www.ieee802.org/3/dj/public/24_05/bruckman_3dj_01a_2405.pdf Implement the suggested remedy with editorial license.

**Proposed Response**

The LOCK_INIT state in Figure 184û9 'DSP lock state diagram' includes the action 'test_sym <= false', however the test_sym variable isn't defined in subclause 184.6.2 'Variables' and isn't used anywhere else in Figure 184û9.

It seems that this should have been 'test_ps <= false' as the test_ps variable isn't initialised during reset in the LOCK_INIT state but used to control the GET_SYMBOL to FIND_1ST transition below.

**Suggested Remedy**
Change 'test_sym <= false' to read 'test_ps <= false'.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Table 185-1, Figure 185-1, Figure 185-2 does not reflect the PHY type and clause correlation in Table 169-3a. There is no mention of 800GBASE-R BM-PMA, 800GAU-I8 2C2, 800GAUI-8 C2M, 800GBASE SM-PMA, 800GAUI-4 C2C, and 800GAUI-4 C2M.


**Suggested Remedy**

Clause 185 needs to be updated to reflect these layers.

Table 185-1 needs the following entries -
- 800GBASE-R BM-PMA - conditional
- 800GAU-I8 2C2 - optional
- 800GAUI-8 C2M - optional
- 800GBASE SM-PMA - conditional
- 800GAUI-4 C2C - optional
- 800GAUI-4 C2M - optional

Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M".

Figure 185-1 should include a PMA sublayer in the diagram and be added to legend below Figure 185-2 needs to be updated to show the 800GBASE-R PMA Sublayer and service interface between the PCS and Inner FEC.

**Proposed Response**

PROPOSED ACCEPT IN PRINCIPLE.

Some optional and conditional sublayers are missing from Table 185-1 and the conditions for include the SM-PMA and BM-PMA should be included in this table.

Regarding Figure 185-1 and Figure 185-2, no PMA is shown because the 800GBASE-LR1 Inner FEC sublayer connects directly with the PCS; a PMA is not required between the PCS and the 800GBASE-LR1 Inner FEC. Note that the 800GBASE-LR1 Inner FEC subsumes some functions/services normally provided by a PMA for the PMD.

Add the following rows in Table 185-1:
- 800GBASE-R BM-PMA - conditional
- 800GAU-I8 2C2 - optional
- 800GAUI-8 C2M - optional
- 800GBASE SM-PMA - conditional
- 800GAUI-4 C2C - optional
- 800GAUI-4 C2M - optional

Resolve the concern about conditional SM-PMA and BM-PMA related to Table 185-1 using the response to comment #317.

Implement with editorial license.

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**Comment Type: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general**

**COMMENT STATUS: D/dispatched  A/accepted  R/rejected**

**RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn**

**SORT ORDER: Clause, Subclause, page, line**
**Comment Type**: T  
**Comment Status**: D

**Comment**: Planting the seed for when the PCS is ready to be properly reviewed.

How to calculate the path data delay across the ER1 PCS/PMA? Clause 90 and Annex 90A give general rules, like how to calculate the rx/tx path data delay when there are functions within the PHY that introduce cyclical delay.

But the path data delay in the ER1 PCS is very different from anything that has been imagined in Clause 90 - an Ethernet stream that floats within a GMP frame will present unique challenges; it is not immediately clear how to determine the min/max latency across such a PCS.

This might be worse than the Alignment marker issue!

**Suggested Remedy**

**Proposed Response**: PROPOSED REJECT.

The suggested remedy does not provide sufficient detail to implement.