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<th>L</th>
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<th>Comment Status</th>
<th>Comment</th>
<th>Suggested Remedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
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</table>
| 180 | 180.8.5 | 364 | 23  |    | T            | X             | 1     | 121.8.5.2 Table 121-11 specifies ORL of 21.4dB be applied for TX testing. For 200GBASE-DR1, this needs to be 15.1dB. | Add a new exception to the list in 180.8.5: 
"- The optical return loss is as given in Table 180-6." | O               |
| 181 | 181.8.5 | 386 | 41  |    | T            | X             | 1     | The TDECQ methods reference channel requirements in 121.8.5.2 instead of the channel requirements in local clause 181.8.5.1. | Replace the reference to 121.8.5.2 with reference to 181.8.5.1. | O               |
| 182 | 182.8.5 | 411 | 30  |    | T            | X             | 1     | 121.8.5.2 Table 121-11 specifies ORL of 21.4dB be applied for TX testing. For 200GBASE-FR1, this needs to be 17.1dB. | Add a new exception to the list in 182.8.5: 
"- The optical return loss is as given in Table 182-7." | O               |
<p>| 181 | 181.1  | 372 | 16  |    | T            | X             | 1     | The PHY bracket in Figure 181-1 is shown encompassing the MDI layer, which isn't consistent with previous PMDs. | Shorten the PHY bracket to exclude the MDI layer. | O               |
| 182 | 182.1  | 395 | 21  |    | T            | X             | 1     | The PHY bracket in Figure 182-1 does not encompass the PMD layer, which isn't consistent with previous PMDs. | Lengthen the PHY bracket to include the PMD layer. | O               |
| 181 | 181.6.1 | 378 | 13  |    | T            | X             | 1     | Total average launch power (max) in Table 181-5 is TBD for 800GBASE-FR4-500. | Replace TBD with a value equal to the Average launch power, each lane (max) + 6 dB, which is 4.9 + 6 = 10.9 dB. This methodology is consistent with previous FR4 PMDs (clauses 122, 151). | O               |</p>
<table>
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<td>7</td>
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<td>Cl 183 SC 183.6.1 P425 L16</td>
<td>Total average launch power (max) in Table 183-6 is TBD for 800GBASE-FR4.</td>
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<tr>
<td>8</td>
<td>T</td>
<td>X</td>
<td>Cl 181 SC 181.6.1 P378 L23</td>
<td>Difference in launch power between any two lanes (OMAouter) (max) in Table 181-5 is TBD for 800GBASE-FR4-500.</td>
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<tr>
<td>9</td>
<td>T</td>
<td>X</td>
<td>Cl 183 SC 183.6.1 P425 L28</td>
<td>Difference in launch power between any two lanes (OMAouter) (max) in Table 183-6 is TBD for 800GBASE-FR4.</td>
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<tr>
<td>10</td>
<td>T</td>
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<td>Cl 181 SC 181.6.2 P380 L21</td>
<td>Difference in receive power between any two lanes (OMAouter) (max) in Table 181-6 is TBD for 800GBASE-FR4-500.</td>
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<td>11</td>
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<td>Cl 183 SC 183.6.2 P427 L21</td>
<td>Difference in receive power between any two lanes (OMAouter) (max) in Table 183-7 is TBD for 800GBASE-FR4.</td>
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<td>12</td>
<td>T</td>
<td>X</td>
<td>Cl 183 SC 183.6.1 P425 L24</td>
<td>The TX must be compliant over the full range of fiber length (dispersion), so the use of TDECQ alone is insufficient to determine Outer Optical Modulation Amplitude (OMAouter), each lane (min) in Table 183-6 for 800GBASE-FR4/FR4.</td>
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<td>P365</td>
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<td>183.8.11</td>
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</table>
The current method for optimizing the tap weights of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: “The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration”. Note that the MMSE optimization method is used in almost all TDECQ measurements performed today.

Suggested Remedy
Add the following text at line 36 (end of exceptions list): The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration.

Proposed Response Response Status O
The current method for optimizing the tap weights of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: "The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration". Note that the MMSE optimization method is used in almost all TDECQ measurements performed today.

Suggested Remedy
Add the following text at line 44 (end of exceptions list): The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration.
### Proposed Response

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<td>Broadcom</td>
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<td>This section only mentions that the inner FEC decoder is soft-decision decoder and the details implementation is beyond the scope of this standard. However, shall we specify the soft-decision decoder's performance bound? If not, the optical PMD BER target or link budget might be missed.</td>
<td></td>
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<td><strong>Suggested Remedy</strong></td>
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<tr>
<td>To specify the soft-decision decoder shall provide TBD dB (say 2dB) coding gain over end-end FEC provided that the error statistics are sufficiently random.</td>
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<td>Table 178-4 &quot;120F-1.6TGAUI-16 C2C’</td>
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<td>change to “120F-1.6TAUI-16 C2C’</td>
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<tr>
<td>adjust SNDR with loss correction factor which is about 1 dB based on prior assumptions</td>
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<td><strong>Suggested Remedy</strong></td>
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<tr>
<td>change SNDR to 33.5 dB.</td>
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**Comment Type** TR  **Comment Status** X  
Scale ERL parameter form 0.3ck

**Suggested Remedy**
- In Table 178-7 change TBD’s as follows:
  - $T_{r} = 0.005$ ns
  - $\beta_x = 0$ GHz
  - $\rho_x = 0.618$
  - $N = 400$ UI

**Response Status** O

---

**Comment Type** TR  **Comment Status** X  
Scale ERL parameter form 0.3ck

**Suggested Remedy**
- In Table 163-7 change TBD’s as follows:
  - $T_{r} = 0.005$ ns
  - $\beta_x = 0$ GHz
  - $\rho_x = 0.618$
  - $N = 400$ UI

**Response Status** O

---

**Comment Type** TR  **Comment Status** X  
The baud rate has doubled from .3ck. If loading is scaled down with the baud rate, the physical setting time would remain unchanged. Adjust $N_v$ and $D_p$ accordingly.

**Suggested Remedy**
- Change $N_v = $ TBD to $N_v = 400$

**Response Status** O

---

**Comment Type** TR  **Comment Status** X  
The Bessel-Thomson filter should track $f_r$ which between 0.5 and 0.6 has been shown in presentations.

**Suggested Remedy**
- Change TBD to 67 GHz

**Response Status** O

---

**Comment Type** TR  **Comment Status** X  
Use 3 dB as minimum COM as in .3ck or

**Suggested Remedy**
- Change TBD to 3 (same in 178.10.1 line 28)

**Response Status** O
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<td>X</td>
<td>Reference is wrong and Ildd should reflect tp0d to tp05d.</td>
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<td>35</td>
<td>TR/technical required</td>
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<td>Add a note to explain. S parameter can utilize any R0. For computation purposes s-parameters are converted to 50 ohms which is the native impedance for the most common test equipment.</td>
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<td>36</td>
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<td>It is not clear the power sources have significantly changed from 0.3ck and to avoid the complication of small voltage requirement from packages use the 0.3ck voltages.</td>
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<tr>
<td>37</td>
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<td>X</td>
<td>Presentations so far have not shown the need for Tx FFE. Change to no TxFFE until further data is provided. Rx noise may suggest a need for the TxFFE which would improve performance. It's not clear from a channel perspective that the TX FFE is not a zero sum gain compared to the Rx noise loss of COM. Until Rx FFE noise is better defined zero out TxFFE.</td>
<td></td>
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<tr>
<td>38</td>
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<td>It is not clear the power sources have significantly changed from 0.3ck and to avoid the complication of small voltage requirement from packages use the 0.3ck voltages.</td>
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<tr>
<td>39</td>
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<td>TR</td>
<td>X</td>
<td>Presentations so far have used fr of 0.5, 0.55, 0.58, and 0.6. 67 GHz limits on test equipment and cabling/connector modal physics suggest at least a 9 dB loss is required for good measurements at 67 GHz. Set fr to 0.6 or lower to achieve this.</td>
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<td>change TBD to 40 dB</td>
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<td>SNR_TX can be SNDR when loss correction is employed</td>
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<tr>
<td>Change TBD to 33.5 dB</td>
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<tr>
<td>Selecting values the “Receiver discrete-time equalizer parameters” are critical for making progress. Many presentations a have shown quite a variation. Select values based on what seems consistent or use straw ballot to determine.</td>
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<td><strong>Suggested Remedy</strong></td>
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<td>use straw polls from the following</td>
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<td>bmax(1) = 0.5 0.75 0.85</td>
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<td>bmin(1)= 0 -0.5 -0.75 -0.85</td>
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<td>scale ERL parameter form 0.3ck</td>
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<td>in table 178-14 change TBD's as follows</td>
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<tr>
<td>Tr 0.005 ns</td>
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<tr>
<td>βx 0 GHz</td>
<td></td>
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<tr>
<td>px 0.618</td>
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<tr>
<td>N 7000 UI</td>
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<td>The baud rate has doubled from .3ck,. If loading is scaled down with the baud rate, the physical setting time would remain unchanged. Adjust Np and Dp accordingly.</td>
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<td>Change Np from 200 to 400. change Dp from 4 to 8.</td>
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<tr>
<td>SNDR reduces with loss and used that way for equation 178A–18.</td>
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<td><strong>Suggested Remedy</strong></td>
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<td>Insert a subsection e) Loss correction factor for fitted pulse measurements. See presentation</td>
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<td><strong>Comment Status</strong>: X</td>
<td>SNDR reduces with loss and used that way for equation 178A–18.</td>
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<td>Tr 0.005 ns</td>
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<td>βx 0 GHz</td>
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<td>N 1600 UI</td>
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<td>The COM values need to be set to make progress. Until a more comprehensive proposal is presented use what is in 0.3ck and many other prior standards</td>
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<td>Set COM to 3 dB</td>
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<td>The data rate was doubled and cable length was scaled by a factor of 2 from .3ck. Adjust ERL parameters accordingly</td>
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<td>In table 179-14 change TBD's as follows</td>
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<td>Tr 0.005 ns</td>
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<td></td>
<td>βx 0 GHz</td>
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<td>N 4500 UI</td>
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</table>
**EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment**

**Comment Type: TR, Comment Status: X**

(Table 179–15): Computation can be independent of R0. Add a note to explain. s-parameter can utilize any R0. For computation purposes s-parameters are converted to 50 ohms which is the native impedance for the most common test equipment.

**Suggested Remedy**

Change R0 for TBD to 50 ohms and add a note indicating the imported s-parameter are to be converted into 50 ohm reference before computation.

**Proposed Response**

Response Status: O

**Comment Type: TR, Comment Status: X**

(Table 179–16) Presentations so far have used fr of 0.5, 0.55, 0.58, and 0.6. 67 Ghz limits on test equipment and cabling/connector modal physics suggest at least a 9 dB loss is required for good measurements at 67 GHz. Set fr to 0.6 or lower to achieve this.

**Suggested Remedy**

change TBD to 0.6.

**Proposed Response**

Response Status: O

**Comment Type: TR, Comment Status: X**

Reference to a diagram with TP0d and TP5d is required.

**Suggested Remedy**

Add TP0d and TP5d to figure 93B-1 and table 93B-1.

**Proposed Response**

Response Status: O

**Comment Type: TR, Comment Status: X**

Refence to a diagram with TP0d and TP5d is required.

**Suggested Remedy**

Add TP0d and TP5d to figure 93B-1 and table 93B-1.

**Proposed Response**

Response Status: O
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<tr>
<td>179B</td>
<td>179B.4.2</td>
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<td>The ERL parameter form 0.3ck should be changed as follows: Tr 0.005 ns, βx 0 GHz, ρx 0.618, N 1600 UI, Tlx 0, tw 1, DER0 2e-5.</td>
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<tr>
<td>176A</td>
<td>176A.4</td>
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<td>It would be better to have the existing patterns the same as for previous clause 136.</td>
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<tr>
<td>176D</td>
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<td>T</td>
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<td>The electrical specifications of C2C components are not equivalent to those of the corresponding PMD’s isn’t helpful. What does “not equivalent” mean? Which corresponding PMD’s?</td>
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### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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<td>An insertion loss of only 20dB is less than desirable and the equation is TBD. We shouldn't specify the loss at this time</td>
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<td>The note &quot;The electrical specifications of C2C components are not equivalent to those of the corresponding PMD's. Specifically the test points at which module compliance is defined are different isn't helpful. What does &quot;not equivalent&quot; mean?. Which corresponding PMD's? Although the module test points are different those for the host are the same as Clause 179.</td>
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<td>Delete the note.</td>
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<td>There shouldn't be any Tx parameters in a specification for a reference receiver.</td>
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<td>Delete the rows for transmitter termination resistance, transmitter equalizer coefficients, transmitter differential peak output voltage, transition time, transmitter signal to noise ratio, RLM,</td>
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<tr>
<td>Table 116-1 and Table 116-2 include the 200Gb/s per lane PMDs which require the symbol muxing PMA. This bit muxing PMA would only be used for lower speed AUls. Saying it supports any of the PMDs in the tables is confusing.</td>
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<td>SuggestedRemedy</td>
<td>Change to &quot;The 200GBASE-R PMA(s) can support any of the two, or four lane 200Gb/s PMDs in Table116–1 and the 400GBASE-R PMA(s) can support any of the four, or 8 lane 400Gb/s PMDs in Table 116–2&quot;. As a less preferred approach PMDs could be changed to PHYs in the original sentence and an additional sentence could be added saying &quot;The single lane 200Gb/s PMDs in Table 116-1 and the two lane 400Gb/s in table 115-2 require the symbol-muxing PMAs described in clause 176.&quot;</td>
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<tr>
<td>Clause 176 is for the symbol mux PMA it should not be used for Annex 120F</td>
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<tr>
<td>There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500, 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4,</td>
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<td>SuggestedRemedy</td>
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</table>
There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500. 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4.

Suggested Remedy:
Delete the offending "M"s

In Table 179-16, Use the COM parameter values from https://www.ieee802.org/3/dj/public/24_01/healey_3dj_01_2401.pdf slide 18, which are:

- \( f_r = 0.58 \)
- \( c(-3) = 0 \)
- \( c(-2) = 0 \)
- \( c(-1) = 0 \)
- \( c(0) = 1 \)
- \( c(1) = 0 \)
- \( A_v = 0.413 \)
- \( A_{fe} = 0.413 \)
- \( A_{ne} = 0.45 \)
- \( \eta_0 = 6e^{-9} \)
- \( SNR_{TX} = 33 \)
- \( A_{DD} = 0.02 \)
- \( R_{LM} = 0.95 \)
- \( d_w = 5 \)
- \( N_{fix} = 10 \)
- \( N_g = 0 \)
- \( N_f = 0 \)
- \( N_{max} = 0 \)
- \( b_{max}(1) = 0.85 \)
- \( b_{min}(1) = 0 \)

Additionally, set MLSE = 0 (not enabled)

**Suggested Remedy**

In table 178-13, use the COM parameter values from https://www.ieee802.org/3/dj/public/24_01/healey_3dj_01_2401.pdf slide 18, which are:

- \( f_r = 0.58 \)
- \( c(-3) = 0 \)
- \( c(-2) = 0 \)
- \( c(-1) = 0 \)
- \( c(0) = 1 \)
- \( c(1) = 0 \)
- \( A_v = 0.413 \)
- \( A_{fe} = 0.413 \)
- \( A_{ne} = 0.45 \)
- \( \eta_0 = 6 \times 10^{-9} \)
- \( SNR_{TX} = 33 \)
- \( \sigma_{RJ} = 0.01 \)
- \( A_{DD} = 0.02 \)
- \( R_{LM} = 0.95 \)
- \( d_w = 5 \)
- \( N_{fix} = 10 \)
- \( N_g = 0 \)
- \( b_{max}(1) = 0.85 \)
- \( b_{min}(1) = 0 \)

Additionally, set MLSE = 0 (not enabled).

**Proposed Response**

**Response Status**: O
Proposed Response

# 73

Cl 176E SC 176E.4.1 P632 L6 # 73

Lusted, Kent Intel Corporation

Comment Type TR Comment Status X

The IL_dd for AUI C2M channel is a TBD

SuggestedRemedy

Set IL_dd = 33 per https://www.ieee802.org/3/dj/public/24_01/lusted_3dj_03_2401.pdf

Proposed Response Response Status O

---

# 74

Cl 1 SC 1.5 P51 L11 # 74

Lusted, Kent Intel Corporation

Comment Type TR Comment Status X

The abbreviation "MLSD" is used numerous times in Annex 178A to reference Maximum Likelihood Sequence Detection and should be added to the abbreviations list.

SuggestedRemedy

Add MLSD | Maximum Likelihood Sequence Detection

Proposed Response Response Status O

---

# 75

Cl 30 SC 20.3.2.1.3 P53 L21 # 75

Huber, Thomas Nokia

Comment Type T Comment Status X

There should also be an entry for 800GBASE-ER1 since it is a different PCS

SuggestedRemedy

Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R (or before the entry for 800GBASE-R).

Proposed Response Response Status O

---

# 76

Cl 169 SC 169.1.3 P116 L43 # 76

Huber, Thomas Nokia

Comment Type T Comment Status X

The descriptions of 800GBASE-ER1-20 and 800GBASE-ER1 should refer to 800GBASE-ER1 encoding rather than 800GBASE-R encoding since the ER1-20 PCS is distinct from the 800GBASE-R PCS

SuggestedRemedy

Change 800GBASE-R to 800GBASE-ER1 in the last two rows of the table.

Proposed Response Response Status O

---

# 77

Cl 169 SC 169.1.4 P119 L20 # 77

Huber, Thomas Nokia

Comment Type T Comment Status X

The 800GXS can contain AUIs - so the C2C and C2M clauses should be marked as optional for the ER1 and ER1-20 PHYs, as should the associated PMAs.

SuggestedRemedy

Indicate that 800GBASE-R BM-PMA, 800GAUI-8 C2C, 800GAUI-8 C2M, 800GBASE-R SM-PMA, 800GAUI-4 C2C, and 800GAUI-4 C2M are optional for both ER1 and ER1-20 PHYs.

Proposed Response Response Status O

---

# 78

Cl 169 SC 169.3.2 P122 L35 # 78

Huber, Thomas Nokia

Comment Type T Comment Status X

A similar diagram is needed for 800GBASE-ER1 and 800GBASE-ER1-20 PHYs.

SuggestedRemedy

Use figure 169-2b as a basis. Replace 800GBASE-R PCS with 800GBASE-ER1 PCS, 800GBASE-LR1 Inner FEC with 800GBASE-ER1 PMD, and 800GBASE-R PMD with 800GBASE-ER1 PMD (and of course renams all the service interfaces to align with that).

Proposed Response Response Status O
In tables 171-3 and 171-5, it is not clear what has changed in the rows that are shown.

**Suggested Remedy**
- Indicate the changes with revision marks.

**Proposed Response**
- Response Status: O

The 800G 32:4 PMA, 400G 16:2 PMA and the 200G 8:1 PMA are basically the same, other than the numbers of lanes. The 1.6T 16:8 is different since it has 40b deskew and 4-symbol interleaving. All of the PMAs with the same number of lanes on both sides are essentially the same. It would simplify maintenance and likely reader understanding as well if the number of lanes were parameterized as m and n.

**Suggested Remedy**
- Reorganize 176.5 through 176.8 into 3 clauses: one for 200/400/800 m:n PMAs, one for 1.6T m:n PMAs, and one for 200/400/800/1.6T m:m PMAs, and use a single set of text and figures with the parameters m and n for the number of lanes. Include a table showing PHY rates and the values of m and n (e.g. with columns PHY, m, and n, and rows 200GBASE-R, 8, 1; 400GBASE-R, 16, 2; etc.).

**Proposed Response**
- Response Status: O

Indicating PAM4 decoding as optional seems a bit misleading. The P{MD isn't doing soft-decoding in any case, so the FEC must do some sort of decoding to recover the bits from the PAM4 symbols.

**Suggested Remedy**
- Generalize the label in the box to "Decoding", and explain in the text in 177.5.x that there are multiple options for decoding.

**Proposed Response**
- Response Status: O

The last paragraph on p254 is not necessary - implementations are always free to do things in different orders, as long as the end result matches the specified behavior.

**Suggested Remedy**
- Delete the paragraph.
According to figure 177-2, the first process the receiver performs is PAM4 decoding (or soft-decision decoding).

**Suggested Remedy**

Add a subclause for the decoding process.

**Proposed Response**

Response Status: O

This subclause is confusing and seems to be prescribing a specific implementation. The goal of the process is to find codeword boundaries and remove the pad. If we simply reverse the processes of the tx, this process would (in a logical sense) be performed on the interleaved stream, and would search for the (interelaved) FS pattern.

**Suggested Remedy**

Rewrite the text to describe searching for the FS pattern and finding it at the expected interval.

**Proposed Response**

Response Status: O

Other diagrams of this type do not have dashed boxes around the transmit and received processes.

**Suggested Remedy**

For consistency with the rest of the document, remove the dashed boxes.

**Proposed Response**

Response Status: O
**Comment ID 91**

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**Proposed Response**

**Huber, Thomas**

**Nokia**

**Comment Type** T  
**Comment Status** X

Lane reordering is not optional; the lanes have to be put in the correct order. If they happen to arrive in the correct order, it’s a simple process.

**Suggested Remedy**

Change the second sentence to say “The lane reorder process shall order the PCS lanes according to the PCS lane number.”

**Comment Status** X

**Response Status** O

---

**Comment ID 92**

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**Proposed Response**

**Huber, Thomas**

**Nokia**

**Comment Type** T  
**Comment Status** X

It is not clear why this description is needed. Other clauses about reordering don’t have this.

**Suggested Remedy**

Delete the last paragraph

**Proposed Response**

**Response Status** O

---

**Comment ID 93**

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**Proposed Response**

**Huber, Thomas**

**Nokia**

**Comment Type** T  
**Comment Status** X

This figure is not clear, nor is the relationship of the figure to the pseudocode beneath it. I think the columns 0-3 are just numbers that relate to the post-FEC distribution process. I have no idea why there are 32 sets of 4 symbols, as the algorithm doesn’t do anything on a four-symbol basis. The function is simply reversing flow1 and flow0 every two columns, so that each lane has interleaved symbols from all four codewords. This could be described more simply by using blocks of 16 symbols in the figure (i.e., block 0 would be lanes 0-15 in column 0, block 1 would be lanes 16-31 in column 0, etc.).

**Suggested Remedy**

Revise the figure as suggested. The input side would look like this (where each row here is corresponding to 16 PCS lanes in the figure): 0 2 4 6 1 3 5 7

and the output would be

0 2 5 7

1 3 4 6

This will remove any confusion about whether the 32 blocks are supposed to be somehow related to the 32 PCS lanes, and it will be easier to see what is changing between the figures.

**Proposed Response**

**Response Status** O
Comment ID 94

Proposed Response

#94

Huber, Thomas
Nokia

Comment Type T
Comment Status X

The algorithm is unnecessarily complex. There is no need for bit-level detail since the operation is performed on 10-bit symbols - though really it seems to be performed on 160-bit entities. Per figure 184-3, it's essentially receiving as input alternating sets of 160 bits from flow0 and flow1, and changing the order from 0, 1, 0, 1, 0, 1, 0, 1 to 0, 1, 0, 1, 1, 0, 1, 0.

SuggestedRemedy

A minimal change would be to state that the algorithm operates on 10-bit symbols, delete the for j… loop and its terminator, and replace "10i+j" with "I" in the statement that describes the permutation.

Another option would be to rewrite the description around the 160-bit entities as described, and perhaps also change the figure to show those instead of 40-bit entities (which as noted in a previous comment seem to have no relevance to this process, or to the convolutional interleaver process that follows it).

Comment Status X
Response Status O

Proposed Response Response Status O

Comment ID 95

Proposed Response

#95

Huber, Thomas
Nokia

Comment Type T
Comment Status X

The description of the convolutional interleaver process could be improved. The variable i is used in the first part of the subclause as an index for the delay lines and as an indication of time within a sequence. Then at the bottom of page 447 it's used a symbol index.

SuggestedRemedy

Revise the list above the figure to read as follows, eliminating the overloading of the index i and improving the clarity a bit (and change the figure to label the lines as b=0, b=1, b=2):

a) The input and output switches are always aligned to the same row b, where b = 0 to 2
b) A block of 40 bits is read from row b
c) The contents of row b are shifted to the right by 40 bits
d) A block of 40 bits is written to row b
e) The switch position is updated to (b+1) mod 3

Comment Status X
Response Status O

Proposed Response Response Status O

Comment ID 96

Proposed Response

#96

Huber, Thomas
Nokia

Comment Type T
Comment Status X

Since the convolutional interleaver operates separately on each PCS lane, there's no value in having an algorithm that includes the PCS lanes. Since it operates on 40-bit units, there's also no need to include bit-level description.

SuggestedRemedy

State that the algorithm describes the operation on the 40 bit entities and is run on each PCS lane independently. This allows elimination of the p and j variables.

Completion Status X
Response Status O

Proposed Response Response Status O

Comment ID 97

Proposed Response

#97

Huber, Thomas
Nokia

Comment Type T
Comment Status X

The algorithm relating the convolutional interleaver output to its input doesn't work when i<36 - it refers to negative block numbers for the input (permo) while the delay lines are filling, and those negative numbers need to be ignored as the process starts up. In other words, given the input sequence of 40-bit blocks 0, 1, 2, 3, …, the convolutional interleaver is supposed to produce the output sequence 0, 3, 6, 9, 12, 15, 18, 21, 4, 24, 7, 27, 10, 30, 13, 33, 16, then 36, 19, 2, and then each successive set of 3 is 3 more than the previous (so it continues 39, 22, 5, 42, 25, 8, …). The algorithm says that output 0 is input 0-18 x (0 mod 3), so that produces 0 as expected, but output 1 is then supposed to be input 1-18 x (1 mod 3), which is -17, not 3.

SuggestedRemedy

The text above figure 184-4 already provides an algorithmic description of how the interleaver works. Rather than a second algorithmic description, it might be better to show the worked example as noted in the comment - i.e., show a table of input blocks from 0 to 42, and the corresponding output blocks.

Proposed Response Response Status O
The first statement should not be a 'shall' (which indicates a PICS item of conformance). The second sentence is correct, in that there are 32 encoders, but what's actually required is that each lane has an encoder.

**Suggested Remedy**

Revised the paragraph to read: The BCH encoder works in conjunction with the RS(544,514) FEC to increase the FEC coding gain. There is a BCH encoder process for each PCS lane.

**Proposed Response**

Response Status: O

---

The variable p is being overloaded - it is used at line 35 as a lane index, and at line 40 as the parity polynomial. Since the BCH encoding is done per lane, there is really no need to have a variable related to the lane number. The text can simply state that the algorithm is applied to each lane individually.

**Suggested Remedy**

Change the line above the dashed list to say: “The BCH encoding is done separately on each lane. The encoding of each BCH codeword \( u \) is defined as follows:

At the top of page 449, remove the ‘for p…’ loop from the pseudocode.

**Proposed Response**

Response Status: O

---

Cl 184 SC 184.4.6 P449 L16 # 100

Huber, Thomas Nokia

**Comment Type** T **Comment Status** X

Clarify that the circular shift is applied per lane.

**Suggested Remedy**

Make similar changes to what was suggested in previous sections - remove the unnecessary variable p and associated for loop in the pseudocode, and add a sentence stating that the circular shift process is performed on each lane individually.

**Proposed Response**

Response Status: O
It is not clear what “192 bits that are complemented with zeros” is intended to mean. Based on what is in Table 184-2, I think the intent is that a zero is inserted after each bit of the PRBS9 output to form the bit-pairs that become the PS symbols. Also, the text talks about 4-bit PS symbols, but Table 184-2 is showing bit-pairs for each component rather than 4-bit symbols without explaining that outputs 0 and 1 are for the X polarization (so the X PRBS is spread across outputs 0 and 1) and outputs 2 and 3 are for the Y polarization.

**Proposed Remedy**

Revise the two paragraphs above table 184-1 to read as follows:

For both DSP frame_0 and DSP frame_1, the generator is initialized using the seed at the start of every DSP frame. The generator produces a sequence of 192 bits. A zero bit inserted after each bit to generate the bit-pairs that form the pilot symbols, which use the outer points of the 16QAM constellation.

The generator polynomial and seed values are shown in Figure 184-6 and listed in Table 184-1. The complete pilot sequence is shown in Table 184-2. The bit-pairs for the X polarization are distributed in a round-robin manner to outputs 0 and 1. The bit-pairs for the Y polarization are distributed in a round-robin manner to outputs 2 and 3.

The overall flow would be improved if it went BCH interleaver, 4-level signal mapping, DSP frame, with all the pilot symbol details then in the DSP frame clause.

**Proposed Remedy**

Revise so the flow is like this:

184.4.7 BCH interleaver
184.4.8 Four-level signal mapping (current 184.4.9, without subclauses)
184.4.9 DSP frame generation (current 184.4.7.1)
184.4.9.1 Pilot sequence (current 184.4.7.2 and 184.4.8.1)

The editor's note suggesting that the mapping to analog signals probably belongs in the PMD clause seems to make sense, in which case this clause is really not "DP-16QAM mapping", it's really just mapping to 4-level signals, which the PMD will then turn into DP-16QAM.

**Proposed Remedy**

Change the title to "4-level signal mapper", and make the corresponding change in 184.5.3.

The paragraph that begins with "the signals Rx_XI, Rx_XQ, …" doesn't seem to make sense. The Tx and Rx signals are not guaranteed to be the same (i.e., Tx_XI can be received as any of the four components), but the contents of Tx_XI aren't distributed to all the Rx signals.

**Proposed Remedy**

Revise to say: The signals Rx_XI, Rx_XQ, Rx_YI, and Rx_YQ each represent one of the corresponding Tx_XI, Tx_XQ, Tx_YI, Tx_YQ signals from the transmitting PMD. The association between Tx and Rx components is arbitrary (e.g., Rx_XI can be any of the 4 Tx components).

Similar changes should be made in the convolutional de-interleaver as were requested for the convolutional interleaver in earlier comments.

**Proposed Remedy**

Revise the items in the lettered list and the algorithm to align with whatever changes are agreed for the convolutional interleaver.
**Proposed Response**

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Huber, Thomas  
Nokia  

**Comment Type**  
The baseline for the 800GBASE-ER1[-20] PCS has issues with PTP accuracy when an extender sublayer is used.  
**Suggested Remedy**  
Update the baseline per presentations in the May meeting proposing a mechanism to reduce the PTP inaccuracy.

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Huber, Thomas  
Nokia  

**Comment Type**  
The ppm value for this PMD should be 20 ppm  
**Suggested Remedy**  
Replace TBD with 20

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Huber, Thomas  
Nokia  

**Comment Type**  
The ppm value for this PMD should be 20 ppm  
**Suggested Remedy**  
Replace TBD with 20

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Huber, Thomas  
Nokia  

**Comment Type**  
Since 800GBASE-ER1 and -ER1-20 have a separate PCS, the definition for 800GBASE-ER1 and ER1-20 should refer to 800GBASE-ER1 encoding rather than 800GBASE-R encoding  
**Suggested Remedy**  
Change 800GBASE-R to 800GBASE-ER1 for both the ER1 and ER1-20 definitions.

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Huber, Thomas  
Nokia  

**Comment Type**  
There should also be an entry for 800GBASE-ER1 since it is a different PCS  
**Suggested Remedy**  
Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R,(or before the entry for 800GBASE-R).

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Stassar, Peter  
Huawei Technologies  

**Comment Type**  
Currently reference is made to compliance channel in 121.8.5.2, which is for 500m instead of 2km  
**Suggested Remedy**  
Create new subclause 182.8.5.1 and refer to it instead of 121.8.5.2. Create 182.5.2.1 with contents along the lines of 124.8.5.1 from 802.3df with the same compliance channel.  
**Develop with editorial license**
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Stassar, Peter Huawei Technologies

**Comment Type**: T **Comment Status**: X

The TBDs need to be replaced by values. Follow the same methodology as in 154 and latest draft D3.0 of P802.3cw

**Suggested Remedy**

Replace contents by The sum of the transmit and receive delays at one end of the link contributed by the 800GBASE-LR1 PMD including 2 m of fiber in one direction shall be no more than 16 384 bit times (32 pause_quanta or 20.48 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

**Response Status**: O

---

Stassar, Peter Huawei Technologies

**Comment Type**: T **Comment Status**: X

Previously for Clause 154 and draft Clause 156 in D3.0 for P802.3cw 20 dB maximum receiver reflectance has been used, which is a common value in the industry and in draft Clause 155.5.2

**Suggested Remedy**

For Receiver reflectance (max) replace TBD by 20 dB for both ER1-20 and ER1

**Response Status**: O

---

Sakai, Toshiaki Socionext

**Comment Type**: T **Comment Status**: X

**Comment Type**: T **Comment Status**: X

In "Table 178–12" class A package model Transmission line parameter τ(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Suggested Remedy**

Change τ(tau) value in Table 178-12 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.

**Response Status**: O

---

Sakai, Toshiaki Socionext

**Comment Type**: T **Comment Status**: X

In "Table 178–12" class B package model Transmission line parameter τ(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Suggested Remedy**

Change τ(tau) value in Table 178-12 (class B package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.

**Response Status**: O

---

**Comment ID**: 119 Page 24 of 118

**TYPE**: TR/technical required **ER/editorial required** **GR/general required** **T/technical** **E/editorial** **G/general**

**COMMENT STATUS**: D/dispatched A/accepted R/rejected **RESPONSE STATUS**: O/open W-written C/closed Z/withdrawn

**SORT ORDER**: Comment ID

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In "Table 179–15" class A package model Transmission line parameter \( \tau(tau) \) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Suggested Remedy**

- Change \( \tau(tau) \) value in Table 179-15 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
- Or simply delete this row, as the \( \tau(tau) \) value in table 93A-3 is 6.141e-3 ns/mm.

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<th>Comment ID</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>123</td>
<td>T</td>
<td>X</td>
<td>COM reference package parameter value. (transmission line parameter tau)</td>
<td>O</td>
</tr>
</tbody>
</table>

In "Table 176D–6" class A package model Transmission line parameter \( \tau(tau) \) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

**Suggested Remedy**

- Change \( \tau(tau) \) value in Table 176D-6 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
- Or simply delete this row, as the \( \tau(tau) \) value in table 93A-3 is 6.141e-3 ns/mm.
### Transmitter signal measurement filter bandwidth description.

"Unless specified otherwise, transmitter signal measurements are made for each lane separately using a fourth-order Bessel-Thomson low-pass response with 3 dB bandwidth of 40 GHz, with AC-coupled connection from TP2 to the test equipment."

The 4th-BW filter BW should be "TBD GHz", the same as for CL178.9.2, AN176D.3.3 and AN176E.3.3, as the Nyquist frequency of the signal is 53.125GHz and 40GHz is too low.

**Suggested Remedy**

- Change 40GHz to TBD GHz.

**Proposed Response**

Response Status: O

### Clause 183.7.1

Clause 183.7.1 is TBD.

**Suggested Remedy**

- Use the same text and table as given in 182.7.1. Since this sub-clause only reiterates fiber cable specs from external standards, not 802.3 specific specs, this should not be controversial.

**Proposed Response**

Response Status: O

### Clause 183.7.2

Clause 183.7.2 is TBD.

**Suggested Remedy**

- Use the same text as given in 182.7.2. "An optical fiber connection, as shown in Figure 183–7, consists of a mated pair of optical connectors." Since this is a basic definition of terms, it should not be controversial.

**Proposed Response**

Response Status: O
<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>176E</td>
<td>176E.2</td>
<td>Loss budgets are TBD</td>
<td>See Ghiasi C2M May-24 Contribution for background on the numbers</td>
<td></td>
</tr>
<tr>
<td>176E</td>
<td>176E.3</td>
<td>Loss is TBD</td>
<td>Given that number of module plug implementation will have COC or even if there is</td>
<td></td>
</tr>
<tr>
<td>176E</td>
<td>176E.4</td>
<td>Eye height and VEC are TBD</td>
<td>Given that number of module plug implementation will have COC or even if there is</td>
<td></td>
</tr>
<tr>
<td>176E</td>
<td>176E.5</td>
<td>Eye opening reference receiver parameters will be different between TP1d and TP4a measurement</td>
<td>Given that number of module plug implementation will have COC or even if there is</td>
<td></td>
</tr>
</tbody>
</table>

**Comment #130**

**Proposed Response**

- Loss budgets are TBD
- See Ghiasi C2M May-24 Contribution for background on the numbers
- I<sub>IIDD</sub>=28 dB
- Connector with one via = 3 dB
- Module I<sub>IIDD</sub> = 3.6 dB
- Host I<sub>IIDD</sub>=21.4 dB

**Response Status**

- O

**Comment #131**

**Proposed Response**

- 3 dB BW is TBD
- Propose to use 0.55*Baudrate=58.4375 GHz but in current OCM code we use Butterworth, should the COM for C2M be changed to BT4 filter?

**Response Status**

- O

**Comment #132**

**Proposed Response**

- Eye height and VEC are TBD
- See Ghiasi C2M May-24 Contribution for background on the numbers
- VEC=10.7 dB
- VEO=8 mV

**Response Status**

- O

**Comment #133**

**Proposed Response**

- BW is TBD
- Propose to use 0.55*Baudrate=58.4375 GHz

**Response Status**

- O

**Comment #134**

**Proposed Response**

- Loss is TBD
- See Ghiasi C2M May-24 Contribution for background on the numbers
- Bump-bump Insertion loss at Nyquist frequency (53.125 GHz) is less than or equal to 28 dB

**Response Status**

- O

**Comment #135**

**Proposed Response**

- Eye opening reference receiver parameters will be different between TP1d and TP4a measurement
- Given that number of module plug implementation will have COC or even if there is package it will be core-less ~8 mm so there is no need to add package after HCB given the loss of the HCB and plug boards are similar.
- At TP4a this is just the output of the module should be tested with synthetic
- short trace
- long trace
- recommendation is to measure at the ASIC ball otherwise we would need at least 2 test cases with Package A and 2 with Package B

**Response Status**

- O
<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>TP1d and TP4a measurement should be done without device model with just 50 scope termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device model - NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single ended transmitter termination - NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single ended reference resistance - 50 ohms</td>
</tr>
</tbody>
</table>

**Suggested Remedy**

- Propose Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>Single ended receive termination and receive 3 dB BW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Single ended receive termination is the 50 ohm scope termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Receive 3 dB BW=0.55*106.25=58.4375 GHz</td>
</tr>
</tbody>
</table>

**Proposed Remedy**

- Propose Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>Transmitter equalizer coefficients</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Given little benefit of TX FFE C(-3) - NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C(0)=-0.65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C(-1)=[-0.3:0.2:0 ]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C(-2)=[ 0:0.2:0.14 ]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C(1)=[-0.14:0.02:0.14 ] also goes positive to allow slowing driver for reflection mitigation</td>
</tr>
</tbody>
</table>

**Proposed Remedy**

- Propose Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>Jitter and noise parameters are TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Ghiasi C2M May-24 Contribution for background on the numbers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Eta0=1.25E-8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmitter SNR = NA for reference receiver but may use 33 dB for COM code</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmitter Sigma = NA for reference receiver but may use 0.01 UI for COM code</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmitter dual-Dirac jitter = NA for reference receiver but may use 0.02 UI for COM code</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transmitter RLM = NA for reference receiver but may use 95% for COM code</td>
</tr>
</tbody>
</table>

**Proposed Remedy**

- Propose Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>Reference equalizer is TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Propose to use fix 25 tap FFE with 1T DFE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max # of pre-cursor taps = 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DFE max tap weight = 0.75</td>
</tr>
</tbody>
</table>

**Proposed Remedy**

- Propose Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>X</td>
<td>Missing TBDs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R= 50 ohms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rdr=50 ohms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RD=50 ohms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Receiver 3 dB BW=0.55*106.25=58.4375 GHz</td>
</tr>
</tbody>
</table>

**Proposed Remedy**

- Propose Response
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>SC</th>
<th>P/L</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Suggested Remedy</th>
<th>Proposed Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>142</td>
<td>C176D</td>
<td>P605</td>
<td>T</td>
<td>X</td>
<td>Transmitter equalizer coefficients</td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>C176D</td>
<td>P605</td>
<td>T</td>
<td>X</td>
<td>C2C should be aligned with C2M and addressing TBDs</td>
<td></td>
</tr>
<tr>
<td>144</td>
<td>C176D</td>
<td>P605</td>
<td>T</td>
<td>X</td>
<td>C2C reference equalizer should be aligned with C2M and addressing TBDs</td>
<td></td>
</tr>
<tr>
<td>145</td>
<td>C181</td>
<td>P373</td>
<td>T</td>
<td>X</td>
<td>Prior to 181.4 add section for PMA function to support precoder to mitigate burst errors</td>
<td></td>
</tr>
<tr>
<td>146</td>
<td>C180</td>
<td>P349</td>
<td>T</td>
<td>X</td>
<td>Prior to 180.4 add section for PMA function to support precoder to mitigate burst errors</td>
<td></td>
</tr>
<tr>
<td>147</td>
<td>C182</td>
<td>P397</td>
<td>T</td>
<td>X</td>
<td>Prior to 182.4 add section for PMA function to support precoder to mitigate burst errors</td>
<td></td>
</tr>
</tbody>
</table>
### Comment: Prior to 183.4 add section for PMA function to support precoder to mitigate burst errors

**Suggested Remedy:**

The transmitter needs to support \(1/(1+D)\) mod 4 precoding, as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT. Without OLT, the optical transmitter should enable \(1/(1+D)\) mod 4 precoding to mitigate burst errors.

**Proposed Response:**

Response Status: O

---

### Comment: Table 73-5 is missing the indication of highest priority.

**Suggested Remedy:**

Change 1.6Tb/s 8 lane in the capability column to 1.6Tb/s 8 lane, highest priority.

**Proposed Response:**

Response Status: O

---

### Comment: In table 116-3, the last two columns, miss usage of PMD names.

**Suggested Remedy:**

Change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 200GBASE-KR1 and 200GBASE-CR1

**Proposed Response:**

Response Status: O

---

### Comment: 200GBASE-R SM PMA delay constraint is missing

**Suggested Remedy:**

Change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

**Proposed Response:**

Response Status: O

---

### Comment: In Table 116-9, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

**Suggested Remedy:**

Change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

**Proposed Response:**

Response Status: O
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment ID 154**

**Comment Type:** TR  
**Comment Status:** X

In Table 169-1, Row of 800GBASE-CR4 was described as 800Gb/s PHY using 800GBASE-R encoding over four lanes of twinaxial copper cable, which is inconsistent with the description in page 49, 1.4.184aa

**Suggested Remedy:**  
make the language consistent.

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---

**Comment ID 155**

**Comment Type:** TR  
**Comment Status:** X

same as the previous comment on 800GBASE-CR4

**Suggested Remedy:**  
make the description consistent

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---

**Comment ID 156**

**Comment Type:** TR  
**Comment Status:** X

In Table 169-3, Phy type and clause correlation was marked incorrectly for the columns of 8000GBASE-DR8 PMD and 800GBASE-DR8-2 PMD

**Suggested Remedy:**  
remove the unnecessary M in the following rows for 800GBASE-DR8 PMD: 800GBASE-D8-4, 800GBASE-FR4-50, remove the unnecessary M in the following rows for 800GBASE-DR8-2 PMD: 800GBASE-DR4-2, 800GBASE-FR4, and 800GBASE-LR4.

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---

**Comment ID 157**

**Comment Type:** TR  
**Comment Status:** X

In Table 116-6, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

**Suggested Remedy:**  
change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---

**Comment ID 158**

**Comment Type:** TR  
**Comment Status:** X

In Table 169-4, the delay constraints on 800GBASE-R BM-PMA and 800GBASE-R SM-PMA are missing

**Suggested Remedy:**  
add appropriate rows with TBD if no consensus has been built.

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---

**Comment ID 159**

**Comment Type:** TR  
**Comment Status:** X

In Table 174-4, the notes for 1.6TBASE-KR8 and 1.6TBASE-CR8 says includes the medium in one direction. No length of the medium was provided, nor any explicit delay due to the medium was provided. While In Table 169-4, a definitive of 14ns allocated for one direction through cable medium was provided for 800GBASE-CR4. One would assume 1.6TBASE-CR8 would be consistent with 800GBASE-CR4. The same problem applies to 1.6TBASE-KR8.

**Suggested Remedy:**  
Put in explicit allocation of delay constraints for the medium used in 1.6T BASE-CR8 and 1.6TBASE-KR8. Align with that of 800GBASE-CR4 and 800GBASE-KR4, if technically feasible.

**Response:** O  
**Mi, Guangcan**  
Huawei Technologies Co., Ltd

---
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>SuggestedRemedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>160</td>
<td>ER</td>
<td>X</td>
<td>A typo of 'L3' in figure 180-2, right side, 3rd channel output label.</td>
<td>It should be 'L2'.</td>
<td>O</td>
</tr>
<tr>
<td>161</td>
<td>TR</td>
<td>X</td>
<td>Power budget (for maximum TDECQ)' for 800GBASE-FR4-500 in Table 181-7 could be incorrect. It should be equal to channel IL + allocation for penalties (for maximum TDECQ).</td>
<td>Power budget (for maximum TDECQ)' in Table 181-7 should be updated to 7.4 dB</td>
<td>O</td>
</tr>
<tr>
<td>162</td>
<td>TR</td>
<td>X</td>
<td>recommend relationship between 'Tx_OMAout (min)' and 'Tx_Pavg (min)' (in Table 181–5) follow 400G FR4, with delta=3dB, assuming max. OER infinite.</td>
<td>With 'OMAout (min)’=0.8dBm, then 'Average launch power, each lane (min) ’ in Table 181–5 should be changed to -2.2dBm.</td>
<td>O</td>
</tr>
<tr>
<td>163</td>
<td>TR</td>
<td>X</td>
<td>The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' should equal to 'Channel insertion loss' (3.5dB for FR4-500)</td>
<td>Rx_Pavg (min)' in Table 181–6 should be -2.2dBm-3.5dB=-5.7dBm</td>
<td>O</td>
</tr>
<tr>
<td>164</td>
<td>TR</td>
<td>X</td>
<td>The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' should equal to 'Channel insertion loss' (4.0dB for FR4)</td>
<td>Rx_Pavg (min)' in Table 183–7 should be -2.2dBm-4.0dB=-6.2dBm</td>
<td>O</td>
</tr>
</tbody>
</table>

Yu, Rang-chen
InnoLight

Comment ID 165
Page 32 of 118

TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn
SORT ORDER: Comment ID
5/3/2024 10:09:28 AM
Cl 183 SC 183.6.1 P425 L19 # 166
Yu, Rang-chen InnoLight

Comment Type TR Comment Status X
Recommended relationship between 'Tx_OMAout (min)' and 'Tx_Pavg (min)' for 800G LR4 (in Table 183–6) should follow 400G LR4-6, with delta equal to 3dB, assuming max. OER infinite.

Suggested Remedy
With 'OMAout (min)'=1.9dBm, then 'Average launch power, each lane' for 800G LR4 in Table 183–6 should be changed to -1.1dBm.

Proposed Response Response Status O

Cl 183 SC 183.6.2 P427 L18 # 167
Yu, Rang-chen InnoLight

Comment Type TR Comment Status X
The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' for 800G LR4 should equal to 'Channel insertion loss' (6.3dB for LR4)

Suggested Remedy
Rx_Pavg (min)' for 800G LR4 in Table 183–7 should be -1.1dBm-6.3dB=-7.4dBm

Proposed Response Response Status O

Cl 183 SC 183.6.3 P429 L6 # 155
Yu, Rang-chen InnoLight

Comment Type T Comment Status X
Footnote e did not clarify what's the compisiton of total 5dB allocation for penalties.

Suggested Remedy
Recommend to add "Allocations to penalties for 800G-LR4 including penalties due to dipersion 3.9dB, DGD 0.7dB and MPI 0.4dB" to footnote e.

Proposed Response Response Status O

Cl 181 SC 181.6.3 P381 L48 # 169
Yu, Rang-chen InnoLight

Comment Type T Comment Status X
Footnote d did not clarify what's the compisiton of total 3.9dB allocation for penalties.

Suggested Remedy
Recommend to add "Allocations to penalties for 800G-FR4-500 including penalties due to dipersion 3.4dB, DGD and MPI 0.5dB" to footnote d.

Proposed Response Response Status O

Cl 180 SC 180.6.3 P356 L47 # 170
Yu, Rang-chen InnoLight

Comment Type T Comment Status X
Footnote b did not clarify what's the compisiton of total 3.5dB allocation for penalties.

Suggested Remedy
Recommend to add "Allocations to penalties for DRx series including penalties due to dipersion 3.4dB, DGD and MPI 0.1dB" to footnote b.

Proposed Response Response Status O

Cl 182 SC 182.6.3 P404 L3 # 171
Yu, Rang-chen InnoLight

Comment Type T Comment Status X
Although TDECQmax is still TBD. However, the footnote b should also indicate the allocation for penalties, just leave dispersion section as TBD for future update.

Suggested Remedy
Recommend to add "Allocations to penalties for DRx-2 series including penalties due to dipersion TBDdB, DGD and MPI 0.4dB" to footnote b.

Proposed Response Response Status O
Although TDECQmax is still TBD. However, the footnote b should also indicate the allocation for penalties, just leave dispersion section as TBD for future update.

**Comment ID: 172**

**Ramesh, Sridhar**
Maxlinear Inc

**Comment Type:** TR  **Comment Status:** X

**Suggested Remedy**
Recommend to add "Allocations to penalties for 800G-FR4 including penalties due to dispersion TBDbB, DGD and MPI 0.5dB" to footnote e.

**Proposed Response**  **Response Status:** O

---

DGDmax (in Table 181–8) probably used DGDmean=0.8ps, it should be 2.24ps refer to 802.3df DR series.

**Comment ID: 173**

**Ramesh, Sridhar**
Maxlinear Inc

**Comment Type:** TR  **Comment Status:** X

**Suggested Remedy**
Recommend change to 2.24ps

**Proposed Response**  **Response Status:** O

---

"Pad frame sequence" naming does not convey purpose in alignment. Suggest to call this field "Frame Alignment Sequence" instead.

**Comment ID: 174**

**Ramesh, Sridhar**
Maxlinear Inc

**Comment Type:** E  **Comment Status:** X

**Suggested Remedy**
Pad Frame Alignment Sequence

**Proposed Response**  **Response Status:** O

---

Table 179-12: Jitter mask extended below 40Khz and above 40MHz for completeness

**Comment ID: 177**

**Ramesh, Sridhar**
Maxlinear Inc

**Comment Type:** TR  **Comment Status:** X

**Suggested Remedy**
Case A - please amend to <= 0.04, Case F, please amend to >= 40

**Proposed Response**  **Response Status:** O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

184.4.1

Brown, Matt
Alphawave Semi

Comment Type: T  Comment Status: X

The process provided in 184.4.1 "Alignment lock and deskew" merely maps bits on the FEC service interface to vectors; it does not include and RS-FEC symbol alignment. The process in 184.4.2 remaps the vectors such that there is alignment to the RS-FEC symbols and the lanes are properly ordered.

Suggested Remedy:
Either combine the two subclauses and process into one subclause or move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

Proposed Response:  Response Status: O

184.4.2

Brown, Matt
Alphawave Semi

Comment Type: T  Comment Status: X

The lane reorder process is stated as being optional, however, that is not the case. It is not required (or optional) if the lanes are already in order (e.g., connected to a PCS above) and mandatory if the lanes may not be in order (e.g., connected to an 8:32 PMA above), thus it is conditional, rather than optional.

Suggested Remedy:
Change the first 2 sentences in 184.4.2 to "If the sublayer above the Inner FEC does not provide the PCS lanes in order at the service interface, the lane reorder function shall reorder the PCS lanes according to the PCS lane number."

Proposed Response:  Response Status: O

174.1.2

Brown, Matt
Alphawave Semi

Comment Type: T  Comment Status: X

This list of interface widths has been traditionally included in "new ethernet rate introduction" clauses since 10 Gb/s Ethernet. It seems unnecessary and present and extra burden to amend with each new interface added. The number of lanes is abundantly clear in each clause that defines and interface. The original intent was to point out that the structural detail of the specified interfaces are to be as specified while others that are not are not specified.

Suggested Remedy:
Delete the paragraph and lists from page 155 line 47 to page 156 line 12.

Proposed Response:  Response Status: O

177.5.3

Brown, Matt
Alphawave Semi

Comment Type: T  Comment Status: X

177.5.3 lists a few counter to be supported by the inner FEC. The definition for some of these could be improved. Further, additional counters should be included provides bins of error counts to help estimate quality of the link.

Suggested Remedy:
A contribution with more details will be provided.

Proposed Response:  Response Status: O
<table>
<thead>
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**Comment Type:** T  
**Comment Status:** X  
**Proposed Response**  
**Response Status:** O

Comment ID 184

The Inner FEC transmit (184.4) and receive (184.5) functions provide a BCH encoder/decoder and other functions to be performed on each PCS lane. Although there is one per PCS lane, these should be called "flows" rather than "lanes" to be consistent with other FEC clauses and to differentiate between "lanes" that go between sublayers.

**Suggested Remedy**
When describing the process applied to each PCS lane in each direction, use the word "flow" rather than "lane".

Comment Type: T  
Comment Status: X  
Proposed Response:  
Response Status: O

Comment ID 185

Many state diagrams in this draft as well as in the base standard use the operator "++" to indicate that the variable be incremented by 1. However, this operator is never defined.

**Suggested Remedy**
Import Clause 21 and... Amend 21.5 to include definition of "++.
Delete the following from state diagram conventions in multiple clauses. "The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented."

Comment Type: T  
Comment Status: X  
Proposed Response:  
Response Status: O

Comment ID 186

Host output characteristics need to be defined with consideration of the variable output settings that can result from training. This will affect the entire subclause 176E.3.3.

**Suggested Remedy**
Define the output characteristics using a methodology similar to that of transmitter specifications in 179.9.4.
Use a table similar to Table 179-7 but with different values due to the higher host channel insertion loss budget for C2M.
A detailed proposal will be provided.

Comment Type: TR  
Comment Status: X  
Proposed Response:  
Response Status: O

Comment ID 187

Module output characteristics need to be defined with consideration of the variable output settings that can result from training. This will affect the entire subclause 176E.3.4.

**Suggested Remedy**
Define the output characteristics using a methodology similar to that of transmitter specifications in 179.9.4.
Use a table similar to Table 179-7 but with different values due to the lower insertion loss assumed for the module output test.
A detailed proposal will be provided.

Comment Type: TR  
Comment Status: X  
Proposed Response:  
Response Status: O
Proposed Response

# 188

CI 176E  SC 176E.3.5  P624  L3  # 188

Ran, Adee  Cisco

Comment Type TR  Comment Status X

Host input characteristics need to be defined with consideration of the availability of training.
This will affect the entire subclause 176E.3.5.

SuggestedRemedy

Define the input characteristics using a methodology similar to that of receiver specifications in 179.9.5, with the required changes due to the lack of a cable assembly.
Use a table similar to Table 179-10 but with additional rows for DC common-mode voltage and AC common-mode voltage tolerance.

A detailed proposal will be provided.

Proposed Response  Response Status O

---

Proposed Response

# 189

CI 176E  SC 176E.3.6  P628  L26  # 189

Ran, Adee  Cisco

Comment Type TR  Comment Status X

Module input characteristics need to be defined with consideration of the availability of training.

This will affect the entire subclause 176E.3.6.

SuggestedRemedy

Define the input characteristics using a methodology similar to that of receiver specifications in 179.9.5, with the required changes due to the lack of a cable assembly and usage of MCB instead of HCB.
Use a table similar to Table 179-10 but with additional rows for DC common-mode voltage tolerance and AC common-mode voltage tolerance.

A detailed proposal will be provided.

Proposed Response  Response Status O

---

Proposed Response

# 190

CI 174A  SC 174A.3  P539  L25  # 190

Ran, Adee  Cisco

Comment Type TR  Comment Status X

174A.3 "Frame loss ratio for a Physical Layer implementation" is empty.

I assume a "Physical Layer implementation" means the path between the RS and the MDI.
It is unclear how frame loss ratio can be defined for this path, because the two interfaces are not equivalent; frames are defined only at the RS, and cannot be identified, checked for errors, or counted on the MDI. Similarly, the signals on the MDI cannot be compared to the data stream on the RS, so no other "error metric" can be defined.
This is in contrast to "RS to RS link" and other subclauses, in which such checking and counting is possible.

This subclause should be deleted.

SuggestedRemedy

Delete 174A.3.

Proposed Response  Response Status O

---

Proposed Response

# 191

CI 174A  SC 174A.4  P539  L30  # 191

Ran, Adee  Cisco

Comment Type TR  Comment Status X

174A.4 "Frame loss ratio for an xMII Extender" is empty.

Since this annex defines several performance metrics, the titles of specific subclauses should be based on the sub-link in question, while the specific requirement (FLR, BER, etc.) should preferably be in the subclause text.

SuggestedRemedy

A presentation with proposed content is planned.

Proposed Response  Response Status O

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EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment ID 192**

<table>
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<td>P539</td>
<td>36</td>
<td># 192</td>
</tr>
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</table>

Ran, Adee  
Cisco

**Comment Type** TR  
**Comment Status** X  

174A.5 "Frame loss ratio for PHY" is empty.

Since this annex defines several performance metrics, the titles of specific subclauses should be based on the sub-link in question, while the specific requirement (FLR, BER, etc.) should preferably be in the subclause text.

**Suggested Remedy**  
A presentation with proposed content is planned.

**Proposed Response**  
Response Status O

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**Comment ID 193**

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<td>P119</td>
<td>31</td>
<td># 193</td>
</tr>
</tbody>
</table>

Ran, Adee  
Cisco

**Comment Type** TR  
**Comment Status** X  

A new 800GBASE-ER1 PCS is defined in clause 186. It should be mentioned in the introduction clause, 169.2.3 ("Physical Coding Sublayer (PCS)" in 802.3df) which currently only refers to the 800GBASE-R PCS.

**Suggested Remedy**  
Bring 169.2.3 into the draft and amend it to include the clause 186 PCS.

**Proposed Response**  
Response Status O

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**Comment ID 194**

<table>
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<td>P86</td>
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</table>

Ran, Adee  
Cisco

**Comment Type** TR  
**Comment Status** X  

The existing semantics of the link_status parameter of AN_LINK.indication enables only two values, OK and FAIL. This imposes a need to bring up a link within a specified time (link_fail_inhibit_timer), otherwise AN will restart (per the Arbitration state diagram, Figure 73-11). This can cause numerous problems in a segmented link.

The AN should be tolerant to a link in which one or more of the devices is still in the process of training. This can be achieved by adding a third possible value to link_status, indicating that the negotiated PHY is still training.

**Suggested Remedy**  
A presentation with proposed content is planned.

**Proposed Response**  
Response Status O

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**Comment ID 195**

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<td>116.3.2</td>
<td>P99</td>
<td>52</td>
<td># 195</td>
</tr>
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</table>

Ran, Adee  
Cisco

**Comment Type** TR  
**Comment Status** X  

segment-by-segment training requires passing the RTS status of each device/sublayer in both directions.

When there is a physical interface with a training protocol, RTS is communicated using the protocol. But when two sublayers are attached, e.g. PMD and PMA, the status has to be communicated through the service interface.

This can be achieved if the inter-sublayer service interface includes both IS_SIGNAL.indication and IS_SIGNAL.request.

The values of the parameter SIGNAL_OK should be extended to allow communicating that a sublayer is in the process of training. A new value IN_PROGRESS would enable that.

Similar changes should be applied in clauses 169 and 174. The mapping of RTS to SIGNAL_OK should be defined in annex 176A.

**Suggested Remedy**  
A presentation with proposed content is planned.

**Proposed Response**  
Response Status O

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**Comment ID 196**

<table>
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<td>P548</td>
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<td># 196</td>
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</table>

Ran, Adee  
Cisco

**Comment Type** ER  
**Comment Status** X  

The annex title includes "Control function and start-up protocol", while in the subclauses and text there are alternative terms such as "interface control function", "Start-up protocol", and "training" (176A.9).

This mega-function requires nomenclature to describe it. It would be good to have an acronym-friendly name so that it can be included in tables of other clauses (e.g. Table 116-3, Table 179-1).

**Suggested Remedy**  
A presentation with proposed nomenclature is planned.

**Proposed Response**  
Response Status O

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<tr>
<td>197</td>
<td>ER</td>
<td>X</td>
<td>The &quot;Segment by segment training&quot; seems to be an introductory subclause that explains the purpose of the whole thing. It would help readers if this introduction is placed at the beginning of the annex. The current introduction in 176A.1 seems too brief.</td>
<td>O</td>
</tr>
<tr>
<td>198</td>
<td>ER</td>
<td>X</td>
<td>&quot;tx_symbol and rx_symbol variables&quot; do not appear in this annex. They are in fact parameters of the service interface primitives of the sublayer that implements the control function. Tie the text defining the symbols to the service interface of the sublayer.</td>
<td>O</td>
</tr>
<tr>
<td>199</td>
<td>TR</td>
<td>X</td>
<td>&quot;The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0)&quot; Some interfaces have 8 lanes. The default mapping provided in Table 176A–1 can be used instead.</td>
<td>O</td>
</tr>
</tbody>
</table>
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

Proposed Response

#200

Cl 176A  SC 176A.2.3.3  P552  L40  # 200
Ran, Adee  Cisco

Comment Type  TR  Comment Status  X

"These three variations are produced as described for the PRBS13 free-running function in 176A.2.3.2"

PRBS13 free-running is defined only with PAM4 and does not have PAM2 or PAM4+precoding variants. These variants are defined for the PRBS13 function in 176A.2.3.1, but the definition of the precoding variant includes resetting of the precoder state at the beginning of each training frame, which would be inadequate.

Suggested Remedy

Change to the following:

The initial state of the PRBS31 generator shall not be all zeros. It may be any other value.

When the training pattern selector is set to PAM4, the training pattern is generated in a similar manner to the definition in 176A.2.3.2, except that PRBS31 generator output is used instead of PRBS13 generator output.

When the training pattern selector is set to PAM2, the training pattern is generated in a similar manner to the definition in 176A.2.3.2, except that PRBS31 generator output is used instead of PRBS13 generator output, and the pair of bits {A, A} is used instead of {A, B}.

When the training pattern selector is set to PAM4 with precoding, the training pattern is generated from the PRBS31 PAM4 pattern by precoding the Gray-mapped PAM4 symbols as specified in 135.5.7.2. The precoder initial state is not specified. The state is not re-initialized or reset during generation of the training pattern.

Proposed Response  Response Status  O

Cl 176A  SC 176A.6  P557  L3  # 201
Ran, Adee  Cisco

Comment Type  TR  Comment Status  X

"When the interface control state diagram (Figure 176A–6) is in the TRAIN_LOCAL state, the device may request its link partner to..."

It is important to also note at which states requests from the link partner should be processed, and what happens in the other states - this may not be obvious.

Suggested Remedy

Insert the following paragraphs after the first one:

When the interface control state diagram is in either the TRAIN_LOCAL or TRAIN REMOTE state, the device shall respond to requests received from the link partner.

When the interface control state diagram is in any state other than TRAIN_LOCAL or TRAIN_REMOTE, the device shall not send any requests to the link partner and shall ignore requests from the link partner.

Proposed Response  Response Status  O
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**Comment Type:** TR/technical required | ER/editorial required | GR/general required | T/technical | E/editorial | G/general

**Comment Status:** D/dispatched | A/accepted | R/rejected | Response Status: O/open | W/written | C/closed | Z/withdrawn

**Commenter:** Ran, Adee | Parsons, Earl | Parsons, Earl | Shakiba, Hossein | Shakiba, Hossein | Shakiba, Hossein 

**Proposed Response:** A presentation with proposed content is planned.

**Suggested Remedy:** The maximum and minimum dispersion values in this table should be replaced by equations similar to ones found in previous clauses (i.e. Table 151-12). This method is sometimes called "CM1".

In the minimum column replace "-2.94" with "0.0115 x λ x [1-(1324/λ)^4]". In the maximum column replace "1.66" with "0.0115 x λ x [1-(1300/λ)^4]". These are the same values as in Table 151-12 with the coefficient divided by 4.

**Proposed Response:** Replace TBDs with values agreed upon by the Task Force.

The positive and negative dispersion values in this table should come from a channel model that uses a statistical approach. A contribution on fiber dispersion statistics will be submitted.

**Proposed Response:** Change reference to section 178A.1.8.1

**Suggested Remedy:** Change to h_ISI(n) = 0 for n = d+1

The factor 2/3 in equation (178A-36) is specific to PAM4. This change does not apply if the equation is rewritten. See contributions lim_3dj_02_2405.pdf and shakiba_3dj_01_2405.pdf.

**Suggested Remedy:** Change 2/3 to L/2(L-1) to make it general. Note that L=4 still yields 2/3. Please refer to contribution tbd.

**Proposed Response:** Change to h_ISI(n) = 0 for n = d+1
Proposed Response

Cl 178A SC 178A.1.11.1 P660 L33 # 212
Shakiba, Hossein Huawei Technologies Canada
Comment Type T Comment Status X
The factor 3/4 in equation (178A-37), as is or rewritten, is specific to PAM4. See contributions lim_3dj_02_2405.pdf and shakiba_3dj_01_2405.pdf.
SuggestedRemedy
Change 3/4 to (L-1)/L to make it general. Note that L=4 still yields 3/4. Please refer to contribution tbd.
Proposed Response Response Status O

Cl 178A SC 178A.11.1 P660 L52 # 213
Shakiba, Hossein Huawei Technologies Canada
Comment Type T Comment Status X
Although clear, the result of the PDF convolution conv[p(y),p(y/b1)] is a PDF and assumed to have been normalized to satisfy the PDF sum requirement.
SuggestedRemedy
Either mention that after convolution, the result should be normalized, or add a normalization coefficient of 1/b1 in font of conv.
Proposed Response Response Status O

Cl 178A SC 178A.11.1 P661 L1 # 214
Shakiba, Hossein Huawei Technologies Canada
Comment Type T Comment Status X
Although clear, the result of the PDF convolution of equation (178A-39) is a PDF and assumed to have been normalized to satisfy the PDF sum requirement.
SuggestedRemedy
Either mention that after convolution, the result should be normalized, or add a normalization coefficient of 1/(1-b1) in font of conv.
Proposed Response Response Status O

Cl 179A SC 179A.7 P668 L9 # 215
Noujeim, Leesa Google
Comment Type T Comment Status X
TP0 and TP5 are not the appropriate test points for Annex 179A COM
SuggestedRemedy
Change text to "...between TP0d and TP5d"
Proposed Response Response Status O

Cl 179A SC 179.11.1 P326 L27 # 216
Noujeim, Leesa Google
Comment Type T Comment Status X
There is no test method or definition for the nominal characteristic impedance of the cable assembly. The components (eg paddle card, twinax) within a cable assembly may have different nominal characteristic impedances. There is no need to specify the nominal characteristic impedance of the cable assembly, since the performance of the cable assembly is determined by cl 179.11.2-7.
SuggestedRemedy
Remove "The nominal characteristic impedance of the cable assembly is 100 ohms"
Proposed Response Response Status O

Cl 179A SC 179.11.2 P326 L42 # 217
Noujeim, Leesa Google
Comment Type T Comment Status X
The maximum frequency of 40GHz is is insufficient for 200Gbps/lane PAM4
SuggestedRemedy
Proposed Response Response Status O
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Proposed Response

Cl 179  SC 179.9.4.8  P315  L35  # 227
Noujeim, Leesa  Google
Comment Type  T  Comment Status  X

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns.

Suggested Remedy

Change text to “…Tx equal to twice the delay between the test fixture connector and the test fixture host-facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result”

Proposed Response  Response Status  O

Cl 179  SC 179.9.4  P309  L23  # 225
Noujeim, Leesa  Google
Comment Type  T  Comment Status  X

Adopted baseline https://www.ieee802.org/3/dj/public/24_01/ran_3dj_01a_2401.pdf has BT filter bandwidth as TBD but D1.0 has 40GHz. 3dB bandwidth of 40GHz is insufficient for 200Gbps/lane PAM4.

Suggested Remedy


Proposed Response  Response Status  O

Cl 179  SC 179.9.4.3  P314  L39  # 226
Noujeim, Leesa  Google
Comment Type  T  Comment Status  X

Nb of 6 should be increased since hosts shouldn’t be penalized for having reflections within capability of receiver to compensate; hosts in this generation should have equalization capability well beyond 6 UI.

Suggested Remedy

increase Nb to 20 (or TBD based on ref receiver capabilities)

Proposed Response  Response Status  O

Cl 179  SC 179.5  P665  L24  # 229
Noujeim, Leesa  Google
Comment Type  T  Comment Status  X

Doubling ILdd_(host+TFmax) implies both ends of the link have the same host designations.

Suggested Remedy

Replace “2*ILdd_(host+TFmax)” with "ILdd_(host+TFmax)_end1 + ILdd_(host+TFmax)_end2” or similar notation to accommodate asymmetric Link Configurations in Table 179A-3.

Proposed Response  Response Status  O
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment 231**

**Comment ID:** 231

**Li, Mike**

**Intel**

**Comment Type:** TR

**Comment Status:** X

**Comment:** 3dB BW is TBD

**Suggested Remedy:**

- Change it to 65 GHz.
- Rational, considering the common and cost effective 1.85mm connector BW, and associated ~7% measurement error, give rise to this number.

**Response:**

**Response Status:** O

**Comment 232**

**Comment ID:** 232

**Li, Mike**

**Intel**

**Comment Type:** TR

**Comment Status:** X

**Comment:** dERL (min) is TBD

**Suggested Remedy:**

- Change it to -3 dB. See lim_3dj_01_2403a.

**Response:**

**Response Status:** O

**Comment 233**

**Comment ID:** 233

**Li, Mike**

**Intel**

**Comment Type:** TR

**Comment Status:** X

**Comment:** "absolute value of step size for all taps (max)" ingreated from 802.3ck, value not suitable for 802.3dj at 200G/L, and no simod supports"

**Suggested Remedy:**

- Change it 0.02, see lim_3dj_01_2405

**Response:**

**Response Status:** O

**Comment 234**

**Comment ID:** 234

**Li, Mike**

**Intel**

**Comment Type:** TR

**Comment Status:** X

**Comment:** "value at minimum state for c(-3) (max) " from 802.3ck, parameter not suitable for 802.3dj at 200G/L, and no simod supports"

**Suggested Remedy:**

- C(-3) is not needed, delete it, see lim_3dj_01_2405

**Response:**

**Response Status:** O

**Comment 235**

**Comment ID:** 235

**Li, Mike**

**Intel**

**Comment Type:** TR

**Comment Status:** X

**Comment:** "value at max state for c(-2) (min) " from 802.3ck, parameter not suitable for 802.3dj at 200G/L, and no simod supports"

**Suggested Remedy:**

- change it to 0.16, see lim_3dj_01_2405

**Response:**

**Response Status:** O
### EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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<th>Proposed Response</th>
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**Comment Type**: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general

**Comment Status**: D/dispatched  A/accepted  R/rejected  

**Response Status**: O/open  W/written  C/closed  Z/withdrawn

**Sort Order**: Comment ID

Comment ID: 242

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<td>X</td>
<td>For Test1, replace them with IL(min): 13.5dB, Ilmax: 14.5 dB; for Test2, replace them with IL(min): 27.5dB, Ilmax: 28.5; see li_3dj_01_2311, lusted_3dj_02_2311.pdf</td>
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<td>178</td>
<td>178.9.3.3</td>
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<td>IL for Class B PKG are TBDs</td>
<td>X</td>
<td>For Test1, replace them with IL(min): 10.5dB, Ilmax: 11.5 dB; for Test2, replace them with IL(min): 21.5dB, Ilmax: 22.5; see li_3dj_01_2311, lusted_3dj_02_2311.pdf</td>
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TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn
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| 249        | 178| 178.9.3.3 | 282 | 16 | 249 | Li, Mike, Intel  
**Comment Type**: TR  
**Comment Status**: X  
**Suggested Remedy**:  
COM for test1 and test2 are TBDs  
*Proposed Response*:  
*Response Status*: O |
| 250        | 178| 178.10 | 284 | 11 | 250 | Li, Mike, Intel  
**Comment Type**: TR  
**Comment Status**: X  
**Suggested Remedy**:  
COM(min) is TBD  
*Proposed Response*:  
*Response Status*: O |
| 251        | 178| 178.10 | 284 | 12 | 251 | Li, Mike, Intel  
**Comment Type**: TR  
**Comment Status**: X  
**Suggested Remedy**:  
IL(max) is TBD  
*Proposed Response*:  
*Response Status*: O |
| 252        | 178| 178.10 | 284 | 14 | 252 | Li, Mike, Intel  
**Comment Type**: TR  
**Comment Status**: X  
**Suggested Remedy**:  
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*Proposed Response*:  
*Response Status*: O |
| 253        | 178| 178.10.1 | 284 | 28 | 253 | Li, Mike, Intel  
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**Comment Status**: X  
**Suggested Remedy**:  
COM TBD  
*Proposed Response*:  
*Response Status*: O |
| 254        | 178| 178.10.1 | 285 | 38 | 254 | Li, Mike, Intel  
**Comment Type**: TR  
**Comment Status**: X  
**Suggested Remedy**:  
Ro TBD  
*Proposed Response*:  
*Response Status*: O |
| 255        | 178| 178.10.1 | 285 | 40 | 255 | Li, Mike, Intel  
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**Suggested Remedy**:  
RD(T) TBD  
*Proposed Response*:  
*Response Status*: O |
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<th>Comment Status</th>
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<td>X</td>
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<td>178</td>
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<td>Replaced it with 0.5, see lim_3dj_01_2405, slide 5</td>
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<tr>
<td>178</td>
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<td>C(-3) not needed</td>
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**Proposed Response**

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<td>178</td>
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<td>TR</td>
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<td>Replace it with 0:0.16:0.02 (min, max, step), see lim_3dj_01_2405, slide 5</td>
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<td>178</td>
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**Proposed Response**

**Li, Mike Intel**

**Comment ID**: 261
Comment ID: 262

Li, Mike Intel

**Comment Type:** TR

**Comment Status:** X

**Suggested Remedy:**
- Replace it with -0.2.0.0.02 (min,max, step), see lim_3dj_01_2405, slide 5

Proposed Response: Response Status O

---

Comment ID: 263

Li, Mike Intel

**Comment Type:** TR

**Comment Status:** X

**Suggested Remedy:**
- g1 inherited from 802.3ck, no simod support, not appropriate
- Replace them with -15:0, 1 (min, max, step), see lim_3dj_01_2405, slide 5

Proposed Response: Response Status O

---

Comment ID: 264

Li, Mike Intel

**Comment Type:** TR

**Comment Status:** X

**Suggested Remedy:**
- g2 inherited from 802.3ck, no simod support, not appropriate
- Replace them with fb/4.223, fb/80 (fz1,fz2)

Proposed Response: Response Status O

---

Comment ID: 265

Li, Mike Intel

**Comment Type:** TR

**Comment Status:** X

**Suggested Remedy:**
- f1,fp2, fp3 from 802.3ck, no simod support, not appropriate
- Replace them with fb/1.8973, fb/2.6562, fb/80 (fp1,fp2, fp3)

Proposed Response: Response Status O

---

Comment ID: 266

Li, Mike Intel

**Comment Type:** TR

**Comment Status:** X

**Suggested Remedy:**
- Av, Afe, Ane TBDs
- Replace them with 0.413, 0.413, 0.608 V (Av, Afe, Ane)

Proposed Response: Response Status O
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<td>269</td>
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**Li, Mike**  
*Intel*

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**Comment ID** 285
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment ID 286**

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<td>Update the equation per slide 4 of lim_3dj_02_2405, see also a marked version in the support data sheet.</td>
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**Comment ID 288**

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<td><strong>Comment Type</strong> TR</td>
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<td>&quot;value at min state for c(-1) (max) &quot; from 802.3ck, parameter not suitable for 802.3dj at 200G/L, and no simod supports&quot;</td>
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**Comment ID 289**

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<td>In Figure 176-18, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols</td>
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**Comment ID 290**

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**Comment ID 291**

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#### Comment 292

**Comment ID**: 292  
**Page**: 52  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: TR  
**Comment Status**: X

The Q values of Convolutional interleaver are not in line with previous contributions, D0.1, D0.2, with the TP2 test vectors of Annex 177A and have to be corrected.

**Suggested Remedy**

- Q=24 for 1.6TBASE-R, Q=48 for 800GBASE-R, Q=96 for 400GBASE-R and Q=192 for 200GBASE-R

**Proposed Response**

Response Status: O

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**Comment 293**

**Comment ID**: 293  
**Page**: 33  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: T  
**Comment Status**: X

For Figure 176–5, it has to be explained what A'/B' shall be.

**Suggested Remedy**

Add an explanation for A'/B', e.g. "A'/B' are the symbols from previous 2 CWs that are delayed".

**Proposed Response**

Response Status: O

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**Comment 294**

**Comment ID**: 294  
**Page**: 49  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: T  
**Comment Status**: X

In all Figures in the 800G PMA section, it is referred to A'/B' symbols, although we have 4 RS CWs

**Suggested Remedy**

Change to use A,B,C,D for the 4 RS CWs, instead of A, B, A', B'

**Proposed Response**

Response Status: O

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**Comment 295**

**Comment ID**: 295  
**Page**: 53  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: T  
**Comment Status**: X

Usually, a convolutional interleaver switches round-robin from low to high delay lines and the convolutional de-interleaver switches round-robin from high to low delay lines. Why in Figure 177-3 it is defined the other way round?

**Suggested Remedy**

Change the convolutional interleaver order if that is the case.

**Proposed Response**

Response Status: O

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**Comment 296**

**Comment ID**: 296  
**Page**: 57  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: T  
**Comment Status**: X

It is not declared when the first pad insertion should happen.

**Suggested Remedy**

Indicate in the text that the first pad insertion will happen right at the beginning of CWs, same as in the test vectors.

**Proposed Response**

Response Status: O

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**Comment 297**

**Comment ID**: 297  
**Page**: 59  
**Type**: TR/technical required  
**Comment Status**: A/accepted  
**Response Status**: O/open

**Comment**

Galan, Jose Vicente  
Maxlinear Inc  

**Comment Type**: T  
**Comment Status**: X

The details of how to use the IBSF are beyond the scope of this standard. Does it mean this is vendor discretionary? Or will it be defined in other standard?

**Suggested Remedy**

Clarify in the text where the use of the IBSF will be defined.

**Proposed Response**

Response Status: O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Proposed Response

Cl 176 SC 176C P594 L1 # 298
Loewenthal, Arnon alphawave semi

Comment Type T
Comment Status X
Annex 176C "SM-PMA test vectors" is currently empty.

Suggested Remedy
Add test vectors for 200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, and 1.6TBASE-R 16:8 to Annex 176C based on supporting contribution on May interim.

Proposed Response
Response Status O

Cl 184 SC 184.4.1 P445 L3 # 299
Loewenthal, Arnon alphawave semi

Comment Type T
Comment Status X
Need to further define the deskew requirement. For now it is defined as optional. In practice full deskew is optional, but doing 10b alignment of RS symbols is mandatory.

Suggested Remedy
Replace lines 8-18 with the requirement of partial deskew, which means 10b RS symbols resolution deskew.

Proposed Response
Response Status O

Cl 184 SC 184.4.2 P445 L19 # 300
Loewenthal, Arnon alphawave semi

Comment Type T
Comment Status X
Need to further define the lanes reorder requirement. For now it is defined as optional. In practice full lanes reorder is optional, but partial reorder, meaning having flow-0 on lanes 0-15 and flow-1 on lanes 16-31 is required. Not doing that would impact end to end FEC performance and margins.

Suggested Remedy
Two options:
1. remove the word 'optional' from line 22.
2. Define the restriction of having flow-0 on lanes 0-15 and flow-1 on lanes 16-31.

Proposed Response
Response Status O

Cl 182 SC 182.1 P392 L44 # 301
Maki, Jeffery Juniper Networks

Comment Type TR
Comment Status X
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

Suggested Remedy
Delete the acronym IMDD.

Proposed Response
Response Status O

Cl 182 SC 182.1 P393 L29 # 302
Maki, Jeffery Juniper Networks

Comment Type TR
Comment Status X
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

Suggested Remedy
Delete the acronym IMDD.

Proposed Response
Response Status O

Cl 182 SC 182.1 P394 L23 # 303
Maki, Jeffery Juniper Networks

Comment Type TR
Comment Status X
Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

Suggested Remedy
Delete the acronym IMDD.

Proposed Response
Response Status O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Proposed Response**

**Comment Type**: TR

**Comment Status**: X

**Associated clause description is malformed.** The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

**Suggested Remedy**

Delete the acronym IMDD.

**Proposed Response**

**Response Status**: O

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**Comment ID**: 306

**Cl**: 177A  **SC**: 177A  **P**: 643  **L**: 5  **#**: 806

Maki, Jeffery  Juniper Networks

**Comment Type**: T  **Comment Status**: X

Annex title unnecessarily uses the acronym IMDD. Not clear what purpose is achieved that cannot be achieved simply by omitting the use of the acronym IMDD.

**Suggested Remedy**

Delete the acronym IMDD.

**Proposed Response**

**Response Status**: O
### Proposed Response

#### Comment ID 310

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**Comment Type:** TR  
**Comment Status:** X

**Comment:**

800GBASE-ER1-20 is defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." This PHY as noted in Table 169-3a, uses PCS encoding as defined in Clause 186.

**Suggested Remedy:**

Define new name for family / encoding based on Clause 186 encoding.

**Proposed Response**

Define new name for family / encoding based on Clause 186 encoding.

**Response Status:** O

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### Proposed Response

#### Comment ID 311

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**Comment Type:** TR  
**Comment Status:** X

**Comment:**

With the adoption of the objective to do 500m over 4 WDM lanes on a single mode fiber and its nomenclature 800GBASE-FR4-500, "FR" is no longer limited to just represent 2km (e.g. FR-500). This introduces an inconsistency for 200GBASE-FR1 and 200GBASE-DR1 (DR1 is not FR1-500). In addition, when looking at 2km for 1,2,4,8 fibers- a confusing "family" of PHYs emerges (200GBASE-FR1, 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2).

**Suggested Remedy:**

Rename 200GBASE-FR1 to 200GBASE-DR1-2

**Proposed Response**

Rename 200GBASE-FR1 to 200GBASE-DR1-2

**Response Status:** O

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### Proposed Response

#### Comment ID 312

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**Comment Type:** TR  
**Comment Status:** X

**Comment:**

For 100Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R SM PMA is "C" / conditional if either 200GAUI-1 is implemented. For 200Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R BM PMA is "C" / conditional if either 200GAUI-2 is implemented. For 400Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE R BM PMA is "C" / conditional if either 400GAUI-4 is implemented.

**Suggested Remedy:**

For 100Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R SM PMA is "C" / conditional if either 200GAUI-1 is implemented. For 200Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R BM PMA is "C" / conditional if either 200GAUI-2 is implemented. For 400Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE R BM PMA is "C" / conditional if either 400GAUI-4 is implemented.

**Proposed Response**

Change entries as described above in Tables 116-3, 116-4 and 116-4a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C / with notes as stated above. Modify entry in Table 178-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C is implemented. Modify entry in Table 178-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C is implemented. Modify entry in Table 179-1 to 200GBASE-R SM PMA to Conditional. Add note "c" A 200GBASE-R SM PMA must be implemented if a 200GAUI-1 C2C is implemented. Modify entry in Table 179-2 to 400GBASE-R SM PMA to Conditional. Add note "c" A 400GBASE-R SM PMA must be implemented if a 400GAUI-4 C2C is implemented. Modify entry in Table 180-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented. Modify entry in Table 180-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented. Modify entry in Table 182-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented. Modify entry in Table 182-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented.

**Response Status:** O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Proposed Response**

### Comment 313

**Comment Type:** TR  
**Comment Status:** X  
**Cl 116 SC 116.1.4 P98 L18**

**D'Ambrusia, John**  
Futurewei, U.S. Subsidiary of Huawei

**Comment:**

there is no PMD called 400GBASE-LR4

**Suggested Remedy:**

- Change 400GBASE-LR4 to 400GBASE-LR4-6

**Proposed Response:**

**Response Status:** O

### Comment 314

**Comment Type:** TR  
**Comment Status:** X  
**Cl 116 SC 116.2.4 P99 L1**

**D'Ambrusia, John**  
Futurewei, U.S. Subsidiary of Huawei

**Comment:**

In support of 200 Gb/s per lane signaling - 200GBASE-R BM-PMA and 400GBASE-R PMA. Clause 176 was developed. No addition was made to 116.2 Summary of 200GbE and 400 GbE sublayers was made.

**Suggested Remedy:**

- Modify last sentence of 116.2.4 and add additional text
  - The 200GBASE-R and 400GBASE-R PMAs, which supports bit multiplexing, is specified in Clause 120.
  - The 200GBASE-R and 400GBASE-R PMAs, which supports symbol multiplexing, is specified in Clause 176.
  - Note that "PMA" is used as a general term to represent both types of PMAs for each speed.

**Proposed Response:**

**Response Status:** O

### Comment 315

**Comment Type:** TR  
**Comment Status:** X  
**Cl 169 SC 169.1.3 P116 L42**

**D'Ambrusia, John**  
Futurewei, U.S. Subsidiary of Huawei

**Comment:**

800GBASE-ER1-20 and 800GBASE-ER1 are both defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." These two PHYs as noted in Table 169-3a, they use PCS encoding as defined in Clause 186.

**Suggested Remedy:**

- Define new name for family / encoding based on Clause 186 encoding.
- Eliminate table entries for ER1-20 and ER1 from Table 169-3a.
- Create new table for PHY type and clause correlation for new family based on Clause 186 encoding.
- Modify description of entry for 800GBASE-ER1-20 in Table 169-1 to reflect new family name.
- Modify description of entry for 800GBASE-ER1 in Table 169-1 to reflect new family name.

**Proposed Response:**

**Response Status:** O

### Comment 316

**Comment Type:** TR  
**Comment Status:** X  
**Cl 169 SC 169.1.4 P117 L12**

**D'Ambrusia, John**  
Futurewei, U.S. Subsidiary of Huawei

**Comment:**

Table 169-2 introduces the 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA in Table 169-2, but there is no real explanation to the use of the sub-layers - just the required PMA service interfaces, as noted in Items C&E. The clarification of these two sublayers is actually defined in 176.2 Conventions, which does not make sense.

**Suggested Remedy:**

- Move definitions of 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA from 176.2 to 169.1.3 Nomenclature

**Proposed Response:**

**Response Status:** O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

D'Ambrosia, John
Futurewei, U.S. Subsidiary of Huawei

Comment Type TR Comment Status X

800GBASE-R BM-PMA and 800GBASE-R-SM-PMA are noted as optional in Tables 169-2, 169-3, and Table 169-3a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not.

Suggested Remedy

For 100Gb/s based PHYs the 800GBASE-R BM-PMA is mandatory, all AUIs are optional, and 800GBASE R SM PMA is “C” / conditional if either 800GAUI-4 is implemented.
For 200Gb/s based PHYs the 800GBASE-R SM-PMA is mandatory, all AUIs are optional, and 800GBASE R BM PMA is “C” / conditional if either 800GAUI-8 is implemented.

Modify entry in Table 178-3 to 800GBASE-R BM PMA to Conditional. Add note “c” A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented. Modify entry in Table 180-3 to 800GBASE-R BM PMA to Conditional. Add note “c” A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented. Modify entry in Table 179-3 to 800GBASE-R SM PMA to Conditional. Add note “c” A 800GBASE-R SM PMA must be implemented if a 800GAUI-4 C2C is implemented. Modify entry in Table 180-3 to 800GBASE-R BM PMA to Conditional. Add note “c” A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented.

D'Ambrosia, John
Futurewei, U.S. Subsidiary of Huawei

Comment Type TR Comment Status X

In support of 200 Gb/s per lane signaling - 800GBASE-R BM-PMA, Clause 176 was developed. No addition was made to 169.2 Summary of 800 GbE architecture

Suggested Remedy

Modify 169.2.4 to read:
- The PMA sublayer provides a medium-independent means to support the use of a range of physical media.
- The 800GBASE-R PMA, which supports bit multiplexing, is specified in Clause 173.
- The 800GBASE-R PMA, which supports symbol multiplexing, is specified in Clause 176.

Note that “PMA” is used as a general term to represent both types of PMAs.

D'Ambrosia, John
Futurewei, U.S. Subsidiary of Huawei

Comment Type TR Comment Status X

800GBASE-ER1 and 800GBASE-ER1-20 use the Clause 186 800GBASE-ER1 PCS/PMA. This layer is not described as part of 169.2.

Suggested Remedy

Create 169.2.4c 800GBASE-ER1 PCS/PMA
- The 800GBASE-ER1 PCS performs encoding of data from the 800GMII, performs GMP mapping, applies FEC, and transfers the encoded data to the PMA. The 800GBASE-ER1 PMA sublayer performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface.

The 800GBASE-ER1 PCS is specified in Clause xxx.

D'Ambrosia, John
Futurewei, U.S. Subsidiary of Huawei

Comment Type TR Comment Status X

5/3/2024 10:09:28 AM

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Comment ID

Comment ID 319 Page 61 of 118
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment Type: TR**
**Comment Status:** X

For 800GBASE-LR1 in Table 169-3a
800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M

**Suggested Remedy**
Change entries for 800GBASE-LR1 to C for 800GBASE-R BM-PMA and 800GBASE-R SM-PMA
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

**Proposed Response**

**Response Status:** O

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**Comment Type: TR**
**Comment Status:** X

Table 185-1, Figure 185-1, Figure 185-2 does not reflect the PHY type and clause correlation in Table 169-3a. There is no mention of 800GBASE-R BM-PMA, 800GAUI-8 C2C, 800GAUI-8 C2M, 800GAUI-4 C2C, and 800GAUI-4 C2M.


**Suggested Remedy**
Clause 185 needs to be updated to reflect these layers.
Table 185-1 needs the following entries -
800GBASE-R BM-PMA - conditional
800GAUI-8 C2C - optional
800GAUI-8 C2M - optional
800GAUI-4 C2C - optional
800GAUI-4 C2M - optional
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

Figure 185-1 should include a PMA sublayer in the diagram and be added to legend below
Figure 185-2 needs to be updated to show the 800GBASE-R PMA Sublayer and service interface between the PCS and Inner FEC

**Proposed Response**

**Response Status:** O

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**Comment Type: TR**
**Comment Status:** X

Current baseline proposal is lacking tap weight restrictions, which were indicated as TBD when adopted.

**Suggested Remedy**
Propose adopting the TDECQ tap weight restrictions as presented in welch_3dj_01_0524.

**Proposed Response**

**Response Status:** O
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**Comment ID 325**

**Comment Type**: TR  
**Comment Status**: X  
**Proposed Response**:  
Current baseline proposal is lacking tap weight restrictions, which were indicated as TBD when adopted.  
**Suggested Remedy**: Propose adopting the TDECQ tap weight restrictions as presented in welch_3dj_01_0524.

**Comment ID 326**

**Comment Type**: TR  
**Comment Status**: X  
**Proposed Response**:  
In later 100GPL specs (ie, 100GBASE-FR1) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.5 dB as it was not updated to reflect the changes to effective TDECQ(min).  
**Suggested Remedy**: Propose changing "Average launch power, each lane (min)" in Table 180-7 from -2.8 dBm to -3.3 dBm.

**Comment ID 327**

**Comment Type**: TR  
**Comment Status**: X  
**Proposed Response**:  
In later 100GPL specs (ie, 400GBASE-FR4) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.6 dB as it was not updated to reflect the changes to effective TDECQ(min).  
**Suggested Remedy**: Propose changing "Average launch power, each lane (min)" in Table 183-6 from -1.8 dBm to -2.2 dBm.

**Comment ID 328**

**Comment Type**: TR  
**Comment Status**: X  
**Proposed Response**:  
In later 100GPL specs (ie, 100GBASE-FR1) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.5 dB as it was not updated to reflect the changes to effective TDECQ(min).  
**Suggested Remedy**: Propose changing "Average launch power, each lane (min)" in Table 182-7 from -2.1 dBm to -2.6 dBm.

**Comment ID 329**

**Comment Type**: T  
**Comment Status**: X  
**Proposed Response**:  
For the added row in Table 90A-1, the potential timestamp accuracy impairment due to alignment marker insertion/removal for 1.6T is incorrect. It should be 1.28ns, not 2.56ns. The values for 200G, 400G, and 800G are also erroneous (should all be 5.12ns). I've filed a maintenance request to correct these, too.  
**Suggested Remedy**: Change 2.56 to 1.28ns in the added row for Table 90A-1.
Different scrambler seeds for the two flows are NOT strictly necessary for the 1.6TBASE-R PCS. The output PCSLs are never bit muxed, so having identical outputs from FEC A and FEC C, for example, should never have any adverse effect on "clock content" of the SerDes output. It doesn't hurt to have the scramblers be seeded differently, however.

Suggested Remedy
Consider changing the last sentence on page 173 from:
When reset is asserted, the two scramblers shall be initialized to a value other than zero and different from each other.
To:
When reset is asserted, the two scramblers shall be initialized to values other than zero.

(snuck in an editorial correction there, too!)

Proposed Response Response Status O

Has any thought been given to how to calculate the latency through the 1.6TBASE-R PCS, i.e. the path data delay values for the purposes of TimeSync?
I do not see anything within the 1.6TBASE-R PCS that would prevent proper calculation of the path data delay values.
Clause 90.7.1 is instructive here, explaining that the path data delays should be "reported as if the DDMP is at the start of the FEC codeword". However, the existing language in 90.7.1 is awkward for PCSs with more than one FEC engine like the 1.6TBASE-R PCS, which has four FEC codewords in parallel.

Suggested Remedy
No proposed change to Clause 175.
Clause 90.7.1 could be cleaned up to account for when there are multiple FEC codewords in parallel, but I assume that is out-of-scope for the 802.3dj project? I'll submit a maintenance request.

Proposed Response Response Status O

I understand why the use of the stateless encoder decoder is restricted to 200GBASE-R, and 400GBASE-R over 200Gbps lanes. Allowing it on other PMDs/AUIs would be out-of-scope for the 802.3dj project.
HOWEVER, shouldn't common sense prevail, here?
The stateless encoder/decoder was designed such that it is all-but-identical to the stateful encoder, only differing in their treatment of /E/ blocks. Since the 200GBASE-R and 400GBASE-R links are always protected by FEC, it is not as if /E/ blocks can occur at random causing divergent behaviour of the two encoder/decoder types.
There is absolutely no danger of causing backward-compatibility issues, because the stateful encoder/decoder are still allowed for all PMDs. The stateless encoder/decoder was added to the standard to allow greater implementation flexibility (removing long timing paths). But any new PCS implementation that may attach to either 100Gbps/lane or 200Gbps/lane PMDs would have to implement the stateful encoder/decoder! With the stateless encoder, the standard is offering more implementation flexibility that implementors cannot actually use.

Suggested Remedy
Consider removing the restriction on PMD type when using the stateless encoder and decoder in subclauses 119.2.4.1 and 119.2.5.8, respectively.

Proposed Response Response Status O

ER1 PCS: Planting the seed for when the PCS is ready to be properly reviewed.
How to calculate the path data delay across the ER1 PCS/PMA? Clause 90 and Annex 90A give general rules, like how to calculate the rx/tx path data delay when there are functions within the PHY that introduce cyclical delay.
But the path data delay in the ER1 PCS is very different from anything that has been imagined in Clause 90 - an Ethernet stream that floats within a GMP frame will present unique challenges; it is not immediately clear how to determine the min/max latency across such a PCS.
This might be worse than the Alignment marker issue!

Suggested Remedy

Proposed Response Response Status O
Cl 180 SC 180.7.1 P358 L28 # 335
Ferretti, Vince Corning

Comment Type TR Comment Status X
ITU-T G.652.B cabled fiber attenuation is only specified for 1310 nm and 1550 nm wavelengths. It is not specified for wavelengths between 1260 nm and 1310 nm and not meant to be used in xWDM applications

Suggested Remedy
Remove ITU-T G.652.B (dispersion unshifted) as a fiber option.

Proposed Response Response Status O

---

Cl 180 SC 180.7.3.2 P361 L9 # 338
Lambert, Angie Corning

Comment Type T Comment Status X
IEC 61753-1-1 has been superseded by IEC 61753-1.

Suggested Remedy
Change "IEC 61753-1-1" to "IEC 61753-1".

Proposed Response Response Status O

---

Cl 180 SC 180.7.3.3 P361 L42 # 340
Lambert, Angie Corning

Comment Type T Comment Status X
IEC 61753-021-2 has been superseded by IEC 61753-021-02.

Suggested Remedy
Change "IEC 61753-021-2" to "IEC 61753-021-02".

Proposed Response Response Status O

---

Cl 180 SC 180.7.3.4 P361 L50 # 339
Lambert, Angie Corning

Comment Type T Comment Status X
IEC 61753-021-2 has been superseded by IEC 61753-021-02.

Suggested Remedy
Change "IEC 61753-021-2" to "IEC 61753-021-02".

Proposed Response Response Status O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Proposed Response

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TYPE: TR/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  Z/withdrawn
SORT ORDER: Comment ID

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**Comment:** IEC 60950-1 has been superseded by IEC 62368-1.

**Suggested Remedy:** Change "IEC 60950-1-1" to "IEC 63268-1."

**Response Status:** O

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**Comment:** IEC 61753-021-2 has been superseded by IEC 61753-021-02.

**Suggested Remedy:** Change "IEC 61753-021-2" to "IEC 61753-021-02."

**Response Status:** O

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**Comment:** IEC 61753-021-2 has been superseded by IEC 61753-021-02.

**Suggested Remedy:** Change "IEC 61753-021-2" to "IEC 61753-021-02."

**Response Status:** O

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**Comment:** In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

**Suggested Remedy:** Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

**Response Status:** O

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**Comment:** In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

**Suggested Remedy:** Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

**Response Status:** O

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**Comment:** In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

**Suggested Remedy:** Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

**Response Status:** O
In Table 178-12, the transmission line parameters for the "Class B package model" do not match the adopted baseline proposal li_3dj_01a_2311 slide 9.

Proposed Response

Replace the characteristic impedance for stage 1 with 92 Ohms, and the length/characteristic impedances for stage 2 through 4 with 70 Ohm/1 mm, 80 Ohm/1 mm, and 100 Ohm/0.5 mm respectively. Similarly in Table 179-15 and Table 176-D-6.

Comment Status

X

Response Status

O

Healey, Adam
Broadcom Inc.

Comment Type

T

Comment Status

X

The reader may be tempted to interpret the parameters in Tables 178-12 and 178-13 as implementation requirements. E.g., "Receiver discrete-time equalizer parameters" may mistakenly be interpreted as requirements for receiver implementations. It would be worthwhile to add text here clarifying that the parameters represent a minimum level performance and that there is expected to be a variety of approaches to implementation that achieve this performance.

Suggested Remedy

Add text stating the parameter values in the tables are chosen to represent the minimum required transmitter and receiver performance and they do not represent required implementation details. Compliant implementations are only required to meet or exceed this minimum level of performance. Similarly in 179.11.7 and 176.D.4.1.

Proposed Response

Response Status

O

Healey, Adam
Broadcom Inc.

Comment Type

T

Comment Status

X

Parameters "f_min", "delta_f", and "M" are defined in Table 178-13 but are not used in Annex 178A. Any guidance on appropriate choices for measurement start frequency, frequency step, and simulation time step may be provided in a general way in Annex 178A (see, for example, 178A.1.3). The values for these parameters rarely, if ever, change and it seems unnecessary to add a rows for them to an already lengthy table.

Suggested Remedy

Remove these parameters from Table 178-13. Also remove these parameters from Tables 179-16 and Table 176D-7.

Proposed Response

Response Status

O

Healey, Adam
Broadcom Inc.

Comment Type

T

Comment Status

X

Typo.

Suggested Remedy

Change "106.255" to "106.25".
The relationship between "detector error ratio", "PAM-L symbol error ratio", and "bit error ratio" is not documented and, as a result, not generally understood. While these quantities are related, they are not interchangeable. Prior assumptions that they are interchangeable has led to errors in the translation between COM results and expected (measured) receiver performance. This new annex gives us an opportunity to clarify the relationship between DER0 and other terms or to replace DER0 with a more generally understood term.

Suggested Remedy
Slide 5 of <https://www.ieee802.org/3/dj/public/23_11/healey_3dj_01a_2311.pdf> suggest expressions for relationship between detector error ratio and other terms. Either replace "DER0" with a target PAM-4 symbol error ratio (or bit error ratio) and adjust the equations for calculating COM accordingly, or document the relationship between DER0 and the other two terms.

Comment Status X
Response Status O

The reference to 179.8.9 seems inappropriate here since that subclause contains cross-references specific to the Clause 179.

Suggested Remedy
Replicate the content of 179.8.9 here, replacing references to Clause 179 electrical requirements to the corresponding references in Clause 178.

Comment Status X
Response Status O

The Annex 176A control function is required and should be included in Table 178-1 (as is done in Table 179-1).

Suggested Remedy
Add "176A - Control" as "Required" in Tables 178-1, 178-2, 178-3, and 178-4.

Comment Status X
Response Status O

The title of Table 176E-7 suggests that is should contain reference receiver parameters. Many of the parameters in the table are not relevant to a reference receiver or an eye diagram measurement. It is understood that this may become moot if a different test method is adopted, but until this decision is made the table can be trimmed down to remove "TBDs" that will never need to be defined.

Suggested Remedy
Remove parameters "maximum start frequency", "maximum frequency step", all "transmitter" parameters including "number of signal levels" and "level separation mismatch ratio", "number of samples per unit interval", and "target detector error ratio". It is also questionable whether device termination and package model parameters are needed (they were not used in Annex 120G).

Comment Status X
Response Status O

The Q values are not the same as the baseline adopted.

Suggested Remedy
According to the adopted baseline, change the Q values as follows:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

Comment Status X
Response Status O

20b deskew is incorrect. According to Motion #10 in https://www.ieee802.org/3/dj/public/23_07/motions_3cwdfdj_2307.pdf, it is required to deskew to codeword boundaries.

Suggested Remedy
Change "20b deskew" to "deskew to codeword boundaries" or simply "deskew"
Cl 176 SC 176.5.1.3.1 P201 L32 # 568
He, Xiang Huawei
Comment Type TR Comment Status X
20b deskew is incorrect. According to Motion #10 in https://www.ieee802.org/3/dj/public/23_07/motions_3cwdfdj_2307.pdf, it is required to deskew to codeword boundaries.
SuggestedRemedy
Remove the second and third paragraph in 176.5.1.3.1 and reuse 119.2.5.1.
Proposed Response Response Status O

Cl 30 SC 30 P56 L33 # 569
He, Xiang Huawei
Comment Type TR Comment Status X
Add TimeSync entity managed object classes for Inner FEC sublayers defined in Clause 177 and 184.
SuggestedRemedy
(Presentation will be prepared for this comment.)
Proposed Response Response Status O

Cl 45 SC 45 P51 L9 # 570
He, Xiang Huawei
Comment Type TR Comment Status X
Add MDIO interface registers for Inner FEC sublayers defined in Clause 177 and 184.
SuggestedRemedy
Add definitions for the new register set defined for the Inner FEC sublayers in 30.3.1.1 - 30.1.1.14.
(Presentation will be prepared for this comment.)
Proposed Response Response Status O

Cl 184 SC 184.4.7.1 P450 L14 # 871
He, Xiang Huawei
Comment Type TR Comment Status X
It is said "4-bit pilot symbols (PS) are inserted every 64 4-bit blocks (one 4-bit PS, 63 4-bit message blocks)."
But in Figure 184-5, message blocks m<0:63>, m<64-127>, …between pilot symbols has 64 4-bit blocks.
SuggestedRemedy
Change Figure to match the text, i.e., change m<0:63> to m<0:62>, change m<64:127> to m<63:125>, etc.
Proposed Response Response Status O

Cl 184 SC 184.6.5 P462 L1 # 872
He, Xiang Huawei
Comment Type TR Comment Status X
It is possible that one polarization is locked but the other polarization can not get locked.
With the current variable list and state diagrams this can not be identified or reported.
(This is a little different from AM lock process across PCS lanes, where it is way up in the sublayers higher than the pilot sequence lock, and it may not be a problem.)
SuggestedRemedy
Recommend to add a timer (value TBD) to indicate that it has waited long enough after one polarization is locked but the other is still not locked.
Proposed Response Response Status O

Cl 184 SC 184.8 P464 L10 # 873
He, Xiang Huawei
Comment Type TR Comment Status X
Only "alignment_valid" is reported, not individual "dsp_lock<x>" variables.
SuggestedRemedy
It is recommended to report both "dsp_lock<x>" in table 184-7, as we did for PCS lane lock where we reported "Lane x aligned" for all PCS lanes.
Proposed Response Response Status O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment ID: 374**
**Page 71 of 118**

- **Cl 185 SC 185.7.1 P481 L21**
- **He, Xiang** Huawei
- **Comment Type: TR** Comment Status: X

The 800GBASE-LR1 Inner FEC would not see or use scrambled idles as its input. The input to the 800GBASE-LR1 Inner FEC should be "scrambled idle processed by 800GBASE-R PCS".

**Suggested Remedy**
- Change "pattern description" column in Table 185-9 to "Scrambled idle proceed by 800GBASE-R PCS and then encoded by the 800GBASE-LR1 Inner FEC".

**Response Status: O**

**Comment ID: 375**

- **Cl 185 SC 185.7.1 P481 L21**
- **He, Xiang** Huawei
- **Comment Type: TR** Comment Status: X

The scrambled idle test pattern for 800GBASE-R PCS is defined in 172.2.4.11, not 175.2.4.11.

**Suggested Remedy**
- Change "175.2.4.11" to "172.2.4.11" and format as external reference.

**Response Status: O**

**Comment ID: 376**

- **Cl 175 SC 175.2.4.5 P174 L3**
- **Ofelt, David** Juniper Networks
- **Comment Type: T** Comment Status: X

Text says to interleave two codewords from flow 0 and two from flow 1, but it isn’t clear that those two should be from different FEC encoders.

**Suggested Remedy**
- After FEC encoding, a FEC codeword from each of the two encoders in flow 0 and a FEC codeword from each of the two encoders in flow 1 are then interleaved and distributed to individual PCS lanes.

**Response Status: O**

**Comment ID: 377**

- **Cl 175 SC 175.2.4.5 P174 L3**
- **Ofelt, David** Juniper Networks
- **Comment Type: T** Comment Status: X

Editor’s Note asks if we should require different reset values for the scramblers.

**Suggested Remedy**
- Yes, we should!

**Response Status: O**

**Comment ID: 378**

- **Cl 176 SC 176.5.1.6.6 P207 L6**
- **Ofelt, David** Juniper Networks
- **Comment Type: T** Comment Status: X

Should there be an arc from ALIGNMENT_FAIL to LOSS_OF_ALIGNMENT?

**Suggested Remedy**
- If so, add the arc

**Response Status: O**

**Comment ID: 379**

- **Cl 176 SC 176.7.1 P221 L20**
- **Maniloff, Eric** Ciena
- **Comment Type: E** Comment Status: X

Table 176-7 includes two references to 400GBASE-R, these should be replaced with 800GBASE-R.

**Suggested Remedy**
- Replace the text "400GBASE-R" with "800GBASE-R" in Table 176-7.

**Response Status: O**
### Comment 380

**Comment Type**: T<br>
**Comment Status**: X<br>

800GBASE-LR1 is being defined to allow unlocked lasers with frequency errors larger than the DSP digital acquisition range. Additional parameters are required for the Tx laser to accommodate this. Values will be provided after further study, but the new parameters can be added to Table 185-4. A supporting contribution will be provided.

**Suggested Remedy**
- Add the following parameters to Table 185-4:
  - Maximum Tx laser frequency slew rate: Preacquisition [Units GHz/s]
  - Maximum Tx laser frequency slew rate: Post acquisition [Units GHz/ms]
  - Laser Relative Frequency tracking accuracy [Units GHz]

**Proposed Response**
- Response Status: O

### Comment 381

**Comment Type**: T<br>
**Comment Status**: X<br>

The specification should have a Tx clock noise defined.

**Suggested Remedy**
- Add an entry for Tx clock phase noise (PN): Maximum PN mask
- Add an entry for Tx clock phase noise (PN): Maximum total integrated random jitter
- Add an entry for Tx clock phase noise (PN): Maximum total periodic jitter

**Proposed Response**
- Response Status: O

### Comment 382

**Comment Type**: T<br>
**Comment Status**: X<br>

A value of -27dB is appropriate for Maximum discrete reflectance.

**Suggested Remedy**
- Replace TBD for Maximum discrete reflectance with -27

**Proposed Response**
- Response Status: O

### Comment 383

**Comment Type**: T<br>
**Comment Status**: X<br>

A value of 24dB is appropriate for Optical Return Loss.

**Suggested Remedy**
- Replace TBD in Table 185-7 with 24

**Proposed Response**
- Response Status: O

### Comment 384

**Comment Type**: T<br>
**Comment Status**: X<br>

TQM is currently undefined. Recommend adopting RSNR Penalty as a TQM. Supporting Contribution to be provided.

**Suggested Remedy**
- Replace TQM with RSNR Penalty

**Proposed Response**
- Response Status: O
There sentence below the editor's note is a repeat of what is captured in 171.3.2. It is also not related to “link fault signaling” as defined in 81.3.4, which is the topic of this subclause.

Suggested Remedy
Delete the sentence below the editor's note.

Comment Type: T
Comment Status: X

There is an issue with subclause 171.3.3 generated by 802.3df. There is an incorrect reference of “171.6.2” in the following bullets:

— An additional signal TXRD indicates the state of the rx_rm_degraded variable (see 171.6.2) as detected by the PHY 800GXS in the transmit direction
— An additional signal TXLD indicates the state of the FEC_degraded_SER variable (see 171.6.2) as detected by the PHY 800GXS in the transmit direction

Suggested Remedy
Import subclause 171.3.3 and correct the two bullets as follows:

— An additional signal TXRD indicates the state of the rx_rm_degraded variable (see 172.2.6.2.2) as detected by the PHY 800GXS in the transmit direction
— An additional signal TXLD is the logical OR of the FEC_degraded_SER and rx_local_degraded variables (see 172.2.6.2.2) as detected by the PHY 800GXS in the transmit direction.

Nominal characteristic impedance of the cable assembly is "100-ohm"

Suggested Remedy
Contributions to the task force have demonstrated the nominal characteristic impedance of the cable assembly is ~92-ohm
Cl 179 SC 179.11.3 P327 L34 # 390
Kocsis, Sam Amphenol
Comment Type T Comment Status X
ERL requirement for cable assemblies that have COM less than "4dB"
SuggestedRemedy
Change "4dB" to "TBD". Historical precedent may not be relevant for this specification
Proposed Response Response Status O

Cl 179 SC 179.11.7 P331 L44 # 391
Kocsis, Sam Amphenol
Comment Type T Comment Status X
Rd(t) = "TBD"
SuggestedRemedy
Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package
Proposed Response Response Status O

Cl 178 SC 178.9.1 P275 L39 # 395
Kocsis, Sam Amphenol
Comment Type T Comment Status X
RD(t) = "TBD"
SuggestedRemedy
Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package
Proposed Response Response Status O

Cl 179 A SC 179A.7 P668 L9 # 393
Kocsis, Sam Amphenol
Comment Type E Comment Status X
"TP0 and TP5"
SuggestedRemedy
Change to "TP0d and TP5d"
Proposed Response Response Status O

Cl 179 C SC Table 179C-4 P682 L38 # 394
Kocsis, Sam Amphenol
Comment Type E Comment Status X
"QSFP-DD800"
SuggestedRemedy
Change to "QSFP-DD1600"
Proposed Response Response Status O

Cl 178 SC 178.9.1 P275 L39 # 395
Kocsis, Sam Amphenol
Comment Type T Comment Status X
The reference impedance should match the system impedance, Rd as defined in COM spreadsheets.
SuggestedRemedy
92-ohm, TBD, or straw poll based on proposed values presented in Task Force contributions
Proposed Response Response Status O
Proposed Response

# 396
Cl 178  SC 178.10.1  P285  L40  # 396
Kocsis, Sam  Amphenol

Comment Type  T  Comment Status  X
Rd(t) = "TBD"

Suggested Remedy
Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Proposed Response  Response Status  O

# 397
Cl 178  SC 178.10.1  P285  L41  # 397
Kocsis, Sam  Amphenol

Comment Type  T  Comment Status  X
RD(r) = "TBD"

Suggested Remedy
Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Proposed Response  Response Status  O

# 398
Cl 176D  SC 176D.3.3  P597  L33  # 398
Wu, Mau-Lin  MediaTek

Comment Type  TR  Comment Status  X
The value of '106.255 +/- 50 ppm' is not correct.

Suggested Remedy
Change '106.255' to '106.25'.

Proposed Response  Response Status  O

# 399
Cl 178  SC 178.9.2  P275  L49  # 399
Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
Transmitter measurement bandwidth is TBD

Suggested Remedy
Replace TBD with 62 GHz

Proposed Response  Response Status  O

# 400
Cl 178  SC 178.9.3.3  P282  L16  # 400
Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
COM values in Table 178–10 are TBD

Suggested Remedy
Replace TBD with 3 dB

Proposed Response  Response Status  O

# 401
Cl 178  SC 178.9.3.4  P282  L45  # 401
Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
"The test channel COM, calculated per items 3) through 7) in 93C.2, is at least 3 dB"
The reference to the test channel COM is wrong.

Suggested Remedy
Change it to "The test channel COM, calculated per item e) through h) in 178.9.3.3, is at least 3 dB" to be correct

Proposed Response  Response Status  O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Comment ID 402
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
Minimum COM in Table 178-11 is TBD
Suggested Remedy
   Replace TBD with 3 dB in Table 178-11 and in line 28 of page 284
Proposed Response  Response Status  O

Comment ID 403
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
Single-ended reference resistance R0 value in Table 178-13 is TBD
Suggested Remedy
   Replace TBD with 50 Ohm
Proposed Response  Response Status  O

Comment ID 404
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
Receiver 3 dB bandwidth fr value in Table 178-13 is TBD
Suggested Remedy
   Replace TBD with 0.58*fb
Proposed Response  Response Status  O

Comment ID 405
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
The max/min values and step size of transmitter equalizer in Table 178-13 need to match those in the Table 178-6 and those in sub-clauses 179.9.4.1.4 & 179.9.4.1.5
Suggested Remedy
   On line 14 replace TBD with -0.06:0.02:0
   On line 18 replace TBD with 0.0:0.02:0.12
   On line 22 replace TBD with -0.34:0.02:0
   On line 28 replace TBD with -0.2:0.02:0
Proposed Response  Response Status  O

Comment ID 406
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
Transmitter differential peak output voltage in Table 178-13 is TBD
Suggested Remedy
   Replace Av with 0.413 V
   Replace Afe with 0.413 V
   Replace Ane with 0.608 V
Proposed Response  Response Status  O

Comment ID 407
Li, Tobey  MediaTek
Comment Type  TR  Comment Status  X
Transmitter transition time Tr value in Table 178-13 is TBD
Suggested Remedy
   Replace TBD with Tr = 4 ps
Proposed Response  Response Status  O
Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
One sided noise spectral density in Table 178-13 is TBD

Suggested Remedy
Replace TBD with 6e-9 V^2/GHz

Proposed Response  Response Status  O

Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
Level separation mismatch ratio RLM in Table 178-13 is TBD

Suggested Remedy
Replace TBD with 0.95

Proposed Response  Response Status  O

Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
"4th order Bessel-Thomson filter with 3 dB bandwidth of 40 GHz" is inconsistent with

Suggested Remedy
Change "40 GHz" to either "TBD" or "62 GHz"

Proposed Response  Response Status  O

Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
COM values in Table 179–11 are TBD

Suggested Remedy
Replace TBD with 3 dB

Proposed Response  Response Status  O

Li, Tobey  MediaTek

Comment Type  TR  Comment Status  X
Receiver 3 dB bandwidth fr value in Table 179–16 is TBD

Suggested Remedy
Replace TBD with 0.58*fb

Proposed Response  Response Status  O
### IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

#### Proposed Response

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**Comment Type:** TR  **Comment Status:** X

The max/min values and step size of transmitter equalizer in Table 179-16 need to match those in the Table 179-7 and those in sub-clauses 179.9.4.1.4 & 179.9.4.1.5

**Suggested Remedy**

- On line 14 replace TBD with -0.06:0.02:0
- On line 18 replace TBD with 0:0.02:0.12
- On line 22 replace TBD with -0.34:0.02:0
- On line 26 replace TBD with 0.5
- On line 28 replace TBD with -0.2:0.02:0

**Proposed Response**  **Response Status:** O

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**Comment Type:** T  **Comment Status:** X

Transmitter differential peak output voltage in Table 179-16 is TBD

**Suggested Remedy**

- Replace Av with 0.413 V
- Replace Afe with 0.413 V
- Replace Ane with 0.608 V

**Proposed Response**  **Response Status:** O

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**Comment Type:** TR  **Comment Status:** X

Transmitter transition time Tr value in Table 179-16 is TBD

**Suggested Remedy**

Replace TBD with Tr = 4 ps

**Proposed Response**  **Response Status:** O

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Level separation mismatch ratio RLM in Table 179-16 is TBD

**Suggested Remedy**

Replace TBD with 0.95

**Proposed Response**  **Response Status:** O

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**Comment Type:** TR  **Comment Status:** X

Number of samples per unit interval in Table 179-16 is TBD

**Suggested Remedy**

Replace TBD with 32

**Proposed Response**  **Response Status:** O

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**Comment Type:** TR  **Comment Status:** X

Transmitter measurement bandwidth is TBD

**Suggested Remedy**

- Replace TBD with 62 GHz

**Proposed Response**  **Response Status:** O
**EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment**

*Comment ID* 423

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

Signaling rate of 106.255 ± 50 ppm in Table 176D–1 is incorrect

**SuggestedRemedy**

Change "106.255 ± 50 ppm" to "106.25 ± 50 ppm"

**Proposed Response**

Response Status O

---

*Comment ID* 424

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

Reference to ERL methodology is missing

**SuggestedRemedy**

Add reference to 176D.4.3.

**Proposed Response**

Response Status O

---

*Comment ID* 425

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

4th order Bessel-Thomson filter BW is TBD

**SuggestedRemedy**

Replace TBD with 62 GHz

**Proposed Response**

Response Status O

---

*Comment ID* 426

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

Nyquist frequency in Table 176D–4 is incorrect

**SuggestedRemedy**

Change "26.5625 GHz" to "53.125 GHz"

**Proposed Response**

Response Status O

---

*Comment ID* 427

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

COM values in Table 176D–4 are TBD

**SuggestedRemedy**

Replace TBD with 3 dB

**Proposed Response**

Response Status O

---

*Comment ID* 428

**Li, Tobey**

**MediaTek**

**Comment Type** TR

**Comment Status** X

Reference to test procedure is missing

**SuggestedRemedy**

Add reference to 176D.3.4.4

**Proposed Response**

Response Status O
Table reference is missing

Suggested Remedy
- Add reference of ERL to 176D.4.3.
- Add reference of differential-mode to common-mode return loss to 176D.4.4.

Response Status: O

Minimum COM is TBD

Suggested Remedy
- Replace TBD with 3 dB in Table 176D–5 and in line 38 of page 604

Response Status: O

Single-ended reference resistance R0 value in Table 176D–6 is TBD

Suggested Remedy
- Replace TBD with 50 Ohm

Response Status: O

Receiver 3 dB bandwidth fr value in Table 176D–7 is TBD

Suggested Remedy
- Replace TBD with 0.58*fb

Response Status: O

Transmitter transition time Tr value in Table 176D–7 is TBD

Suggested Remedy
- Replace TBD with Tr = 4 ps

Response Status: O

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Comment ID
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

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Comment ID 441

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<td>Replace TBD with Tr = 4 ps</td>
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<td>Level separation mismatch ratio RLM in Table 176E–7 is TBD</td>
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IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Proposed Response

**Cl 176E SC 176E.5.2 P635 L5 # 443**

Li, Tobey MediaTek

Comment Type TR Comment Status X

Number of samples per unit interval in Table 176E–7 is TBD

Suggested Remedy

Replace TBD with 32

Proposed Response Response Status O

**Cl 176E SC 176E.5.2 P635 L35 # 444**

Li, Tobey MediaTek

Comment Type TR Comment Status X

"Dp equal to 3" is not right as there are 3 pre-taps for the host

Suggested Remedy

Change "Dp equal to 3" to "Dp equal to 4"

Proposed Response Response Status O

**Cl 116 SC 116 P92 L40 # 445**

Simms, William NVIDIA

Comment Type E Comment Status X

Spacing of text on line 40 is different than spacing of the same text in lin 38

Suggested Remedy

Make spacing the same

Proposed Response Response Status O

**Cl 176A SC 176A.4.1+ P555 L46 # 447**

Simms, William NVIDIA

Comment Type E Comment Status X

Should the status field name be uniquified? The field name in the text of the table and text sections below the table do not clearly identify text as a field.

Suggested Remedy

Change Receiver ready to RECEIVER_READY or at maybe receiver_ready and use the same in the text below the table 176A-3- Status field structure. Pertains to all field names.

Proposed Response Response Status O

**Cl 176A SC 176A.6.4 P558 L54 # 448**

Simms, William NVIDIA

Comment Type E Comment Status X

It took me longer than usual to realize the algorithm continues on page 559

Suggested Remedy

Maybe put a "---continued---" at the last line of page 558. Disregard if this is inconsistent with IEEE style

Proposed Response Response Status O

**Cl 176A SC 176A-6 P568 L21 # 449**

Simms, William NVIDIA

Comment Type ER Comment Status X

Figure 176A-6 has an extraneous < in the name "local_tf_lock<"

Suggested Remedy

Change to "local_tf_lock"

Proposed Response Response Status O

---

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general
COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed Z/withdrawn
SORT ORDER: Comment ID
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Page 83 of 118</th>
</tr>
</thead>
</table>

**Comment ID 450**

Cl 176D  SC 176D.3.3  P598  L 16  
Simms, William  NVIDIA  
**Comment Type E  Comment Status X**
Where does the value for SNDR of 32.5dB come from?

**Suggested Remedy**
No change suggested, looking for source material

**Proposed Response  Response Status O**

**Comment ID 451**

Cl 176D  SC 176D.3.4.4  P603  L 31  
Simms, William  NVIDIA  
**Comment Type TR  Comment Status X**
Moot point maybe given table is all TBD, but the frequency should be 53.125GHz

**Suggested Remedy**
change to 53.125GHz

**Proposed Response  Response Status O**

**Comment ID 452**

Cl 178  SC 178.9.2  P276  L 18  
Simms, William  NVIDIA  
**Comment Type T  Comment Status X**
SCMR may need to be relaxed for 200Gb/s. Measure of 15dB full band at TP0v given full band Vcm noise of 80mVpp at TP2.

**Suggested Remedy**
Likely need to tighten 80mV Vcm in table 179-7 for 200Gb/s

**Proposed Response  Response Status O**

**Comment ID 453**

Cl 175  SC 175.2.4.6  P175  L 22  
Opsasnick, Eugene  Broadcom  
**Comment Type T  Comment Status X**
Sub-clause 172.2.4.6 has a reference to a text file containing the 800GBASE-R alignment marker values. CL 175 should add a similar note with a corresponding text file for the 1.6TBASE-R alignment markers.

**Suggested Remedy**
Add text near line 22: "NOTE—A text file containing the alignment marker patterns, as shown in Table 175-1 is available at https://standards.ieee.org/downloads/802.3/.

A presentation will be submitted with a corresponding text file containing the 1.6TBASE-R AM values.

**Proposed Response  Response Status O**

**Comment ID 454**

Cl 175  SC 175.2.4.5  P174  L 3  
Opsasnick, Eugene  Broadcom  
**Comment Type T  Comment Status X**
The Editor's note at the end of subclause 175.2.4.5 "Scrambler" states that there are no requirements or restrictions in the 1.6TE PCS baselines for the scrambler seeds for each flow. The note also mentions that the corresponding sub-clause in 802.3df for 800GE PCS states that the two flows would have identical outputs if the seeds are identical and the data input is identical (such as after reset). The 1.6TE PCS does not have two separate sets of PCSLs like 800GE PCS, but the PCSL formation could have back-to-back repeating RS-symbol values if identical seeds are used. Suggest to require different seeds after reset in the scramblers of each flow as written in the paragraph above the editor's note.

**Suggested Remedy**
Remove the editor's note at the top of page 174, and leave the wording in 175.2.4.5 as-is with the requirement that the two scramblers are initialized with different seeds.

**Proposed Response  Response Status O**
Cl 175A  SC 175A  P539  L8  # 455
Opsasnick, Eugene  Broadcom

Comment Type  T  Comment Status  X

Annex 175A contains tabular data for an example created by the 1.6TBASE-R PCS TX functions, including the scrambler output, RS-FEC codeword generation, and PCS lane interleaving. The editor's note on page 539 has a placeholder for a link to a text file that has the machine readable text data. That data file needs to be created.

Suggested Remedy
A presentation is planned to submit a data file which corresponds to the Annex 176A example and can be referenced in the editor's note.

Proposed Response  Response Status  O

Cl 90A  SC 90A  P519  L43  # 456
Opsasnick, Eugene  Broadcom

Comment Type  T  Comment Status  X

In table 90A-1, the column titled "Alignment marker/ codeword marker insertion/removal" has a value of 2.56ns for 1.6T in the last row. This value should be the xMII time (at MAC data rate) of one Alignment marker block. The 1.6TE PCS lanes are now running at 100G vs 25G for slower speeds, so this number does not scale directly from the other entries. The value for the 1.6T row should be 1.28ns (a full AM group = 8 256b/257b blocks, so the MII time = 8 * 256 / 1600 = 1.28ns). Note that this column has correct values for 25G, 40G, 50G, and 100G. However, the value listed for 200G, 400G and 800G of 2.56ns should be 5.12ns and should also be fixed in maintenance.

Suggested Remedy
Change the accuracy impairment value of 2.56 ns to 1.28 ns for the 1.6T Ethernet rate in Table 90A-1.

Proposed Response  Response Status  O

Cl 176A  SC 176A.6.4  P558  L17  # 457
Opsasnick, Eugene  Broadcom

Comment Type  T  Comment Status  X

This the entire block of pseudo-code in this subclause is exactly the same as the code in subclause 136.8.11.4.4, and the entire subcluse only differs by adding one coefficient (-3) to the k_list. I suggest replacing the text of the entire subclause with a refernece to subclause 136.8.11.4.4.

Suggested Remedy
New text for this subclause:
"The handling of incoming requests is specified by the coefficient update state diagram (Figure 136-9).

The behavior of the UPDATE_C(k) function shall be consistent with the algorithm specified in 136.8.11.4.4 with one exception:
- The set of valid equalizer coefficient indices, k_list, is expanded by one from [-2, -1, 0, 1] to [-3, -2, -1, 0, 1]."

Proposed Response  Response Status  O

Cl 176A  SC 176A.10.4  P566  L46  # 458
Opsasnick, Eugene  Broadcom

Comment Type  T  Comment Status  X

The state diagram shown in Figure176A-8 "Training frame lock state diagram" on page 570 and Figure 176A-9 "Coefficient update state diagram" are exactly the same as the state diagrams of the same names in Figure 136-8 and Figure 136-9. Only the reset signal is renamed from "mr_restart_training" to "mr_restart".

Suggested Remedy
Remove Figure 176A-8 and Figure 176A-9.

Change "mr_restart" to "mr_restart_training" in subclause 176A.10.2.1 on page 564, line 21.

Change the text at the bottom of page 566 to refer to the equivalent state diagrams in clause 136 instead of the removed figures (with editorial license).

Any variables defined in subclause 176A.10.3.1 which are only used in the removed state diagrams can also be removed.

Proposed Response  Response Status  O
In Figure 176-16 and Figure 176-17, on the following page, the symbol pattern of the even PCSLs in the upper half (PCSL 16-31) is not shown. It would be easier to see the RS symbol patterns if the figures included at least one even PCSL in the range of 16-31.

SuggestedRemedy
These two figures show PCSLs for lanes 0,1, and 31. Suggest to show the PCSL symbol pattern for lanes 0, 1, ..., 15, 16, 17, ..., 31.

Proposed Response  Response Status O

We are now using a Next Page to advertise IEEE defined PHYs. However the order of when Next Pages are introduced, defined and then used is a bit out of order. So re-arranging the order in which AN is specified would help readers to better understand what how Next Pages are defined, how to use them and when to use them.

SuggestedRemedy
Presentation will be provided.

Proposed Response  Response Status O

The title of Clause 173 does include BM.

SuggestedRemedy
Remove the BM- from Table 171-1 for the Clause 173 entry and footnote A.

Proposed Response  Response Status O

The MDIO mapping table is different from Clause 175, it should use the new form that Clause 175 is using.

SuggestedRemedy
Have Tables 171-5a through 171-5d use the same format as Clause 175

Proposed Response  Response Status O

The last sentence is giving the transcoded blocks sent to each flow a name. So it's not really make a flow of blocks. If anything it's making a series or stream of blocks.

SuggestedRemedy
Change the last sentence to read: "The transcoded blocks sent to flow 0 are referred to as tx_xcoded_f0<256:0> and the ones sent to flow 1 as tx_xcoded_f1<256:0>.

Proposed Response  Response Status O

tx_am_sf doesn't allow but provides a way to communicate the mandatory degrade status.

SuggestedRemedy
Change "allows the local PCS to communicate the status of the FEC degraded feature to the remote PCS" to "communicates the local PCS FEC degraded status to the remote PCS".

Proposed Response  Response Status O
Comment Type: T
Comment Status: X

am_mapped_f0 and am_mapped_f1 aren't solely based on the 10b-distribution and we never talk about how this two variables are us splitting the alignment marker group up.

Suggested Remedy

Change:
“The variables am_mapped_f0 and am_mapped_f1 are then derived from 10-bit interleaving the group of 16 alignment markers, am_x, using the following procedure”

To:
“The alignment marker group is mapped into variables am_mapped_f0 and am_mapped_f1 as follows. First a 10-bit interleaving the group of 16 alignment markers, am_x, is done using the following procedure.”

Proposed Response: Response Status: O

Comment Type: T
Comment Status: X

am_mapped_f0 and am_mapped_f1 contain data that is sent into flow 0/1 and through codewords AB and CD.

Suggested Remedy

Change:
“Note that am_mapped_f0 contains the 10-bit symbols of FEC codewords A and B, and am_mapped_f1 contains the 10-bit symbols of FEC codewords C and D.”

To:
“Note that am_mapped_f0 is sent to flow 0 which produces FEC codewords A and B, and am_mapped_f1 is sent to flow 1 which produces FEC codewords C and D.”

Proposed Response: Response Status: O

Comment Type: T
Comment Status: X

The counters for correctd, uncorrected and error have always been mandatory, while the cw counter and bin counters have been optional. So Should is not appropriate.

Suggested Remedy

Change:
“The following counters should be implemented to aid a network operator in determining the link quality.”

To:
“The PCS provides the following counters that track FEC decoder statistics.”

Proposed Response: Response Status: O

Comment Type: T
Comment Status: X

The Note about tracking statistics across all 4 decoders is missing from the bin counter.

Suggested Remedy

Add this to the definition of the FEC_codeword_error_bin_i

“Note that this counter tracks codewords with errors across all four codewords.”

Proposed Response: Response Status: O
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### Comment 470
**Cl:** 119
**SC:** 119.2.5.8
**Proposed Response:**
- **Comment Type:** E
- **Comment Status:** X
- **Extraneous "either"
- **Suggested Remedy:** remove the word "either"
- **Proposed Response:**

### Comment 471
**Cl:** 176
**SC:** 176.2
**Proposed Response:**
- **Comment Type:** E
- **Comment Status:** X
- Is respectively necessary here? X is just a list of different rates.
- **Suggested Remedy:** remove the ", respectively"

### Comment 472
**Cl:** 176
**SC:** 176.2
**Proposed Response:**
- **Comment Type:** E
- **Comment Status:** X
- Is respectively necessary here? X is just a list of different rates.
- **Suggested Remedy:** remove the ", respectively"

### Comment 473
**Cl:** 176
**SC:** 176.2
**Proposed Response:**
- **Comment Type:** E
- **Comment Status:** X
- **It's a multiplexor or a multiplexing function
- **Suggested Remedy:** add the word function after multiplexing

### Comment 474
**Cl:** 176
**SC:** 176.5.1.6.4
**Proposed Response:**
- **Comment Type:** T
- **Comment Status:** X
- Figure 119-12 uses functions and variables defined in CL119 but those aren't called out to be used, just that restart_lock_mux is used to replace restart_lock
- **Suggested Remedy:**
  - add "using the state variables defined in 119.2.6.2" after Table 119-1 with editorial license

### Comment 475
**Cl:** 175
**SC:** 175.5.1.3.1
**Proposed Response:**
- **Comment Type:** T
- **Comment Status:** X
- There is more details to the AM lock function add a reference
- **Suggested Remedy:**
  - add a "(see 175.5.1.6.4)" after Table 119-1

### Comment 476
**Cl:** 176
**SC:** 176.5.1.3.5
**Proposed Response:**
- **Comment Type:** E
- **Comment Status:** X
- **It's a multiplexor or a multiplexing function
- **Suggested Remedy:**
  - add the word function after multiplexing
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</table>

**Comment 477**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

Figure 119-12 uses functions and variables defined in CL119 but those aren't called out to be used, just that restart_lock_mux is used to replace restart_lock  

**Suggested Remedy:**  
add "using the state variables defined in 119.2.6.2" after Table 119-1 with editorial license  

**Proposed Response**  
Response Status O

**Comment 478**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

test pattern generate is overlapping with the IS_SIGNAL_request line in Figure 176-2  

**Suggested Remedy:**  
Move "test pattern generate" to not overlap with the inst.IS_SIGNAL.request line  
Same in Figure 176-9,10,13,14,15,19,20,24,25,26  

**Proposed Response**  
Response Status O

**Comment 479**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

test pattern generate is overlapping with the IS_SIGNAL_request line in Figure 176-2  

**Suggested Remedy:**  
Move "test pattern generate" to not overlap with the inst.IS_SIGNAL.request line  
Same in Figure 176-9,10,13,14,15,19,20,24,25,26  

**Proposed Response**  
Response Status O

**Comment 480**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

test pattern check is overlapping with IS_SIGNAL.request  

**Suggested Remedy:**  
Move "test pattern check" to no overlap withPMA.IS_SIGNAL.request in Figure 176-21  

**Proposed Response**  
Response Status O

**Comment 481**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

A note that modifying the data stream could affect TimeSync would be useful.  

**Suggested Remedy:**  
Add the following note:  
"NOTE -- Insertion or removal of characters may affect protocols like times synchronization (see 90.4.1.2)"  

**Proposed Response**  
Response Status O

**Comment 482**

Slavick, Jeff  
Broadcom  

**Comment Type:** T  
**Comment Status:** X  

Counter_done needs to be at the end of the counter name.  

**Suggested Remedy:**  
Change symbol_pair_lock_counter_done_demux to symbol_pair+lock_counter_done_demux_done  

**Proposed Response**  
Response Status O
Slavick, Jeff  
Broadcom

**Comment Type:** E  **Comment Status:** X
I think it's best if the Start of the counter is the last thing in the Box

**Suggested Remedy:**
Move "Start symbol_pair_lock_counter_demux" to be the last thing in LOSS_OF_SYMBOL_PAIR_LOCK box

**Proposed Response:**

---

Slavick, Jeff  
Broadcom

**Comment Type:** T  **Comment Status:** X
Detailed functions and state diagrams has no content

**Suggested Remedy:**
Change 176.5.1.6 to be a sub-heading of 176.5.1.5 (4th tier I think).

**Proposed Response:**

---

Slavick, Jeff  
Broadcom

**Comment Type:** T  **Comment Status:** X
The Variables state that these all of them, not inheriting Cl119 functions except for some replacements.

**Suggested Remedy:**
Copy Figure 119-12 into Cl 176 and modify it to use:

- restart_lock_dir **with dir in italics**
- amps_lock_dir **with dir in italics**
- pcs_lane_mapping_dir **with dir in italics**

- add a NOTE that italics dir is either mux or demux

In Variables, Constants and Counters sections define everything that is used, referring to Cl 119 when possible.

- Change references to Figure 119-12 to point to the new figure.

- With editorial license

**Proposed Response:**

---

Slavick, Jeff  
Broadcom

**Comment Type:** T  **Comment Status:** X
The deskew process doesn't need an exception since the referred texts says to do it across "ALL" PCSLs

**Suggested Remedy:**

- Remove the deskew across 16 lanes exception in 176.6.1.2.1
- Remove the deskew across 32 lanes exception in 176.7.1.2.1

**Proposed Response:**

---

Slavick, Jeff  
Broadcom

**Comment Type:** T  **Comment Status:** X
The delay line for Cl177 starts with feeding data into the longest delay line while Cl184 sends it to the delay line with the shortest delay.

**Suggested Remedy:**
Change Cl177 to have the Delay Line 0 be the minimal delay and the Delay Line 2 to be the longest delay.

**Proposed Response:**

---
Comment Type: T  Comment Status: X
The last paragraph describing options for how the pad insertion could be done is unnecessary. The requirement that it occurs every 8704 CW and follows the Figure 177-6 is sufficient.

Suggested Remedy
Remove the last paragraph of 177.4.6

Comment Type: T  Comment Status: X
Monitor and drop says you monitor on all flows. But Figure 177-7 is a per flow state diagram. So is each Flow checking for 140 bad out of 150? And 150 is not a multiple of 8 for it to span across all flows evenly.

Suggested Remedy
"keeps monitoring 150 consecutive codewords on all flows, if at least 140 codewords are invalid, drop sync and restart from step a)."

Change:
"each flow counts the number of invalid codewords seen in consecutive non-overlapping 150 codeword windows, if at least 140 codewords are invalid, drop sync and restart from step a)."

Comment Type: E  Comment Status: X
In Figure 177-8 the wrong character is showing up for the <= symbol

Suggested Remedy
Fix <= symbol in Figure 177-8

Comment Type: T  Comment Status: X
Counters automatically have a _done variable created for them, so no need to define fc_cnt_done

Suggested Remedy
Remove fc_cnt_done definition

Comment Type: T  Comment Status: X
Defining how a miscorrected codeword can occur could be phrased more clearly.

Change:
"Note that when there is more than one bit error in a codeword there is a chance that the soft decision decoder could miscorrect the codeword."

Comment Type: T  Comment Status: X
The PRBS gen should "stop" if training stops.

Suggested Remedy
Add "while training is in progress while this mode is selected" after "is not stopped or reset".
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Suggested Remedy</th>
<th>Proposed Response</th>
<th>Response Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cl 176A SC 176A.2.3.3 P552 L43</td>
<td>T</td>
<td>X</td>
<td>Add &quot;while training is in progress while this mode is selected&quot; after &quot;is not stopped or reset&quot;.</td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>Cl 176A SC 176A.2.3.3 P552 L41</td>
<td>T</td>
<td>X</td>
<td>PRBS13 free-running can only provide PAM4 it does not have a select for PAM2 or PAM4 with precode while PRBS31 does have those options. So how can we refer to PRBS13 free running for how to map the PRBS data to training pattern.</td>
<td>Split the 2nd paragraph of 176A.2.3.3 into 3 paragraphs that define how the pattern for each of the possible encoding options as is done in 176A.2.3.1</td>
<td>O</td>
</tr>
<tr>
<td>Cl 176A SC 176A.2.3.2 P552 L31</td>
<td>T</td>
<td>X</td>
<td>There is only 1 mode of operation for PRBS13 free-running, PAM4. We do have 1 free mode.</td>
<td>Add PRBS13-free running with precode as an option for a training pattern.</td>
<td>O</td>
</tr>
<tr>
<td>Cl 176A SC 176A.6.2 P557 L53</td>
<td>T</td>
<td>X</td>
<td>To support AUI or PMDs only providing a subset of the available PRESETs we should define a behavior in that scenario</td>
<td></td>
<td>O</td>
</tr>
</tbody>
</table>
Slavick, Jeff
Broadcom

**Comment Type**: T  **Comment Status**: X
You have self generated data you’re sending but you don’t have your self setup to send mission data yet.

**Suggested Remedy**
Remove the "No data is available," from the option 1 of Extend training bit

---

Rodes, Roberto
Coherent

**Comment Type**: T  **Comment Status**: X
Adding explanation on allocation for penalties calculation.

**Suggested Remedy**
Use same approach than for the inserion loss adding a note in the LR4 value with the text:"Allocation for penalties is calculated using an additional penalty of 0.7dB from DGD, and 0.4dB from MPI"

---

Rodes, Roberto
Coherent

**Comment Type**: T  **Comment Status**: X
Change spec format consistent with FR4

**Suggested Remedy**
Replace 0.5+TDECQ by 0.5+Max(TECQ,TDECQ)
# Proposed Response

**Comment Type:** TR  
**Comment Status:** X  
In Figure 177–8, the input variable of state FS_LOCK_INIT is not correct. It would cause a FS lock error.

**Suggested Remedy:**

FS_LOCK_INIT state should be entered after all the 8 flows obtain their inner FEC codeword boundaries and inner FEC flow 0 is identified, when fs_lock is false.

Propose change:

- Change the input variable from `!all_synced` to `all_synced * !fs_lock`.
- Change the definition of `all_synced` from

  'A Boolean variable that is set to true when sync_flow<x> is true for all eight flows and is set to false when sync_flow<x> is false for any x.'

  to

  'A Boolean variable that is set to true when inner FEC flow 0 is identified and is set to false when sync_flow<x> is false for any x.'

  (in page 258 line 48-50)

**Response Status:** O  

---

## Proposed Response

**Comment Type:** TR  
**Comment Status:** X  
Add and update connector references as necessary. This is what is in 1.3:


**Suggested Remedy:**

Use these for now (most will be updated before this project is done):

- OSFP Octal Small Form Factor Pluggable Module, Rev 5.0, October 2, 2022
- SFF-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification for QSFP Double Density 8x Pluggable Transceivers, Rev 7.0, September 29, 2023
- SFF-8665 Rev 1.9.4, 2022-04-01, QSFP+ 4X Pluggable Transceiver Solutions
- SFF-TA-1011 Rev 1.1, 2024-04-19, Cross Reference to Select SFF Connectors and Modules
- SFF-TA-1027, Rev 1.0, 2024-04-16, QSFP2 Connector, Cage, & Module Specification
- SFF-TA-1031, Rev 1.0, 2023-06-11, SFP2 Cage, Connector, & Module Specification
- https://osfpmsa.org/specification.html
- http://www.qsfp-dd.com/specification/

Refer to these documents from 179C.

**Response Status:** O  

---

## Proposed Response

**Comment Type:** T  
**Comment Status:** X  
Don't LR4 come before LR1 (same reach, narrower) and the order goes up the page, counting the bits forward.

**Suggested Remedy:**

Swap 800GBASE-LR4 and 800GBASE-LR1

**Response Status:** O  

---
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment ID 508**

<table>
<thead>
<tr>
<th>CI 45</th>
<th>SC 45.2.1.60b</th>
<th>P65</th>
<th>L24</th>
<th># 508</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>T</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>800GBASE-DR4-2 has longer reach than 800GBASE-FR4-500</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Swap them

**Proposed Response**
Response Status O

**Comment ID 509**

<table>
<thead>
<tr>
<th>CI 45</th>
<th>SC 45.2.1.60c</th>
<th>P67</th>
<th>L21</th>
<th># 509</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
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<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>T</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>It's unfortunate that 800GBASE-ER1 and 800GBASE-ER1-20 are in different registers, and 800GBASE-ER1-20, having less reach, should come first</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Move 800GBASE-ER1 from 1.73.14 to 1.74.0. 1.73.14 goes back to reserved - maybe it can be used for 800GBASE-LR20-1 ;)

**Proposed Response**
Response Status O

**Comment ID 510**

<table>
<thead>
<tr>
<th>CI 116</th>
<th>SC 116.5</th>
<th>P107</th>
<th>L46</th>
<th># 510</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>T</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>A new footnote has appeared &quot;At the PCS receive input, 1 UI is equivalent to 1 bit.&quot; attached to an unchanged number. There is no equivalent footnote for Table 116-8. In 802.3, &quot;bit&quot; means MAC bit. I don't know what point the footnote is making - that PCS lanes use binary signalling not PAM4? Nor why it is here. If it were kept, it should say &quot;1 bit on a PCS lane&quot; or similar.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Delete footnote f

**Proposed Response**
Response Status O

**Comment ID 511**

<table>
<thead>
<tr>
<th>CI 179</th>
<th>SC 179.9.4</th>
<th>P309</th>
<th>L44</th>
<th># 511</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
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</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>T</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>AC common-mode voltages are not as large as this in practice, even at 200G/lane</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Reduce both AC common-mode voltage limits for CR, KR, C2C and C2M.

**Proposed Response**
Response Status O

**Comment ID 512**

<table>
<thead>
<tr>
<th>CI 179</th>
<th>SC 179.9.4</th>
<th>P309</th>
<th>L46</th>
<th># 512</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Supply voltages and voltage swing trend downwards over the years. This 1200 mV max has not changed since 10GBASE-KR, a long time ago. C2M has 750 mV.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Reduce 1200 mV to e.g. 1000 mV, here, in the receiver Table 179-10 and in the text in 179.9.5.2. Reduce the steady-state voltage vF max from 0.6 V to 0.5 V. Similarly for KR and C2C.

**Proposed Response**
Response Status O

**Comment ID 513**

<table>
<thead>
<tr>
<th>CI 179</th>
<th>SC 179.9.4</th>
<th>P310</th>
<th>L27</th>
<th># 513</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dawe, Piers</td>
<td>Nvidia</td>
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</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td>TR</td>
<td><strong>Comment Status</strong></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Our way of measuring jitter doesn't work well enough with the increased max host loss over 3ck. It is not clear that it can or should be fixed. Our way of defining SNDR doesn't work correctly over host loss either. This can be fixed, but &quot;vertical and horizontal noise&quot; act together to degrade BER: more of one goes with less of the other.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Suggested Remedy**
Delete the SNDR and jitter specs. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.

**Proposed Response**
Response Status O
## IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>179</td>
<td>179.9.4.6</td>
<td>P315</td>
<td>15</td>
<td>514</td>
<td>514</td>
</tr>
<tr>
<td></td>
<td>Dawe, Piers</td>
<td>Nvidia</td>
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<td></td>
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</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td><strong>Comment Status</strong></td>
<td><strong>Proposed Response</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TR</td>
<td>X</td>
<td></td>
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</tr>
</tbody>
</table>

**As explained in other comments, up to 3ck the SNDR spec acted together with the jitter spec to protect the link performance - but we don’t have a satisfactory way of measuring jitter at today’s speeds and losses, and separating the two things out "leaves margin on the table".**

**Suggested Remedy**
Delete the SNDR section. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C.

**Proposed Response**
Response Status O

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>180.6.2</td>
<td>P354</td>
<td>35</td>
<td>517</td>
<td>517</td>
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<tr>
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<td>Dawe, Piers</td>
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<tr>
<td><strong>Comment Type</strong></td>
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<td><strong>Proposed Response</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>T</td>
<td>X</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**In 802.3db we acknowledged that single-lane PMDs are often packaged in multilane modules, and subject to much the same crosstalk as multilane PMDs.**

**Suggested Remedy**
Delete footnote e, "No aggressors needed for 200GBASE-DR1." In 180.8.13 Stressed receiver sensitivity, add "For a receiver in a multilane device, the OMA outer of the aggressor lanes is specified in Table 180-8."

**Proposed Response**
Response Status O

<table>
<thead>
<tr>
<th>Cl</th>
<th>SC</th>
<th>P</th>
<th>L</th>
<th>#</th>
<th>Comment ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>180.8.11</td>
<td>P365</td>
<td>51</td>
<td>518</td>
<td>518</td>
</tr>
<tr>
<td></td>
<td>Dawe, Piers</td>
<td>Nvidia</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Comment Type</strong></td>
<td><strong>Comment Status</strong></td>
<td><strong>Proposed Response</strong></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>T</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**"The upper -3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate": I believe this dates back at least to the first Fibre Channel, ~1 Gb/s, long before adaptive equalisers that optimise the receiver bandwidth. We have a RIN spec to help the accuracy of the TDECQ spec, which is the actual assessment of signal quality. Gigabit Ethernet now uses 937.5 MHz, 75% of the signalling rate. Measuring a peaky noise spectrum in too much bandwidth gives a flattering average, which is not what we want.**

**Suggested Remedy**
Change the bandwidth for RIN measurement to be the same as the TDECQ receiver’s BT4 filter (50% of signalling rate ~ 53.1 GHz) or 75%, or something in between.

**Proposed Response**
Response Status O
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

**Comment ID 519**

**Cl 180 SC 180.8.13 P366 L25 # 519**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

More exceptions - I found these in 167.8.14

SuggestedRemedy

The applied sinusoidal jitter is specified in 180.8.13.1.  
The values of overshoot/undershoot and transmitter power excursion of the stressed receiver conformance signal are within the limits specified in Table 180-7.  
For a receiver in a multilane device, the OMA outer of the aggressor lanes is specified in Table 180-8.

Add a sinusoidal jitter section following 167.8.14.1 (but see next comment).

**Proposed Response**

Response Status O

---

**Comment ID 520**

**Cl 180 SC 180.8.13 P366 L26 # 520**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

If the rising LF jitter slope for 113.4375 GBd is based on 4 MHz, 0.05 UI pk-pk, the LF jitter slope for 106.25 GBd must match in absolute time units (not UI) so that there is not an unbounded buffering requirement (or one jitter slope can be modified in shape).

SuggestedRemedy

In the FECi clauses, instead of 2e5/f, 0.05 UI, use 2.13e5/f, 0.053 UI.  Or, here and in the other non-FECi PMD and PMA clauses, use 1.875e5/f, 0.047 UI.

**Proposed Response**

Response Status O

---

**Comment ID 521**

**Cl 180 SC 180.10 P368 L11 # 521**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

Bit number should match number of lanes

SuggestedRemedy

Change 1.9.4 to 1.9.n.  Below, change 1.10.4 to 1.10.n.  Similarly in other clauses.

**Proposed Response**

Response Status O

---

**Comment ID 522**

**Cl 176E SC 176E.5.2 P633 L33 # 522**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

**Proposed Response**

Response Status O

---

**Comment ID 523**

**Cl 176 SC 176E.5.2 P636 L49 # 523**

Dawe, Piers  
Nvidia  

Comment Type TR  
Comment Status X

"within the time interval t_s +/-0.05 UI and with accumulated probability for each sample weighted by the function w(t) defined by Equation (176E-4)": this makes the measurement too tolerant to jitter.

SuggestedRemedy

Remove the Gaussian weighting function w(t), increase +/-0.05 to +/-0.07, same as TDECQ.  This will make VEC look worse, but will be a better measurement to protect the link.  Use this method for CR also, with "software channel" ("far end eye measurement") as appropriate.

**Proposed Response**

Response Status O

---

**Comment ID 524**

**Cl 179A SC 179A.4 P663 L50 # 524**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

Defining a "host channel" that includes most of the host but leaves out the connector, is not helpful.  The connector is part of the host and its loss is significant.

SuggestedRemedy

Define the recommended channel either from pad TP0d to the outside of the connector, or more usefully, from TP0d to TP2 (the loss from outside of the connector to TP2 is the HCB loss which will be well defined)

**Proposed Response**

Response Status O

---

**Comment ID 525**

**Cl 179A SC 179A.4 P663 L50 # 525**

Dawe, Piers  
Nvidia  

Comment Type T  
Comment Status X

**Proposed Response**

Response Status O
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comments

Comment ID 525

Cl 179C SC 179C.1 P680 L15 # 525
Dawe, Piers Nvidia

Comment Type T Comment Status X

MDIs are mechanical entities. For 106.25 GBd operation, there are SFP2 (SFF-TA-1031) and QSFP2 (SFF-TA-1027). Any "SFP224" would be an SFP2 module or cable end with 200G-capable circuitry. But this annex is for the MDI, not the circuitry. Similarly for "QSFP224" and QSFP2.

Suggested Remedy

Correct the names. Add references to SFF-TA-1011 which relates the names and specs for the SNIA-SFF modules, and SFF-8665, which defines the components of a QSFPx "solution".

Proposed Response Response Status O

Comment ID 526

Cl 179C SC 179C.1 P680 L17 # 526
Dawe, Piers Nvidia

Comment Type TR Comment Status X

Refer to the specification for each connector type where each is first mentioned. See another comment against 1.3 for the reference docs.

Suggested Remedy

Per comment

Proposed Response Response Status O

Comment ID 527

Cl 179C SC 179C.2.3 P688 L35 # 527
Dawe, Piers Nvidia

Comment Type T Comment Status X

This says "the mechanical interface". The mechanical spec is SFF-TA-1027, QSFP2. It is a standard, not an MSA.

Suggested Remedy

Change "the TBD MSA" to "SFF-TA-1027".

Proposed Response Response Status O

Comment ID 528

Cl 179C SC 179C.2.4 P689 L35 # 528
Dawe, Piers Nvidia

Comment Type T Comment Status X

There is no QSFP-DD1600 TBD MSA document. QSFP-DD1600 is defined in the singular QSFP-DD MSA document

Suggested Remedy

Change "the QSFP-DD1600 TBD MSA" to "the QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification".

Proposed Response Response Status O

Comment ID 529

Cl 179C SC 179C.2.5 P690 L21 # 529
Dawe, Piers Nvidia

Comment Type T Comment Status X

There is no OSFP1600 TBD MSA document. OSFP1600 is defined in the singular OSFP MSA document, particularly section 4.

Suggested Remedy

Change "the OSFP1600 TBD MSA" to "the OSFP Octal Small Form Factor Pluggable Module specification" or "section 4 of the OSFP Octal Small Form Factor Pluggable Module specification".

Proposed Response Response Status O

Comment ID 530

Cl 116 SC 116.1.4 P94 L6 # 530
Rechtman, Zvi Nvidia

Comment Type T Comment Status X

The comment refers to Table 116–3:


It will be beneficial to add a note about the conditions which allow/require implementation of BM_PMA and SM_PMA

Same apply to Table 116–3a, Table 116–4, Table 169–2

Suggested Remedy

Add a footnote labeled 'b' next to the 'O' marking for 200GBASE-R SM-PMA in the entries for 200GBASE-KR2, 200GBASE-KR4, 200GBASE-CR2, and 200GBASE-CR4. The footnote 'b' should state: Applicable only when 200GAUI-1 C2C interface is used within the PHY

Proposed Response Response Status O
The comment refers to Table 116–8. There is an additional logical skew present in the 200GBASE-R and 400GBASE-R2 BM_PMA of 2 RS-FEC CWs. These skew values should not be included in the skew budget calculations for this table. To prevent misinterpretations, an explicit note is required.

Suggested Remedy

Insert a note in Table 116–8 that states: 'The additional 2 RS-FEC CWs logical skew in clause 176 BM_PMA for 200GBASE-R and 400GBASE-R should not to be factored in the skew budget calculations for this table.'

Proposed Response

Response Status O

The comment refers to Table 169–4. The Inner-FEC delay appears to be missing from the table.

Suggested Remedy

Add 800GBASE-R inner FEC (values are TBDs).

Proposed Response

Response Status O

The comment refers to Figure 176–2. The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols. The intention is to delay the odd (Tx) and even (Rx) PCSLs by 136 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.

Suggested Remedy

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 136 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 136 symbols".

Proposed Response

Response Status O

There is reference in the text to lock process in Figure 119-12. However, there are exceptions to Figure 119-12 as outlined in 176.5.1.6. It can be beneficial to refer to 176.5.1.6 which include both the reference to Figure 119-12 and the list of exceptions list.

Suggested Remedy

Add a reference to 176.5.1.6 instead of Figure 119-12.

Proposed Response

Response Status O
The comment refers to Figure 176-4. The diagram represents a specific skew case between PCS lanes, for instance in the absence of skew between the original PCS lanes, the "first" symbol A might be created by different A codeword which should be denote by A'.

**Suggested Remedy**
- **Option 1:**
  Modify only the first A symbol of the odd PCS lanes to be A'.
- **Option 2:**
  Split the drawing into two: one for 200GBASE-R and another for 400GBASE-R. Then, add index numbers to the A, B symbols.
  This could make it easier to understand the drawings and the roles of the symbols in each context.

**Proposed Response**

**Response Status**

---

The comment refers to Figure 176-5. The diagram represents a specific skew case between PCS lanes. For instance in the absence of skew between the PCS lanes in the PMA:IS_UNITDATA_0:7.request primitive, the first symbol of A' of the odd PCS lane should be marked as A'' because of the additional one symbol delay prior to the 136 symbols delay

**Suggested Remedy**
- **Option 1:**
  Modify only the first A' symbol of the odd PCS lanes to be A''.
- **Option 2:**
  Split the drawing into two: one for 200GBASE-R and another for 400GBASE-R. Then, add index numbers to the A, B symbols.
  This could make it easier to understand the drawings and the roles of the symbols in each context.

**Proposed Response**

**Response Status**

---

The sentence "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords x 544 symbols per codeword / 8 PCS lanes = 136 symbols)." can be misinterpreted:

136 symbol delay x 4 odd PCS lanes = 544 symbols delay in total (not 2 RS-FEC codewords delay)

**Suggested Remedy**
- Remove "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords x 544 symbols per codeword / 8 PCS lanes = 136 symbols)."
- Modify: "Adding the two codeword delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."
- To: "Adding the 136 symbol delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."

**Proposed Response**

**Response Status**

---

The comment refers to Figure 176–8—PMA receive symbol-pair lock state diagram. The state diagram is defined as single state machine per the entire PMA. However, each PMA lane may have a different reference skew, leading to varying SLIP operation requirements per PMA lane (e.g. one PMA lane doesn't require SLIP because all PCS lanes of that lane are locked, but other PMA lane still need to skew to find the 20 symbol bit boundaries) therefore the state diagram should be define per PMA lane and not per PMA.

**Suggested Remedy**
- Modify the state diagram per PMA lane and not per PMA, this include change in the variables to be defined per <y>:
  - `restart_lock_demux<y>`
  - `symbol_pair_lock_demux<y>`
  - `start_symbol_pair_lock_counter_demux<y>`
  - `symbol_pair_lock_demux<y>`

**Proposed Response**

**Response Status**

---

## Comment Details

**Comment ID:** 538

**Page:** 99 of 118

**Date:** 5/3/2024 10:09:29 AM

**Type:** Technical required

**Comment Status:** Dispatched

**Response Status:** Open

**Sort Order:** Comment ID
Comment Type: TR

The comment refers to Figure 176–11.

The functions of "Delay odd PCSLs by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols. The intention is to delay the odd (Tx) and even (Rx) PCSLs by 68 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.

Same apply to Figure 176–13

Suggested Remedy

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 68 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 68 symbols"

Comment Type: TR

The paragraph refers only to the case of PMD control function operation, need to refer to Annex 176A for all electrical interfaces

Suggested Remedy

Replace:
"If the PMA is connected to the service interface of an xBASE-CRn or xBASE-KRn PMD and training is enabled by the management variable mr_training_enable (see 136.7), then precoder_tx_out_enable_i and precoder_rx_in_enable_i shall be set as determined by the PMD control function in the LINK_READY state on lane i (see 136.8.11.7.5 and Figure 136–7). The method by which the MD control function affects these variables is implementation dependent."

With:
"If the PMA support the Control function and start-up protocol for electrical interfaces and training is enabled by the management variable mr_training_enable (see Annex 176A), then precoder Tx_out_enable_i and precoder Rx_in_enable_i shall be set as determined by the control function in the LINK_READY state on lane i (see 176A.10.4 and Figure 176A–6). The method by which the PMA control function affects these variables is implementation dependent."

Comment Type: TR

The operation of precoding after the completion of the start-up protocol is missing

Suggested Remedy

Add the following text:
"If the LINK READY state is entered with local_tp_mode set to "PAM4 with precoding", then the PMA shall transmit all subsequent data on the corresponding lane with precoding (see 176.9.1.2).
If the LINK READY state is entered with remote_tp_mode set to "PAM4 with precoding", then the PMA shall subsequently received data on the corresponding lane includes precoding (see 176.9.1.2)"

Proposed Response

Response Status: O
### Comment 543

**Cl 177** | **SC 177.1.4** | **P250** | **L32** | 
---|---|---|---|
Rechtman, Zvi | Nvidia |

**Comment Type T** | **Comment Status X**

The comment refers to Figure 177–2.

There is a footnote that PAM4 decoding is optional in case of soft decoding.

However, the DataPath is defined using bit streams, also the FEC:IS_UNITDATA_i.indication primitives has two value of 0 or 1, therefore PAM4 decoding must to take place.

**Suggested Remedy**

Either remove the footnote, or elaborate on the intention of this footnote.

**Response**

**Response Status O**

### Comment 544

**Cl 177** | **SC 177.4.1** | **P251** | **L51** | 
---|---|---|---|
Rechtman, Zvi | Nvidia |

**Comment Type TR** | **Comment Status X**

The values of Q and the description of the Convolutional interleaver functionality doesn't match the adopted values in he_3dj_01_2307.pdf.

The values should be:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

**Suggested Remedy**

Modify the Q values to:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

**Response**

**Response Status O**

### Comment 545

**Cl 177** | **SC 177.4.1** | **P256** | **L50** | 
---|---|---|---|
Rechtman, Zvi | Nvidia |

**Comment Type TR** | **Comment Status X**

The description in "The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay" seems to represent block interleave and not convolutional interleave.

**Suggested Remedy**

Modify to:

"The convolutional interleaver is composed of 3 delay lines.

For 200GBASE-R the first line (line0) delays the PHYs data by 4x2x192 = 1,536 RS-FEC Symbols, the second line (line1) by 4x1x192 = 768 RS-FEC symbols and the last line (line3) adds no delay.

For 400GBASE-R the first line (line0) delays the PHYs data by 4x2x96 = 768 RS-FEC Symbols, the second line (line1) by 4x1x96 = 384 RS-FEC symbols and the last line (line3) adds no delay.

For 800GBASE-R the first line (line0) delays the PHYs data by 4x2x48 = 384 RS-FEC Symbols, the second line (line1) by 4x1x48 = 192 RS-FEC symbols and the last line (line3) adds no delay.

For 1.6TBASE-R the first line (line0) delays the PHYs data by 4x2x24 = 192 RS-FEC Symbols, the second line (line1) by 4x1x24 = 96 RS-FEC symbols and the last line (line3) adds no delay."
The input and output round-robin operation is defined relatively to the delay/buffering size of each lane. However, there are lines index that represent the delay and simplify the definition.

**Suggested Remedy**

Change:

"The input data round-robs between the three delay lines beginning with the eight RS-FEC delay line, then the four RS-FEC delay line and lastly the zero delay line. The output of the convolutional interleaver round-robs between the three delay lines receiving one RS-FEC symbol-quartet from each at a time beginning with the eight RS-FEC delay line, then four RS-FC delay line, and lastly the zero delay line"  

To:

"The input data round-robs between the three delay lines beginning with line0, then line1 delay line and lastly line2. The output of the convolutional interleaver round-robs between the three delay lines receiving one RS-FEC symbol-quartet (4 symbols) from each at a time beginning with line0, then line1, and lastly line2"  

**Proposed Response**  
Response Status: O

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The 128,120 Hamming code is very sensitive to error propagation since it can correct up to one error in hard decoding and three errors in soft decoding. Hence, precoding is required.

**Suggested Remedy**

Add precoding, and use the same definition of precoding similar to 176.9.1.2.

**Proposed Response**  
Response Status: O
The comment refers to Figure 176A–6—Interface control state diagram. The RECOVERY state coupled with the absence of timeouts, introduces a new challenge in identifying marginal performance cases. These cases may lead to repeated transitions between TRAIN_LOCAL/TRAIN_REMOTE/SEGMENT_READY state to/from RECOVERY state in scenarios of alternating local_tf_lock.

A possible solution is to limit the number of RECOVERY events by counting and limiting the number of transitions to the RECOVERY state.

**Proposed Remedy**

Define a new counter: "recovery_event_count". This counter increments each time the control state diagram transitions into the RECOVERY state.

**Effects on the state diagram:**

The "recovery_event_count" should be initialized to 0 in the "SEND_TRAINING" state. Upon entering the RECOVERY state, the "recovery_event_count" should be incremented by 1.

**State diagram transition change:**

The transition condition from the RECOVERY state to the FAIL state needs to be modified as follows:

Change "recovery_timer done" to "recovery_timer done || recovery_event_count > X", where X is 5 (or to be determined).

### Proposed Response

Rechtman, Zvi  
Nvidia

**Comment Type**  T  
**Comment Status**  X

**Comment** There is a spurious '<' within the transition condition from the state TRAIN_LOCAL to the state TRAIN_REMOTE.

**Proposed Remedy**

Suggest that 'local_tf_lock< local_rx_ready' should read 'local_tf_lock < local_rx_ready'.

### Proposed Response

Law, David  
HPE

**Comment Type**  T  
**Comment Status**  X

**Comment** Subclause 176A.10.1 'State diagram conventions' says that 'The notation used in the state diagrams follows the conventions of 21.5.'; however subclause 21.5 does not address the operation of timers.

**Proposed Remedy**

Suggest that the text 'All timers operate in the manner described in 14.2.3.2.' be inserted as the new second sentence of the second paragraph of subclause 176A.10.1.

### Proposed Response

Law, David  
HPE

**Comment Type**  T  
**Comment Status**  X

**Comment** The arrow pointing to the Interface A 'Driver' block and arrow pointing from the Interface B 'CDR' block both seem to be pointing in the wrong direction.

**Proposed Remedy**

Reverse the direction of both arrows.
IEEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

**Comment ID: 555**

Law, David  
**HPE**

**Comment Type: T**  
**Comment Status: X**

Figure 176A–5 'Retimer reference model' shows the data multiplexor driven by the tx_mode value, with the multiplexor select set to 0 when tx_mode = training and set to 1 when tx_mode = data. Subclause 176A.10.2.1 'Variables', however, defines three values for tx_mode, training, local_pattern and data. Figure 176A–5, therefore, does not define the multiplexor select value for when tx_mode = local_pattern.

**Suggested Remedy**

Update the figure to reflect the third value of tx_mode and the local pattern generator for each interface.

**Proposed Response**  
**Response Status: O**

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**Comment ID: 556**

Law, David  
**HPE**

**Comment Type: T**  
**Comment Status: X**

The WAIT_ADJACENT to SWITCH_CLOCK transition condition uses the variable mr_training_enabled, however subclause 176A.10.2.1 'Variables' defines the variable mr_training_enable, not mr_training_enabled.

**Suggested Remedy**

Change the transition condition ' (!mr_training_enabled + segment_ready) * ...' to read '(!mr_training_enable + segment_ready) * ...'.

**Proposed Response**  
**Response Status: O**

---

**Comment ID: 557**

Law, David  
**HPE**

**Comment Type: T**  
**Comment Status: X**

Subclause 176A.10.1 'State diagram conventions' says that 'The notation used in the state diagrams follows the conventions of 21.5.' Subclause 21.5.3 'State transitions' says 'The following terms are valid transition qualifiers: ' and item d) says 'An unconditional transition: UCT'. As a result, it is not necessary to expand UCT on it's first use in Annex 176A.

**Suggested Remedy**

Change the text 'UCT (unconditional transition)' to read 'UCT'.

**Proposed Response**  
**Response Status: O**
Comment #: 560

Law, David
HPE

Comment ID 184 SC 184.6.5 P462 L22

Comment Type T Comment Status X

N (the number of consecutive PS symbols matching the expected value for a given polarization stream required to enter frame lock), and M (the number of consecutive PS symbols that don’t match the expected value for a given polarization stream required to exit frame lock) used in Figure 184–9 'DSP lock state diagram' aren’t defined in subclause 184.6 'Inner FEC state diagrams' or its subclauses.

Suggest that these values should be defined in one place (I assume in subclause 184.5.4 ‘DSP frame synchronization and pilot removal’ which includes the text 'The values of N and M are TBD.'), with a pointer to this subclause elsewhere.

Suggested Remedy

[1] Insert a new subclause 184.6.5 'Constants' as follows, renumbering the following subclause.

184.6.5 Constants

M
The number of consecutive PS symbols that fail to match the expected value for a given polarization stream required to exit frame lock (see 184.5.4).

N
The number of consecutive PS symbols matching the expected value for a given polarization stream required to enter frame lock (see 184.5.4).

[2] In subclause 184.6.2 'Variables', change the text 'it is set to true when TBD PS symbols ...' to read 'it is set to true when M PS symbols ...' in the variable 'restart_lock' description.

Proposed Response Response Status O

Comment #: 561

Law, David
HPE

Comment ID 176A SC 176A.2.2 P549 L9

Comment Type T Comment Status X

Subclause 176A.2.2 'Control and status fields' says that 'The control field comprises 16 bits with the structure defined in 176A.3.', yet figure 176A–1 'Training frame structure' above shows the control field comprising of 16 cells. It, therefore, appears that the field is comprised of 16 cells that convey 16 bits.

Suggested Remedy

[1] Change the first paragraph of 176A.2.2 to read 'The control field is comprised of 16 cells which convey 16 bits with the structure defined in 176A.3. The status is comprised of 16 cells which convey 16 bits with the structure defined in 176A.4.

[2] Change the last sentence of the penultimate paragraph of 176A.2.2 to read 'Within each field, the order of transmission is from bit 15 to bit 0, conveyed by cell 15 to cell 0 respectively.'.

Proposed Response Response Status O

Comment #: 562

Law, David
HPE

Comment ID 176A SC 176A.2.2 P549 L25

Comment Type T Comment Status X

Subclause 176A.2.2 says '... if a violation of the DME encoding rules is detected within the control field or the status field, the contents of both fields in that frame are ignored.' If this is requirement, suggest it should be stated using a 'shall' statement.

Suggested Remedy

Change '... the contents of both fields in that frame are ignored.' to read '... the contents of both fields in that frame shall be ignored.'.

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### Proposed Response

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### Suggested Remedy

- The first 'shall' statement in Annex 176A (normative) 'Control function and start-up protocol for electrical interfaces' is in 176A.2.3.1 'PRBS13 function'. It seems, however, that there should be 'shall' statements in relation to the entire Training frame structure.

- **Suggested Remedy**

  1. In subclause 176A.2.1, change 'The training frame marker is a run ...' to read 'The training frame marker shall be a run ...'.
  2. In subclause 176A.2.2, change 'The control field comprises ...' to read 'The control field shall be comprised of ...'.
  3. In subclause 176A.2.2, change 'The status field comprises ...' to read 'The status field shall be comprised of ...'.
  4. In subclause 176A.2.3, change 'The training pattern is the result of a ...' to read 'The training pattern shall be the result of a ...'.

### Suggested Remedy

- 176A.6.4 says that 'The variables coef_req, coef_sts, and k are defined in 176A.10.3.1.', however, 176A.10.3.1 'Variables' uses all lowercase for the coef_sts values (e.g., updated, coefficient at limit and equalization limit) and coef_req (e.g., decrement, increment) whereas 176A.10.3.1 uses all uppercase for the coef_sts values (e.g., UPDATED, COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT) and coef_req (e.g., DECREMENT, INCREMENT).

- **Suggested Remedy**

  - The formatting of the variable values defined in 176A.10.3.1 'Variables' and used in 176A.6.4 should match.

### Proposed Response

- Change 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' to read 'The coefficient status bits reflect the value of coef_sts variable generated by the coefficient update state diagram (Figure 176A–9)'.

- Change 'The last sentence of the tx_disable variable description says that the ’... output on the lane is disabled.’ is correct, the first sentence says that tx_disable ‘... controls the transmitter's output on the interface,’ and tx_disable is defined under subclause 176A.10.2 ‘Per-interface variables, functions and timers’. Suggest that the reference to ’lane’ is changed to ’interface’, or use ’all lanes of the interface’ in the variable description to reflect the segment_ready variable description immediately above.

- **Suggested Remedy**

  - Either

    1. Change the text ’... output on the lane is disabled.’ in the last sentence of the tx_disable variable description to read ’... output on the interface is disabled.’.

    or

    2. Change [1] the text ’... the transmitter's output on the interface,’ in the first sentence of both the tx_disable and tx_mode variable descriptions to read ’... the transmitter output on all lanes of the interface,’; and [2] the text ’... output on the lane is disabled.’ in the last sentence of the tx_disable variable description to read ’... output on all lanes of the interface is disabled.’.
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<td><strong>Suggest a description of what happens when the tx_disable variable is set to false is added to the variable description.</strong></td>
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<td>[1] Add 'When it is false, tx_mode controls the content of the transmitter's output on the interface.' or 'When it is false, tx_mode controls the content of the transmitter's output on all lanes of the interface.', depending on the response to my other comment, to the end of the tx_disable variable description.</td>
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<td><strong>176A.10.3.3 'Timers' is a subclause of 176A.10.3 'Per-lane variables, functions, timers and counters', yet the three times listed, quiet_timer, propagation_timer and recovery_timer are all used by the interface control state diagram. 176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of its interfaces (see 176A.9).'. As a result, it seems these timers should be moved to 176A.10.2.3 'Timers' and the descriptions should be updated to reflect that they operate on a per-interface basis.</strong></td>
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<td>[1] Move the quiet_timer, propagation_timer and recovery_timer definitions to 176A.10.2.3 'Timers' and delete 176A.10.3.3 'Timers'.</td>
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<td>[2] Change the text '... of the interface.' in the description of quiet_timer, propagation_timer and recovery_timer to read '... of the interface when tx_disable is false.'.</td>
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<td><strong>Change 'coef_sts = COEFFICIENT AT LIMIT' (COEFFICIENT misspelt) to read 'COEFFICIENT AT LIMIT'.</strong></td>
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<td><strong>See comment.</strong></td>
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<tr>
<td><strong>176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams independently for each of its interfaces (see 176A.9).', and 176A.10.4 'State diagrams' says 'The interface control state diagram (Figure 176A–6) defines the operation of the startup protocol for AUIs and PMDs'. 176A.10.4 'State diagrams', however, goes on to say, 'The interface control, frame lock and coefficient update state diagrams shall be implemented for each lane.' This doesn't seem to be in alignment with the prior text and doesn't seem to be correct.</strong></td>
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<tr>
<td>[1] Move the quiet_timer, propagation_timer and recovery_timer definitions to 176A.10.2.3 'Timers' and delete 176A.10.3.3 'Timers'.</td>
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<td>[2] Change the text '... of the interface control state diagram on a lane enters the ...' in the description of quiet_timer, propagation_timer and recovery_timer to read '... of the interface control state diagram on an interface enters the ...'.</td>
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</table>
Comment Type | T | Comment Status X
---|---|---
176A.10.3 'Per-lane variables, functions, timers and counters' says 'The device implements one instance of each of the interface control state diagrams, and the set of associated ... for each of the n physical lanes on each of its interfaces (see 176A.9). I don't think this is correct as I believe that the interface control state diagram is one for each interface of a device (see 176A.10.2), and it is the frame lock and coefficient update state diagrams that are one for each lane of each interface of a device.

**Suggested Remedy**

Change "The device implements one instance of each of the interface control state diagrams ..." to read "The device implements one instance of each of the frame lock and coefficient update state diagrams ...".

**Proposed Response**

**Response Status** O

---

Comment Type | T | Comment Status X
---|---|---
The variables local_tf_lock, remote_tf_lock, local_rx_ready and remote_rx_ready are all defined in 176A.10.3 'Per-lane variables, functions, timers and counters' and are related to a lane, yet they are used by figure 176A-6 'Interface control state diagram'. 176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams independently for each of its interfaces (see 176A.9).'.

**Suggested Remedy**

Perhaps figure 176A-6 'Interface control state diagram' should use a 'interface' version of each of these variables that are a logical AND of the respective lane variable in the case of a multi-lane interface.

**Proposed Response**

**Response Status** O

---

Comment Type | T | Comment Status X
---|---|---
The description of the local_tf_lock variable in 176A.10.3.1 says that 'The value of this variable is encoded as the "training lock" bit in the status field of transmitted training frames.'. However, there isn't a "training lock" bit defined for the training frames. Since 176A.4.3 'Receiver frame lock' says 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.' it seems that local_tf_lock is encoded in the 'Receiver frame lock' bit.

**Suggested Remedy**

Change the text '... is encoded as the "training lock" bit ...' in the local_tf_lock variable description to read '... is encoded in the "Receiver frame lock" bit ...'.

**Proposed Response**

**Response Status** O

---

Comment Type | T | Comment Status X
---|---|---
176A.10.3.1 'Receiver frame lock' says that 'When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 176A.10 are met.' It then goes on to say 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.'

176A.10 is 'Variables, functions, counters, and state diagrams', so I wonder if the reference should be to 176A.8 'Handshake timing'? In addition, I don't believe the variables training and local_tf_lock are conditioned on the response time requirements specified in 176A.10 being met, at least I didn't see it in their descriptions.

**Suggested Remedy**

In 176A.4.3 change the text '... response time requirements specified in 176A.10 are met.' to read '... response time requirements specified in 176A.8 are met.' and the text '... and is not set to 1 until training and local_tf_lock are both true.' To read '... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.10 can be met.'

**Proposed Response**

**Response Status** O
The UPDATE_IC function is called in the OUT_OF_SYNC state of the Figure 176A–9 Coefficient update state diagram. The UPDATE_IC function uses the ic_req variable to set the coefficients (see 176A.6.2), and the ic_req variable is derived from the 'initial condition request' bits from the control field of the received training frames (see 176A.10.3.1).

Since, however, the OUT_OF_SYNC state is entered during reset (reset or mr_restart set true), it would seem unlikely that training frames are being received. If that is the case, it isn't clear what the value of the ic_req variable is, and therefore what the coefficients should be set to.

176A.6.2 says that 'The transmitter equalizer is set to preset 1 upon entry to the QUIET state of the interface control state diagram.' Since the QUIET state of the Interface control state diagram is also entered during reset, it seems the coefficients should be set to preset 1 when the Coefficient update state diagram is in the OUT_OF_SYNC state.

Suggested Remedy

1. Delete the first sentence of the ic_req definition in 176A.10.3.1.
2. Add the text 'If the Coefficient update state diagram is in the OUT_OF_SYNC state ic_req is set to preset 1. Otherwise, it is derived from the "initial condition request" bit of the control field of received training frames on the correspondent lane of the interface.' to the end of the ic_req definition in 176A.10.3.1.

Proposed Response
The use of the terms 'segment' and 'link' in Annex 176A, for example in 176A.1 where it says, 'in single-segment or multiple-segment links', are problematic.

IEEE Std 802.3 subclause 1.4.505 'segment' defines it as 'The medium connection, including connectors, between Medium Dependent Interfaces (MDIs) in a CSMA/CD local area network.' Subclause 1.4.372 'link' defines it as 'The transmission path between any two interfaces of generic cabling. (From ISO/IEC 11801.).'

As a result, I believe it would only be correct to call an electrical channel between two PMD sublayers a 'segment'. I do not believe that the electrical channel between any other combinations of sublayers is a 'segment'.

---

Minimum transmit power specification has a big impact on coherent module designs. This has been defined in the initial proposals as a specification on the average power following other coherent physical layer specifications defined for DWDM systems. However, there is opportunity for a 800GBASE-LR1 PMD to change this in a way which can relax module transmit specifications.

Define the minimum transmit power specification to be defined per lane instead of average. See https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for an initial proposal based on this concept. Defining the power per lane provides an opportunity to relax lane mismatch specs.

---

The draft contains separate specifications of X-Y power imbalances and I-Q imbalance. However, there is an opportunity for a 800GBASE-LR1 PMD to change this in a way which can relax module transmit specifications.

Having a separate X-Y and I-Q imbalance specification splits the imbalance power budget and results in a tighter specification than necessary. These specifications should be combined into a single lane-to-lane imbalance specification. See https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for an initial specification methodology proposal.
### Proposed Response

**Cl 185 SC 185.5.2 P478 L15 # 580**

Kota, Kishore
Marvell Semiconductor

**Comment Type** TR

**Comment Status** X

**Suggested Remedy**

Average receiver power (min) and the per-lane transmit power (min) specifications should be tied to an appropriate transmit quality metric similar to the TDECQ specifications in other IMDD clauses.

**Suggested Remedy**

See https://grouper.ieee.org/groups/802/3/dj/public/24_01/kota_3dj_01a_2401.pdf and https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for initial proposals on how to tie the RX sensitivity and TX power specifications with a transmit quality metric. This provides flexibility to allow module designers to explore design tradeoffs to simplify designs in ways which can benefit end users.

**Proposed Response**

**Response Status** O

---

**Cl 00 SC 0 P0 L0 # 581**

Brown, Matt
Alphawave Semi

**Comment Type** T

**Comment Status** X

**Suggested Remedy**

In the past, we have included all previously defined AUI for each new PHY type defined. Given that the PMA multiplexing methods were consistent this was simple to support. Now that we have switched to a different PMA multiplexing method (RS-FEC symbol) things are getting more complicated.

**Suggested Remedy**

For each PHY new 200 Gb/s per lane or higher PHY type, include only one or two previous generations of AUI. Specifically, the new PHY types defined in 802.3dj indication only 100 Gb/s per lane and 200 Gb/s per lane AUIs as being optional within a PHY. Perhaps, also include 50 Gb/s per lane AUIs as well.

**Proposed Response**

**Response Status** O

---

**Cl 177 SC 177.4.7.2 P256 L13 # 582**

Ghiasi, Ali
Ghiasi Quantum/Marvell

**Comment Type** T

**Comment Status** X

**Suggested Remedy**

Pre-coding was shown on riani_3dj_01a_2303 FECI baseline that when was adopted, and pre-coding is essential for FECi PMDs.

**Suggested Remedy**

Please insert text for pre-coder in this sub-clause. as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT. Without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error. See Ghiasi/Riani May-24 presentation on the need for pre-coder

**Proposed Response**

**Response Status** O

---

**Cl 176D SC 176D.2 P596 L32 # 583**

Ghiasi, Ali
Ghiasi Quantum/Marvell

**Comment Type** T

**Comment Status** X

**Suggested Remedy**

Functional block diagram shown for C2C indicate ball-ball specifications

**Suggested Remedy**

C2C component should be called C2C device and change the TP0 to TP0d and TP5 to TP5d.

**Proposed Response**

**Response Status** O

---

**Cl 176D SC 176D.1 P595 L16 # 584**

Ghiasi, Ali
Ghiasi Quantum/Marvell

**Comment Type** T

**Comment Status** X

**Suggested Remedy**

C2C loss is TBD

**Suggested Remedy**

Assuming 28 dB budget and package A length ~300 mm and ~125 mm for package B

**Proposed Response**

**Response Status** O
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### Proposed Response

- **Cl 179A.4**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - Host designated losses of 6.5, 11.5, and 16.5 are for TP0d to TP2
  - **Suggested Remedy**
    - Move the losses to the TP0d to TP2 column
    - Min host loss is the MCB loss of 2.8 dB
    - Max loss is dependent on actual package loss and should be removed
  - **Response Status**: O

- **Cl 179A.5**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - MCB via allowance and HCB are TBD
  - **Suggested Remedy**
    - See Ghiasi C2M May-24 presentation
    - MCB via = 0.8 dB
    - HCB=3.8 dB to allow practical implementations
  - **Response Status**: O

- **Cl 182.7.3.1.1**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - To support breakout, loopback, and OAN/OLT connecto should be labled
  - **Suggested Remedy**
    - DR2-2 connector should be labeled as Tx1Tx2 ------ Rx2Rx1
  - **Response Status**: O

- **Cl 182.7.3.1.2**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - To support breakout, loopback, and OAN/OLT connecto should be labled
  - **Suggested Remedy**
    - DR2-4 connector should be labeled as Tx1Tx2Tx3Tx4 ------ Rx4Rx3Rx2Rx1
  - **Response Status**: O

- **Cl 182.7.3.1.3**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - To support breakout, loopback, and OAN/OLT connecto should be labled
  - **Suggested Remedy**
    - DR2-8 connector should be labeled as Tx1Tx2Tx3Tx4Tx5Tx6Tx7Tx8
    - Rx8Rx7Rx6Rx5Rx4Rx3Rx2Rx1
  - **Response Status**: O

- **Cl 180.7.3.1.1**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - To support breakout, loopback, and OAN/OLT connecto should be labled
  - **Suggested Remedy**
    - DR2-2 connector should be labeled as Tx1Tx2 ------ Rx2Rx1
  - **Response Status**: O

- **Cl 180.7.3.1.2**
  - **Ghiasi, Ali**
  - Ghiasi Quantum/Marvell
  - **Comment Type**: T
  - **Comment Status**: X
  - To support breakout, loopback, and OAN/OLT connecto should be labled
  - **Suggested Remedy**
    - DR2-4 connector should be labeled as Tx1Tx2Tx3Tx4 ------ Rx4Rx3Rx2Rx1
  - **Response Status**: O

**Note:**

- **TYPE:** TR/technical required
- **ER:** editorial required
- **GR:** general required
- **T:** technical
- **E:** editorial
- **G:** general
- **COMMENT STATUS:** D/dispatched
- **A:** accepted
- **R:** rejected
- **RESPONSE STATUS:** O/open
- **W:** written
- **C:** closed
- **Z:** withdrawn
- **SORT ORDER:** Comment ID

**Comment ID:** 591

**Page:** 112 of 118

**Comment Date:** 5/3/2024 10:09:29 AM
EEE P802.3dj D1.0 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 1st Task Force review comment

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<td>Cl 180 SC 180.7.3.1.3</td>
<td>To support breakout, loopback, and OAN/OLT connectro should be labled</td>
</tr>
</tbody>
</table>
| Cl 176 SC 176.5.1.4.2 | Is there anything preventing an implementation from performing a full deskew at the Rx PMA? It is not technically required, but does not cause any adverse functional effects. A full deskew at the Rx SM-PMA would NOT change end-to-end latency, since the skew is all untimately undone at the Rx PCS. A deskew upstream would simply offload the deskew from the Rx PCS. Implementations with a SM-PMA attached to an RxPCS will undoubtedly perform the Alignment marker lock only once (not once in the PMA and again in the PCS). AM-lock plus deskew is a very natural coupling of functions. |}

| Cl 176 SC 176.5.1.4.2 | Add the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2): After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before the would not have and adverse functional effects. |}

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In the AM lock and deskew clauses, is a full deskew not necessary? The goal of the Clause 176 PMA, if I understand correctly, is that at the output lane(s), each set of 4 consecutive 10-bit symbols must come from 4 different RS-FEC codewords. In the current draft, this is not achieved.

Without skew, everything works because the delay is in the same direction as the FEC CW delay. But with n*20b of skew, where some odd PCSLs arrive before even PCSLs, after the 10bit delay on odd PCSLs, (Clause 176.5.1.3.4) and the 2 CW delay (Clause 176.5.1.3.4), there will still be a period of overlap where symbols from the same FEC codeword appear at the same time. Symbols from the same RS_FEC CW can thus appear within 2 symbols after the output mux.

Before skew (showing boundary between FEC words 1 and 2):
PCSL0:       B2 A2 B1 A1 B1 A1
PCSL1:       A2 B2 A1 B1 A1 B1

20-bit skew: PCSL1 arrives before PCSL0 (when PCSL0 is finishing A1/B1, PCSL1 has already started A2/B2)
PCSL0:       B2 A2 B1 A1 B1 A1
PCSL1:       A2 B2 A1 B1 A1 B1

10-bit delay on odd lane (Clause 176.5.1.3.4):
PCSL0:       B2 A2 B1 A1 B1 A1
PCSL1:       A2 B2 A1 B1 A1 B1

2 FEC CW delay on odd lane (Clause 176.5.1.3.4):
PCSL0:       B2 A2 B1 A1 B1 A1
PCSL1:       A1 B1 A0 B0 A0 B0
-> B1s line up on PCSL 0 and 1 for one 8:1 two-symbol mux cycle.

Adding a "full deskew" may not be too costly.
Or, is this potential overlap due to skew understood and planned for in the AUI/PMD loss budgets?

Consider requiring a full deskew instead of the 20/40 bit deskew in clauses (176.5.1.3.1, 176.6.1.2.1, 176.7.1.2.1, 176.8.1.2.1).

Has any thought been put into how to calculate the path data delay values (MII-MDI latencies for timestamping) for the SM-PMAs? For bit-mux PMAs, it is very simple - i.e. it is all implementation delay, since the intrinsic delay from bit muxing/demultiplexing is negligible. But at first glance, determining the latency across the Clause 176 PMA looks like more of a challenge.

a. I don't believe that the intrinsic (i.e. non-implementation) delay is deterministic, due to the partial deskew.

b. But apart from the partial deskew, the latency across the SM-PMA should be deterministic using the principles in Annex 90A.7 (max latency value used for Tx path data delay, min latency value used for Rx path data delay).

c. Traditionally, how to calculate the delays through the PHY layers has been an implementation concern, but this is because the calculation was straightforward at lower rates. At 200Gbps lanes, the standard does not have the luxury of being able to ignore this. If it is overly complicated or ambiguous, and opposite ends of a link do not implement it in the same fashion, the system Time Synchronization will be impaired.

Consider a note in Clause 176 (or next to the PMA path data delay MDIO registers - 45.2.1.176, 45.2.1.177) that the path data delay values for the SM-PMA should be calculated via the method in Annex 90A.7.

I don't think it is necessary, but if a more detailed explanation is deemed useful, then a subclause could be added to Clause 90.7 spelling out explicitly how the path data delay values should be calculated for the SM-PMA.
Skew in series within the PHY sub-layers may not have deterministic sum, making accurate path data delay calculation impossible. See Annex 90A.6 for a more detailed explanation. Towards the MDI, the transmit SM-PMA function should thus have the option to undo any skew introduced by the Tx PCS layer and AUI links. (i.e. do a full de-skew).

In the Rx direction, the same problem exists. If the SM-PMA does not do a full deskew, then the remaining skew, in series with skew from other layers in the PHY (from AUIs, for example) and from the medium, will have a non-deterministic sum. Adding an option for the SM-PMA to do a full deskew (not just a 20/40-bit deskew) would be a way to allow implementations to avoid the TimeSync impairment due to skew between the PHY layers.

This is a lot to digest - I can present the reasoning here if leadership thinks it would be worthwhile.

Suggested Remedy

Consider requiring (or allowing as an option) a full deskew instead of the 20/40 bit deskew in clauses (176.5.1.3.1, 176.6.1.2.1, 176.7.1.2.1, 176.8.1.2.1).

Proposed Response

Response Status: O

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The SM-PMA adds a lot of latency due to the 2x RS-FEC CW delay in the 8:1 and 16:2 SM-PMAs, as compared to the bit-mux PMAs. For setups with a MII-Extender it is actually worse, since the penalty would also exist between the DTE_XS and PHY_XS. If latency is a concern, it actually becomes preferable to use 100Gbps links for the DTE_XS <-> PHY_XS AUI interface, negating the advantages of 200Gbps links!

The latency penalty for the 8:1 and 16:2 PMAs should be noted in Clauses 176.5.1.3.4 and 176.6.1.2.4.

Suggested Remedy

Add the following note to the 2xFEC CW delay sub-clauses (176.5.1.3.4 and 176.6.1.2.4): Note that the delay added to the odd PCSLs (and to the even PCSLs at the far-end) causes an end-to-end latency increase of 51.4ns as compared to BM-PMAs.

Proposed Response

Response Status: O

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Clauses 176.6, 176.7 and 176.8 are missing the 'overview' sub-clauses (with tables) that exist in Clause 176.5 (e.g. 176.5.1.1). The equivalent content is there but is placed directly in each PMA sub-clause (e.g. 176.6.1).

Suggested Remedy

Consider specifying the 1.8 and 8:1 (and equivalent SM-PMAs for other rates) together.

Proposed Response

Response Status: O
### Proposed Response

<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Inner FEC (Clause 177 or Clause 184) needs MDIO registers for TimeSync. They should look like the PMA/PMD clause registers.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Suggested Remedy</strong></td>
<td>Add the following MDIO registers for the Inner FEC, in the same style as the equivalent PMA/PMD MDIO registers.</td>
</tr>
<tr>
<td></td>
<td>- TimeSync capability</td>
</tr>
<tr>
<td></td>
<td>- TimeSync transmit path data delay register</td>
</tr>
<tr>
<td></td>
<td>- TimeSync receive path data delay register</td>
</tr>
</tbody>
</table>

**de Koos, Andras**

**Microchip Technology**

| Comment ID | 603 |
| Comment | **T** |
| Status | X |

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<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Phase of inner FEC pad bits vs outer FEC parity bits:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Suggested Remedy</strong></td>
<td>- An inaccuracy in the path data delay of up to 12ps due to arbitrary phase between the output FEC parity bits and the inner FEC pad bits of the phase is not accounted for.</td>
</tr>
<tr>
<td></td>
<td>- This arbitrary phase would affect the path data delay values.</td>
</tr>
<tr>
<td></td>
<td>- Almost negligible, if my math is correct.</td>
</tr>
</tbody>
</table>

**de Koos, Andras**

**Microchip Technology**

| Comment ID | 604 |
| Comment | **T** |
| Status | X |

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| Comment Type | Due primarily to the convolutional interleaver/deinterleaver, there is a large variation in the input-to-output latency of the Inner FEC sublayer. As such, there is concern that the method to properly calculate the path data delay for the Inner FEC sublayer should be explained in Clause 90, similarly to what is done for the variation from FEC codewords and PCS-lane distribution in clause 90.7.1. |
| **Suggested Remedy** | Do nothing. |
|               | Using the general method in Clause 90A, allocating the maximum value of the intrinsic delay to the transmit PHY and the minimum value of the intrinsic delay to the receive PHY, there is no ambiguity. |
|               | So it should not be necessary to add to Clause 90 for every new PHY type. The principles laid out in Annex 90A.7 should apply. |
|               | If anything, a general note could be added in Clause 177 (or in Clause 45 with the MDIO registers for path data delay values) explaining that the Tx/Rx path data delay values should be calculated following the guidelines in Annex 90A.7, where the maximum latency value is used for the Tx path data delay, and the minimum latency value is used for Rx path data delay. |

**de Koos, Andras**

**Microchip Technology**

| Comment ID | 605 |
| Comment | **T** |
| Status | O |

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| Comment Type | I'm not convinced that the circular shift really adds any robustness. Yes, it distances bit-pairs belonging to the same RS-FEC codeword, but… |
| **Suggested Remedy** | Without the shift, the consecutive bit pairs (after 8:1 multiplexing) belonging to the same RS-FEC code words would each protected by different Inner FEC code words, wouldn't they? |
|               | So is the circular shift just protecting against uncorrected inner-FEC codewords that would all land on the same RS-FEC codeword? Seems overkill. Are there simulations/models showing the benefit of including circular shift? |

**de Koos, Andras**

**Microchip Technology**

| Comment ID | 606 |
| Comment | **T** |
| Status | O |
**Comment ID** 607

**Comment Type** T

**Comment Status** X

**Proposed Response**

Was there not a proposal to make the circular shift optional, in order to minimize latency?

**Suggested Remedy**

Consider removing the circular shift if it does offer no worthwhile benefit.

---

**Comment ID** 608

**Comment Type** T

**Comment Status** X

**Proposed Response**

A figure illustrating the pad bits and their interval for each inner FEC flow would be useful. I always find myself referring to the equivalent RS-FEC Figures (Figure 119–6 and Figure 119–6).

**Suggested Remedy**

Consider adding a figure illustrating the pad insertion and interval, in the same style as Figure 119–6.

---

**Comment ID** 609

**Comment Type** T

**Comment Status** X

**Proposed Response**

A figure illustrating the possible one bit-pair of skew and the relationship to the Inner FEC flows would be very helpful here. I only understand because I recall the Task Force presentations!

**Suggested Remedy**

Consider adding a figure illustrating how the position of the 1 bit-pair of skew determines the Inner FEC flow number.

---

**Comment ID** 610

**Comment Type** T

**Comment Status** X

**Proposed Response**

The convolutional interleaver is composed of three parallel delay lines (numbered 0 to 2), as illustrated in Figure 177–3. Each delay operator "D" represents a storage element of 40 bits. From one delay line to the next higher delay line, Q delay operators are deleted. Modify the Q values to 192/96/48/24 for 200G/400G/800G/1.6TbE.

**Suggested Remedy**

Suggest to modify Line 50-51 in page 251 as follows:

The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay" is correct only if the Q values are 544/272/136/68 for 200G/400G/800G/1.6T. However, the Q values should be 192/96/48/24 as shown in slides 6-11 of he_3dj_01_2307 for 200G/400G/800G/1.6TbE.

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**Comment ID** 611

**Comment Type** T

**Comment Status** X

**Proposed Response**

The systematic Hamming code is most naturally defined in terms of its parity-check matrix, as pointed out in many textbooks and standard documents. One famous example is the systematic double-extended Hamming(128,119) code in OIF-400ZR and ITU-T G.709.3.

**Suggested Remedy**

Suggest to include the construction process and parity-check matrix of the adopted Hamming(68,60) code to enhance the completeness of the document. A Supporting Presentation will be provided.
The generation matrix \( G(60,8) \) for the Hamming(68,60) encoder is given in Table 177–1. It is not accurate. The generation matrix for the Hamming(68,60) should be with 60 rows and 68 columns, where the most-left 60 columns is the identity matrix.

**Suggested Remedy**

Suggest to change the sentence to: "The generator matrix of the Hamming(68,60) code is \( G = [I_{60} ; G_{(60\times8)}] \), where \( I_{60} \) is the 60×60 identity matrix, and \( G_{(60\times8)} \) is a 60×8 matrix used to generate the 8 parity bits given in Table 177–1."

**Proposed Response**

Response Status: O

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For \( \text{permo}[p, 40x(i-18 \ mod \ 3)+j] \), the column index \( 40x(i-18 \ mod \ 3)+j \) may be a negative value.

**Suggested Remedy**

Suggest to add one sentence after Line 9: When \( 40x(i-18 \ mod \ 3)+j \) is negative, \( \text{permo}[p, 40x(i-18 \ mod \ 3)+j] \) will be undetermined value from initial buffer of the convolutional interleaver.

**Proposed Response**

Response Status: O