212 Gb/s PAM4 per Lane C2M Channels A Via Length Performance Study Supplement **Rick Rabinovich** January 17, 2023



Supporter

• Ali Ghiasi



200G PAM4 C2M Via Length Effect Study Supplement Objectives

- Follow up to presentation given on September 21st, 2022
- Study the effect of via length in channel performance
 - ✓ Via lengths = 19/67/93/135 mil
- Evaluated channel performance using COM rev. 3.9 and corresponding new spreadsheets.
- Investigate the effect of Raised Cosine vs. Butterworth filter performance
- Illustrate the paradox when cascading s-parameters of vias and connector models

The intention of this presentation is NOT to:

- ✓ Discuss specific materials
- ✓ Discuss specific equalizations/implementations
- ✓ Discuss specific ASIC footprints
- ✓ Recommend specific receive filters

The intention of this presentation is to:

- Contribute two additional "optimized" channels based on "actual" channel implementations which includes the ASIC breakout, routing, via transitions, and the latest OSFP model available
 - > Via antipads in PCB inner layers were optimized using HFSS Optimetrix
- Provide channels with <u>impairments</u> that seasoned design engineers will encounter when implementing channels operating at 224 Gb/s per lane.
- ✓ Analyze receiver equalization solutions to pass COM rev. 3.9

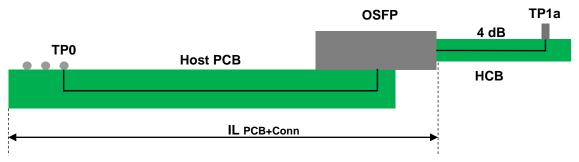


C2M Channel Highlights

- Traditional Topology, i.e., medium PCB material between ASIC and Connector
 - Short Channel Ex. NIC card
- Short Host Channel
 - Well engineered challenging channel
 - Includes Huray model for copper roughness
- Channel with IMPAIRMENTS
 - ASIC/Connector vias and module finger transition
 - Layout trace turns
 - Skew compensation
 - Full channel crosstalk
- MDI is an OSFP connector model
- Crosstalk source mostly at the connector and footprint
- HCB Ideal transmission line with IL=4.0 dB @ Nyquist
- COM rev. 3.9 Includes raise cosine option



Structure View & Insertion Losses



- Full Structure:
 - Two adjacent channels
 - > Matching segmentation meshing (i.e., common minimum element size)
 - Connector integrated with PCB
 - HCB is ideal transmission line with IL = 4 dB @ Nyquist
 - NEXT is evaluated at the ASIC model for more realistic results
- Vias = 19/67/93/135 mil long
- Blind Vias
- Frequency Sweep Range = 10 MHz to 120 GHz

IL @ Nyquist (53.125 GHz)

Name Х 53.1250 -14.6966 m1 m2 52.3700 -13.8375 **Reflections Effect**

Parallel Breakout

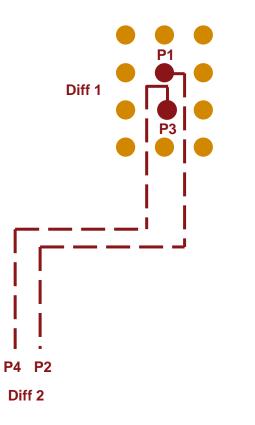
Orthogonal Breakout

- |L PCB+Conn = 8.24/9.32/10.31/8.92 dB٠
- IL HCB $= 4 \, \mathrm{dB}$ ٠
- IL TP0-to-TP1a = 12.27/13.32/13.44/12.93 dB
- IL PCB+Conn = 8.34/10.69/10.14/9.33 dB
- IL HCB $= 4 \, \mathrm{dB}$ •
- IL TP0-to-TP1a = 12.38/14.69/14.17/13.36 dB ٠

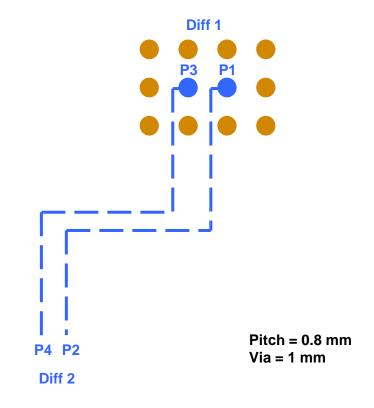


Two ASIC breakouts: Orthogonal vs. Parallel

Orthogonal Breakout

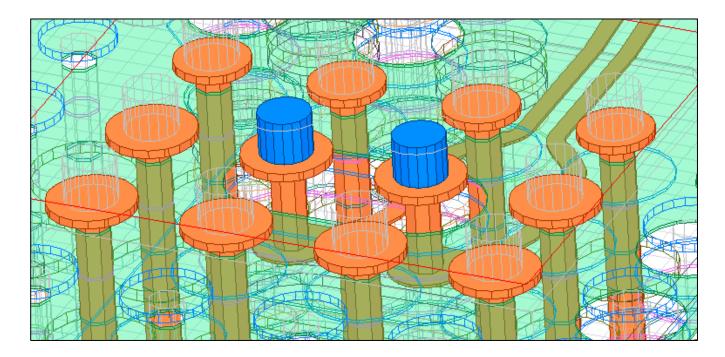








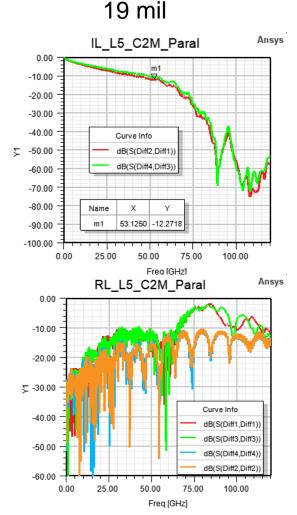
200G PAM4 C2M Via Length Effect Study Supplement ASIC Ball Model Example

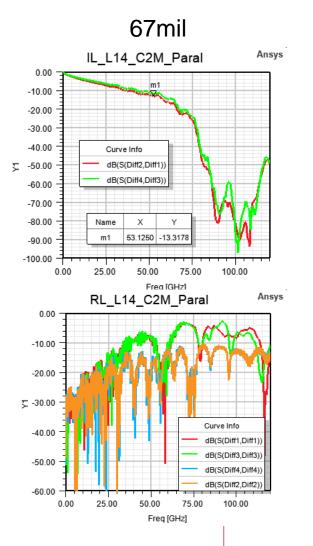


Cp already included in model => Cp=0



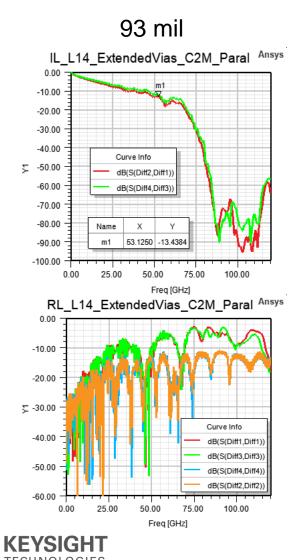
Parallel Breakout - IL/RL Performance

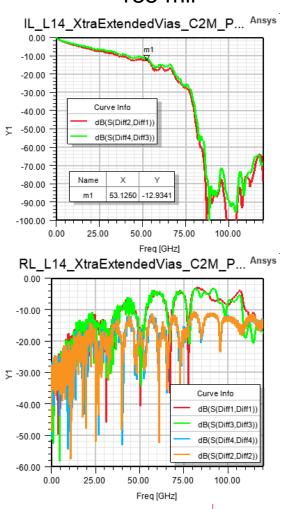






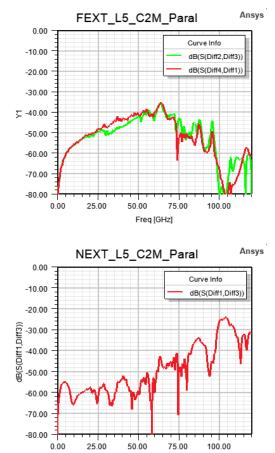
Parallel Breakout - IL/RL Performance



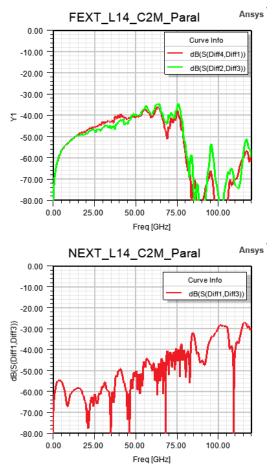


Parallel Breakout - FEXT/NEXT(ASIC) Performance

19 mil



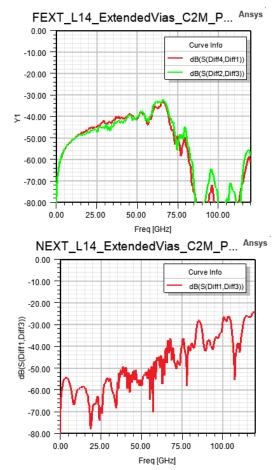
Freq [GHz]

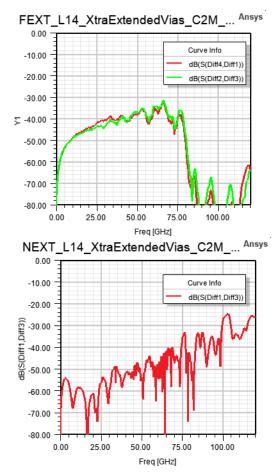




Parallel Breakout - FEXT/NEXT(ASIC) Performance

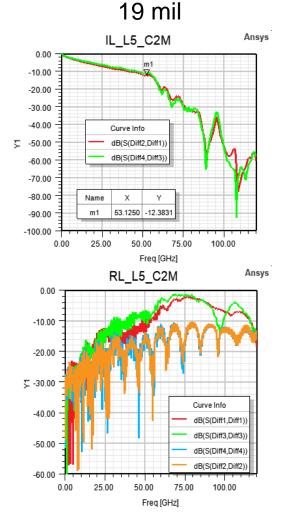
93 mil

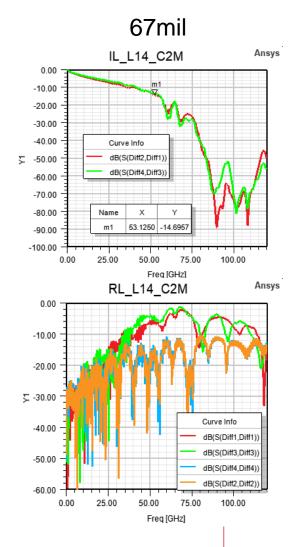






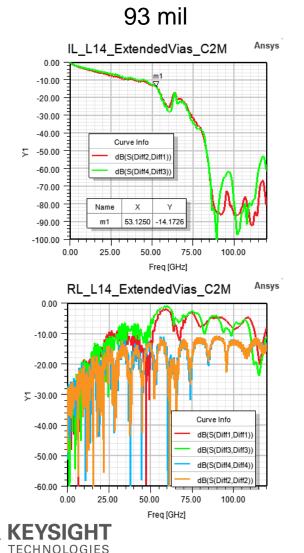
Orthogonal Breakout - IL/RL Performance







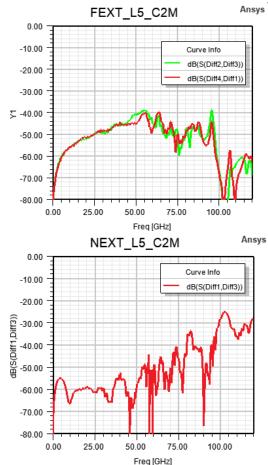
Orthogonal Breakout - IL/RL Performance



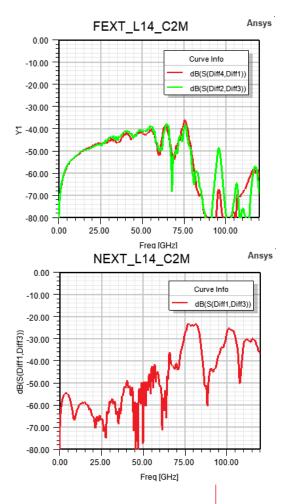
135 mil IL L14 XtraExtendedVias C2M Ansys 0.00 m1 -10.00 -20.00 -30.00 -40.00 Curve Info 71 -50.00 dB(S(Diff2,Diff1)) -60.00 dB(S(Diff4,Diff3)) -70.00 -80.00 Name х γ 53.1250 -13.3523 -90.00 m1 -100.00 50.00 0.00 100.00 Freg [GHz] RL_L14_XtraExtendedVias_C2M Ansys 0.00 -10.00 -20.00 5 -30.00 Curve Info -40.00 dB(S(Diff1,Diff1)) dB(S(Diff3.Diff3) dB(S(Diff4,Diff4) -50.00 dB(S(Diff2,Diff2) -60.00 75.00 0.00 25.00 50.00 100.00 Freg [GHz]

Orthogonal Breakout – FEXT/NEXT(ASIC) Performance

19 mil

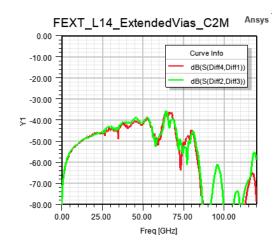


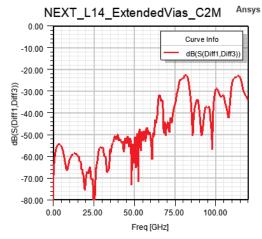


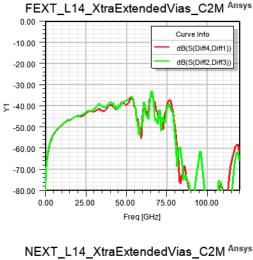


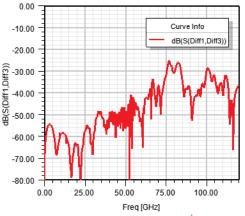
200G PAM4 C2M Via Length Effect Study Supplement Orthogonal Breakout – FEXT/NEXT(ASIC) Performance

93 mil











Structures and COM Configurations

- Four Via Lengths:
 - ✓ 19 mil 67 mil 93 mil 135 mil
- Two Breakouts:
 - ✓ Parallel
 - ✓ Orthogonal
- Medium Package Size = 30 mm
- Two Filters:
 - ✓ Butterworth
 - ✓ Raised Cosine (starts @ 67 GHz, ends @ 79.7 GHz)*
- With PKG_Tx_FFE_Preset*
- Floating Taps:
 - ✓ 6 groups/3 taps per group/120 UI span
- DER = 1e-05 and 5e-5

* Note: Default values in contributed spreadsheets



COM Results

			2 FEXTs - 1 N	IEXT - Medi	um Size Pa	ckage (30 r	nm)				
				Orthogon	al Breakou	t					
Case #	Via Length	PKG_TX_FFE_Preset	Filter	DER_0	SNR_TX	eta_0	Float. Taps	EH (mV)	VEC (dB)	ERL (dB)	ICN
1	19 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	10.3	8.63	17.6	1.47
2	67 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	8.7	9.88	16.6	2.04
3	93 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	6.7	11.21	15.5	2.27
4	135 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	4.5	13.85	15.5	2.83
5	135 mil	Yes	Rcin+ BW	5.00E-05	32.5	4.10E-09	Yes	6.2	11.14	16.1	2.83
			2 FEXTs - 1 N	IEXT - Medi	um Size Pa	ickage (30 r	nm)				
				Paralell	Breakout						
Case #	Via Length	PKG_TX_FFE_Preset	Filter	DER_0	SNR_TX	eta_0	Float. Taps	EH (mV)	VEC (dB)	ERL (dB)	ICN
1	19 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	9.5	8.79	17.6	1.79
2	67 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	7.9	10.28	16.6	2.36
3	93 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	6.9	11.15	15.4	2.62
4	135 mil	Yes	Rcin+ BW	1.00E-05	32.5	4.10E-09	Yes	5.6	13.36	15.5	3.25
5	135 mil	Yes	Rcin+ BW	5.00E-05	32.5	4.10E-09	Yes	7.5	10.80	16.1	3.25

* Pass: VECmax = 12 ; ERLmin = 10



COM Results Highlights

Longer vias require additional equalization features regardless of the ASIC breakout style:

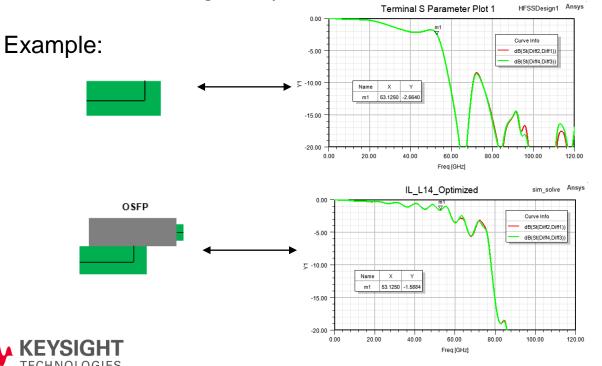
- Stronger filter in addition to traditional Butterworth
 > Raised Cosine or equivalent
- Reduce receiver intrinsic noise
- Higher SNR
- Stronger FEC (segmented?) to account for higher DER
- Floating DFE taps or equivalent



Modeling Paradox – Via + Connector ≠ Via and Connector

Cascading s-parameters from different sources has risks:

- Actual x-talk is lost by interconnecting non-TEM boundaries.
- Cascading s-parameters from different sources
 - Missing interconnect structure pieces and phase information
 - ✓ Double counting of transitions and creating phase distortion
- Unaccounted meshing mismatch
- > Build channel model with a "holistic" approach
 - ✤ Channel model should <u>NOT</u> be just an aggregate of s-parameter structures
 - Channel should be segmented with wave ports along uniform transmission lines several wavelengths away from discontinuities.



Summary

"Equal Distribution of PAIN" to make C2M a viable interface

Longer PCB via solutions are feasible but:

- 1. Need to optimize via transitions
 - Cancel via capacitive and inductive effects
 - Optimize connector to module PCB transition
- 2. Stronger FEC to support higher DER
 - Segmented FEC (?)
- 3. Enhanced Receiver Equalization (compared to P802.3ck):
 - Stronger filter
 - Higher SNR
 - Include floating taps option or equivalent
 - Reduce intrinsic chip noise
- Channel Modeling: Take a holistic approach



Q & A



Additional Data



200G PAM4 C2M Via Length Effect Study Supplement Working Spreadsheet

Table 93A-1 parameters						I/O control		Table 93A–3 parameters			
	Parameter	Setting	Units	Information	DIAGNOSTICS	1	logical	Parameter	Setting	Units	
	f_b	106.25	GBd		DISPLAY_WINDOW	1	logical	package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]		
	f_min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	0.00644805	ns/mm	
	Delta_f	0.01	GHz		RESULT_DIR	.\results\c2m_{date}\		package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
	C_d	[0.4e-4 0.9e-4 1.1e-4;000]	nF	[TX RX]	SAVE_FIGURES	0	logical				
	Ls	[.12.15.14;000]	nH	[TX RX]	Port Order	[1234]		Parameter	Setting		
	C_b	[.3e-4 0]	nF	[TX RX]	RUNTAG	1_Rcos_Txpe_TP1a_COM_m	odel	board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G	
	z_p select	[123]		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm	
	z_p (TX)	[12 30 45; 1 1 1 ; 0.1 0.1 0.1 ; 0.58 0.58 0.58]	mm	[test cases]	Oper	ational		board_Z_c	100	Ohm	
	z_p (NEXT)	[000;000;000;000]	mm	[test cases]	ERL Pass threshold	10	dB	z_bp(TX)	125	mm	
	z_p (FEXT)	[12 30 45; 1 1 1 ; 0.1 0.1 0.1 ; 0.58 0.58 0.58]	mm	[test cases]	VEC Pass threshold	12	db	z_bp (NEXT)	0	mm	
	z_p (RX)	[000;000;000;000]	mm	[test cases]	EH_min	0	Value	z_bp (FEXT)	125	mm	
	PKG_Tx_FFE_preset	[-0.140 1; -0.182 1; -0.231 1]			DER_0	5.00E-05		z_bp(RX)	0	mm	
	C_p	0	nF	[TX RX]	T	4.71E-03	ns	C_0	[0.2e-4 0]	nF	
	R_O	50	Ohm		FORCE_TR	1	logical	C_1	[0.2e-40]	nF	
	R_d	[45 50]	Ohm	[TX RX]	Min_VEO_Test	0	Wm	Include PCB	0	logical	
	A_v	0.387	v	vp/vf=	PMD_type	C2M					
	A_fe	0.387	v	vp/vf=	T_0	50	mUI				
	A ne	0.608	v		samples_for_C2M	100	amples/UI	Seletions (r	ectangle, gaussian, dual_rayleigh, trian	gle	
	L	4			EW	1		Histogram_Window_Weight	gaussian	selection	
	м	32			TDR	and ERL options		Qr	0.02	UI	
		filter and Eq			TDR	1	logical				
	f.r	0.75	*fb		ERL	1	logical				
	c(0)	0.65		min	ERL_ONLY	0	logical		ICN parameters		
	c(-1)	[-0.2:0.02:0]		[min:step:max]	TR_TDR	0.01	ns	f_v	0.278	Fb	
	c(-2)	[0:.02:0.1]		[min:step:max]	N	1000		ff	0.278	Fb	
	c(-3)	[-0.1:.02:0]		[min:step:max]	TDR_Butterworth	1	logical	f_n	0.278	Fb	
	c(1)	[-0.2:0.02:0]		[min:step:max]	beta_x	0		f 2	79.688	GHz	
	Nb	8	UI		rho_x	0.618		A ft	0.450	v	
	b_max(1)	0.85		As/dffe1	TDR_W_TXPKG	1		Ant	0.450	V	
	b max(2N b)	0.15		As/dfe2N b	N bx	8	UI	_			
	b_min(1)	0		As/dffe1	fixture delay time	[0 0.2e-9]			Floating Tap Control		
	b min(2N b)	-0.15		As/dfe2N b	Tukey Window	1		N bg	6	012 or 3 groups	
-	g DC	[-13:1:0]	dB	[min:step:max]		Noise, jitter		N bf	3	taps per group	
	f.z	42.5	GHz		sigma_RJ	0.01	UI	N f	120	UI span for floating taps	
	f p1	42.5	GHz		A DD	0.02	UI	bmaxg	0.2	max DFE value for floating t	
	f_p2	106.25	GHz		eta_0	4.10E-09	V^2/GHz	B float RSS MAX	0.1	rss tail tap limit	
	g DC HP	[-6:1:0]		[min:step:max]	SNR TX	32.5	dB	N tail start	9	(UI) start of tail taps limit	
	f HP PZ	1.0625	GHz		R LM	0.95					
	Butterworth	1	logical	include in fr	11-2022 BenArtsi pkg	5.55			Receiver testing		
	Raised_Cosine	1	logical	include in fr	highlighted are under re-c	onsideration		RX CALIBRATION	0	logical	
	RC_Start	6.70E+10	Hz	start freg for RCos	mli_3df_02_220316			Sigma BBN step	5.00E-03	V	
	RC end	7.97E+10	Hz	end freg for RCos	1111_001_02_220516			orgina boli step	5.00505	Y	
	No_end	7.572+10	114	end neg for neos							
_	den en e	0.0004									
	ulse response truncation threshold	0.0001									



Channel Contributions*

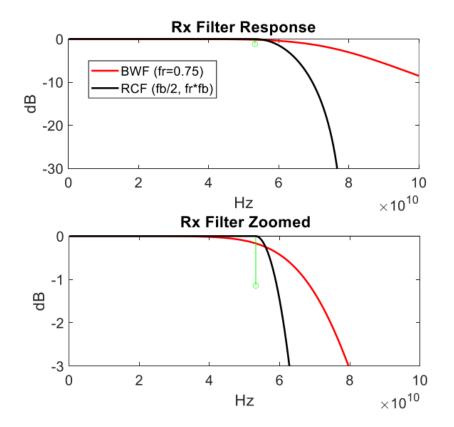
- Rabinovich_C2M_200G_Paral_19mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Paral_19mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Paral_19mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Paral_67mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Paral_67mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Paral_67mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Paral_93mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Paral_93mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Paral_93mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Paral_135mil_011723_FEXT.s4p
- Rabinovich_C2M_200G_Paral_135mil_011723 _NEXT.s4p
- Rabinovich_C2M_200G_Paral_135mil_011723 _Thru.s4p
- Rabinovich_C2M_200G_Ortho_19mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Ortho_19mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Ortho_19mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Ortho_67mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Ortho_67mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Ortho_67mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Ortho_93mil_092122_FEXT.s4p**
- Rabinovich_C2M_200G_Ortho_93mil_092122_NEXT.s4p**
- Rabinovich_C2M_200G_Ortho_93mil_092122_Thru.s4p**
- Rabinovich_C2M_200G_Ortho_135mil_011723 _FEXT.s4p
- Rabinovich_C2M_200G_Ortho_135mil_011723_NEXT.s4p
- Rabinovich_C2M_200G_Ortho_135mil_011723 _Thru.s4p

* Note: Use Port Order = [1 2 3 4]

** Note: Released on 9/21/22



IL Comparison Between Butterworth and Raise Cosine Filters



* Source: Mellitz_3df_elec_01_220621.pdf

