Concatenated FEC Proposal for 200 Gbps per Lane IMDD Optical PMD

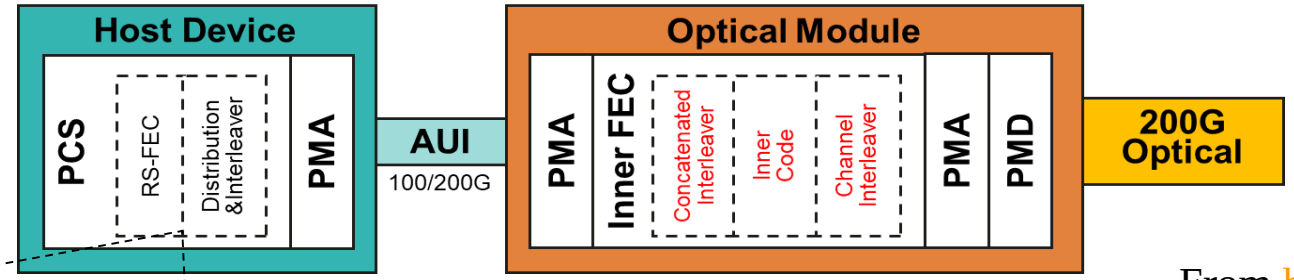
Masoud Barakatain, Kechao Huang, Xiaoling Yang, Qinhui Huang, Zengchao Yan, Huixiao Ma, and Chuandong Li

Huawei Technologies

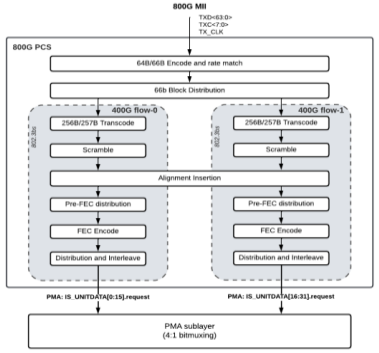
Presentation Goal

- Promote the idea presented in huang_3df_01a_2211
  - It is instrumental for the inner-code dimension to be a multiple of 10b
  - Recommend the use of SFEC(128,120) inner code where Hamming encore is applied to XOR of message PAM4 bits
  - Propose adding *alignment insertion* or *padding* to obtain a baud rate that is an integer multiple of 156.25 MHz reference Xtal frequency
  - Left open any potential use-case for the padding bits
- Present potential use cases for the padding bits
  - Option 1: Generate extra coding gain out of the added overhead, using the same inner SFEC(128,120) engine
  - **Option 2: Reserve the added overhead for future use as a backchannel for optical transceivers**

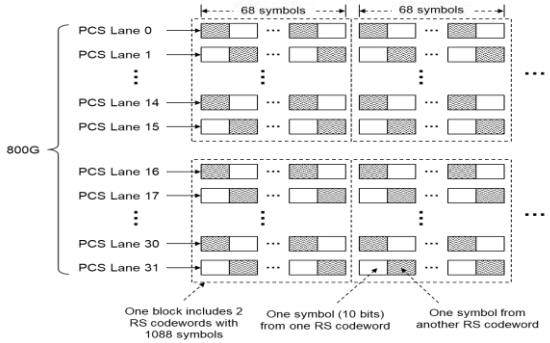
Background (1/2)



From huang_3df_01a_2211



From shrikhande_3df_01b_2207



Details on the PCS bit streams

- Several SFEC inner codes for concatenation with KP4 outer code have been proposed for 200Gb/s per Lane IMDD Optical PMD.
- bliss_3df_01b_202211 proposed to adopt inner code with rate 17/18
  - Effective codeword length n=144, and message length k=136.
  - Baud rate 112.5GBd in keeping with the existing Xtal reference.
  - Concern: message length, k, is not a multiple of 10b, the RS symbol length.

Inner Code Rates: 15/16, 17/18, or 17/19

- 5.88% overhead from rate 17/18 code choice is advantageous
  - Avoids further line bit rate increases and their associated losses and costs
  - Keeps the simple historic Xtal references

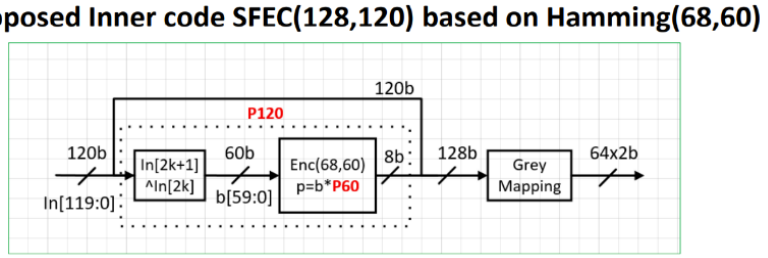
Code Option	Inner code	Code Rate	Codeword effective n *bits*	Message effective k *bits*	Baud Rate (GBd)	Bit Rate (Gb/s)	Multiple of 156.25MHz	BER_in for KP4 threshold*
A	Extended Hamming (128,120)	15/16	128	120	113.333 …	226.666 …	~725.333 …	5.5e-3
B	BCH(144,136)	17/18	144	136	112.5	225	720	5.0e-3
C	Shortened BCH(76,68) from BCH(144,136)	17/19	76	68	118.75	237.5	760	8.2e-3
D	Extended Hamming (128,120) shortened to (76,68) with XOR of message PAM-4 bits	17/18	144	136	112.5	225	720	5.0e-3

*Simulated with maximum likelihood decoding
*Line bit error rate input to Soft Hamming Decoder to achieve <3.2e-4 before and <1e-13 after KP4 decoding for AWGN w/ sufficient interleaving 5/16

From bliss_3df_01b_202211

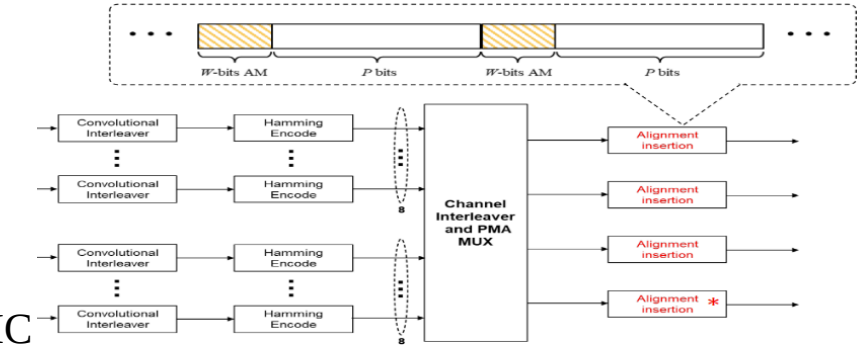
Background (2/2)

- farhood_3df_02b_2211 proposed to adopt SFEC(128,120) inner code
  - Effective codeword length n=128, and message length k=120.
  - Message length, 120 bits, is a multiple of 10b enabling simple interleaver design
  - Concern: baud rate is not an integer multiple of the 156.25MHz Xtal reference



From farhood_3df_02b_2211

- huang_3df_01a_2211 proposed to add a small overhead as "alignment insertion" after the SFEC(128,120) inner code encoding
  - to achieve a baud rate that is an integer multiple of the 156.25MHz Xtal reference
  - Concern: in future co-packaged optics (CPO) or near package optics (NPO) implementations, it may be unwarranted to have two alignment insertions in host ASIC

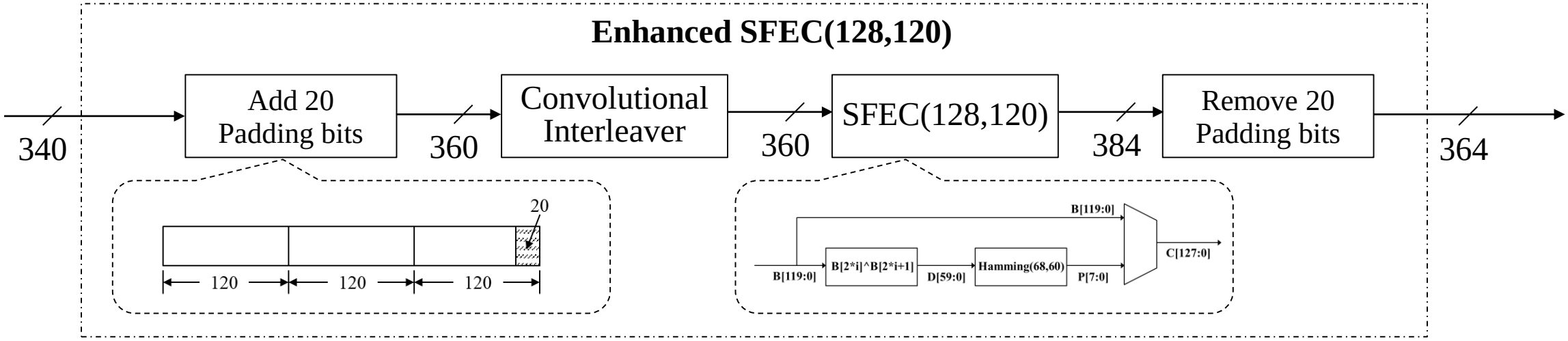


From huang_3df_01a_2211

- **But what do we do with the added overhead?** In this contribution, two solutions are presented
  - Option 1: An enhanced inner FEC solution based on the SFEC(128,120) proposed in farhood_3df_02b_2211
  - Option 2: To leave it as is for now, to be used as reserved channel (RES) for optical transceivers in later iterations

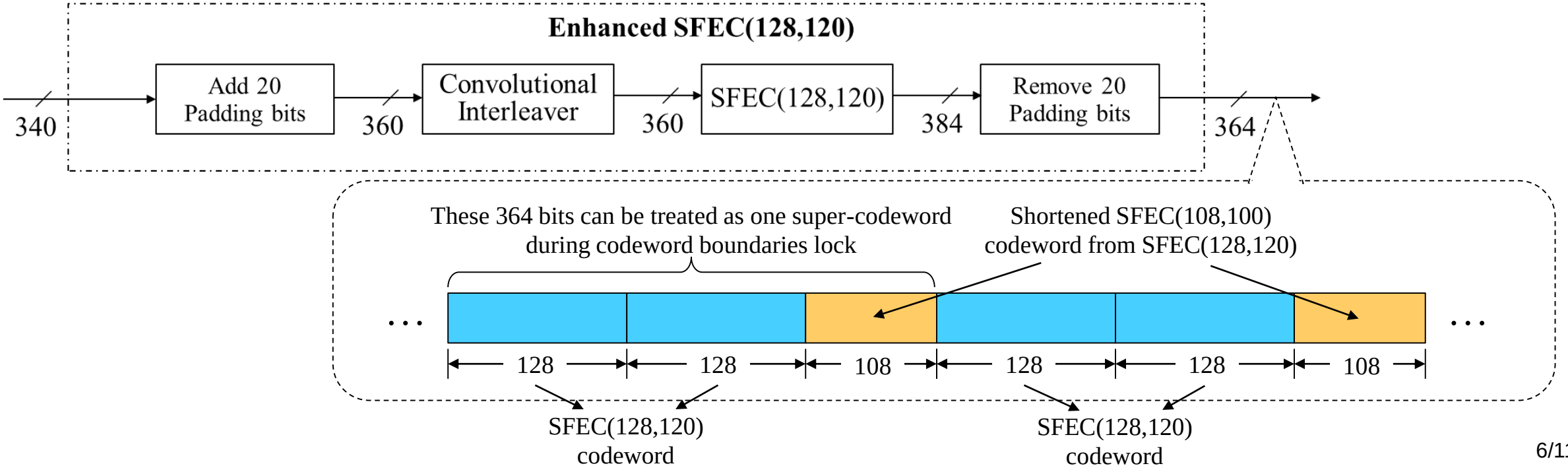
Option 1: Enhanced SFEC(128,120) Inner Code

- Main idea is to obtain a coding gain over the conventional SFEC(128,120) using the added overhead:
  - Add p padding bits (all zero) before encoding, and remove them after the encoding, effectively resulting in a shortened code
  - The resulting FEC rate is lower: $(k-p)/(n-p)$ vs. k/n at the FEC(n,k)
- Proposed enhanced SFEC(128,120) inner code:
  - Constructed based on the SFEC(128,120), which is Hamming (128,120) shortened to (68,60) with XOR of message PAM4 bits
  - For each 340-bit group (the effective message length, equivalent to 3 conventional FEC words), 20 Padding bits (all zero) are added
  - The 360-bit group is processed by the convolutional interleaver, resulting in a 360-bit interleaved group
  - The 360-bit interleaved group is encoded by SFEC(128,120) engine used 3 times, resulting in a 384-bit encoded group
  - The 20 Padding bits within the 384-bit encoded group are removed, resulting in a 364-bit group as the effective codeword



Option 1: Enhanced SFEC Synchronization Process

- In the receiver module, the synchronization process can use the Hamming syndrome calculator to identify the location of inner code boundaries
  - If there are ***T*** or more zero-syndrome received codewords in a window of ***W*** codewords, it is considered that the inner code boundary is locked, which also implies that the convolutional interleaver is correctly locked.
  - See similar synchronization method in IEEE 802.3 Clause 74.7.4.7 for reference.
  - The synchronization process still works well for the case where 'Hamming codeword interleaver' is used after the enhanced SFEC(128,120) encoding.

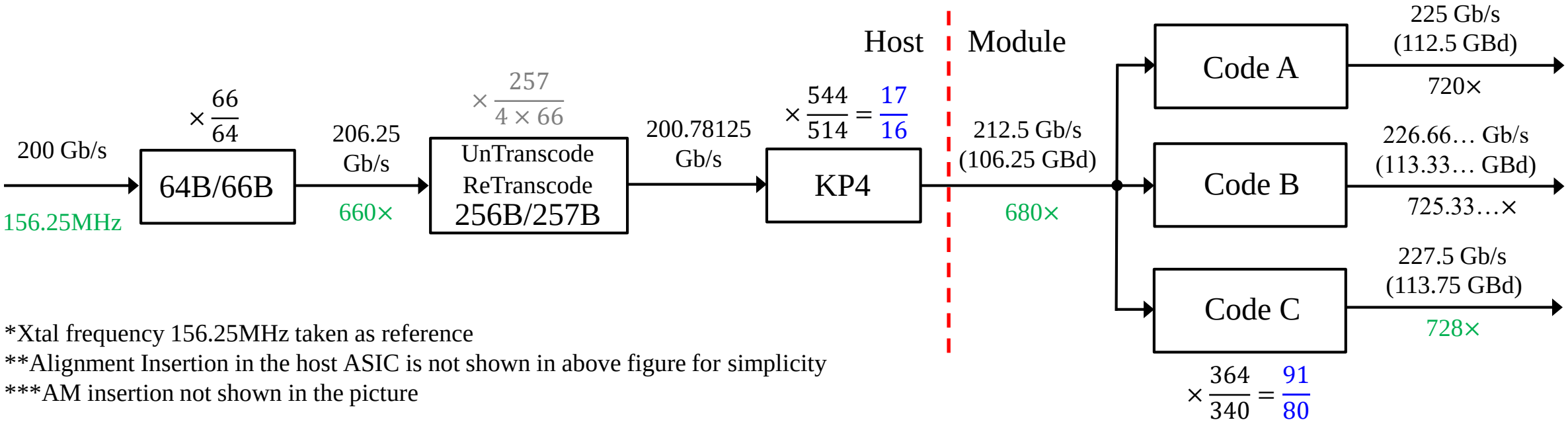


Option 1: Comparison of Inner Codes

Code Option	Inner code	Inner Code Rate	Baud Rate (GBd)	Baud Rate Divided by 156.25MHz	Pre-FEC BER ($\times 10^{-3}$)	Interleaver Latency	Remarks
A	Hamming (144,136) Or (76,68) shortened version with XOR of message PAM4 bits	17/18	112.5	720	4.5 - 4.55	~75ns	Needs extra logic to work with the convolutional interleaver
B	Hamming (128,120) Or (68,60) shortened version with XOR of message PAM4 bits	15/16	113.33…	725.33…	4.8 - 4.85	~55ns	No need for deskew, enable low latency implementation
C	Proposed Enhanced SFEC(128,120)	85/91	113.75	728	5.2	~55ns	Low-latency implementation, similar to Code B

*Table developed based on the table in page 5 of bliss_3df_01b_202211. Hamming(76,68) code is not included in this table due to its high baud rate 118.75GBd.
**Practical soft-decision Chase decoding is used for the inner codes.
***The processing latency for deskew operation is typically about 14ns, see maniloff_3df_01b_2207.

Option 1: Comparison of Inner Codes



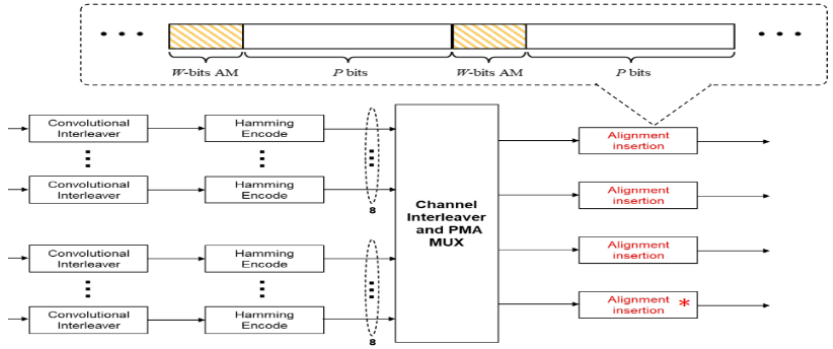
*Xtal frequency 156.25MHz taken as reference
**Alignment Insertion in the host ASIC is not shown in above figure for simplicity
***AM insertion not shown in the picture

- The proposed inner code, enhanced SFEC(128,120), has many advantages:
  - The effective message length (340 bits) is a multiple of 10b, enabling simple convolutional interleaver design.
  - The baud rate is 113.75GBd (728×156.25M or 364×312.5M), compatible with the existing Xtal references (156.25M and 312.5M).
  - The FEC performance is better with pre-FEC BER ~5.2E-3 using practical soft-decision Chase decoding for the inner code, while keeping the interleaver latency low at ~55ns.
  - Simple self-codeword synchronization process can be used to lock the inner code boundaries, which also implies the convolutional interleaver has locked.

Option 2: Reserved Channel

- huang_3df_01a_2211 left the “alignment insertion” unused.
- The added overhead can be reserved for vendor use, a first in IEEE standards.
- Note that we can tune the frequency of the insertions to obtain the desired number of bits per RES use.

- Characteristics and potential benefits of the RES:
  - Insertion happens before the channel interleaver and should be removed accordingly
  - The RES payload shall be DC-balanced
  - Left to be specified by the vendor
  - Some example use cases: compensation of slow changes, temperature, process, channel estimation, OSNR measurement, E2E delay measurement, etc.
  - May be simpler to implement compared to the proposed enhanced SFEC
  - Keeps the Hamming message length a multiple of 10b, resulting in enabling simple convolutional interleaver design
  - Makes the baud rate an integer multiple of the 156.25MHz Xtal frequency
- We leave the definition and protocols of the RES to future meetings.



From huang_3df_01a_2211

Proposal

- Adopt the proposal to use the rate-15/16 SFEC engine in the optical module and to allocate the additional overhead to the RES channel
  - The Hamming message length remains a multiple of 10b, enabling simple convolutional interleaver design.
  - The baud rate becomes 113.75GBd compatible with the existing Xtal references (728×156.25M or 364×312.5M).
  - Many additional benefits for future use of the allocated RES channel.
- To discuss and make decisions on the details of the RES channel in the future meetings.

Thank you