Observation of Inner Code for 200 Gb/s per Lambda IM-DD Optical PMD

Xinyuan Wang, Xiang He, Matt Brown

Huawei Technologies

Background: Adopted Logic Architecture Baseline

- Logic architecture baseline and FEC scheme for 200 Gb/s per lane were adopted.

- Concatenated code based on RS(544,514) as the outer code, soft decision BCH/Hamming as the inner code is under discussion.

  - Coordinated PCS and PMA design is needed.

gustlin_3df_01a_220517.pdf
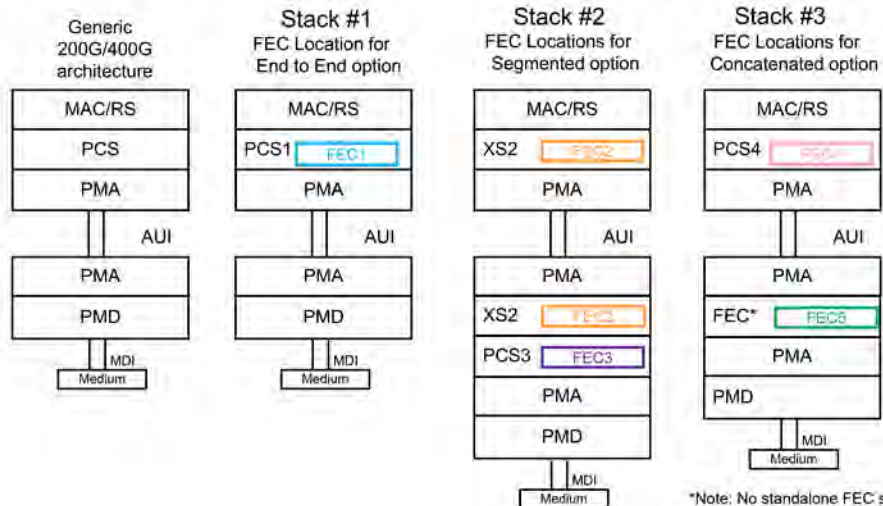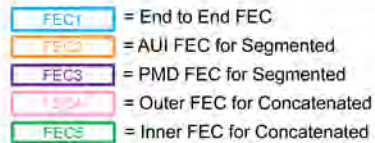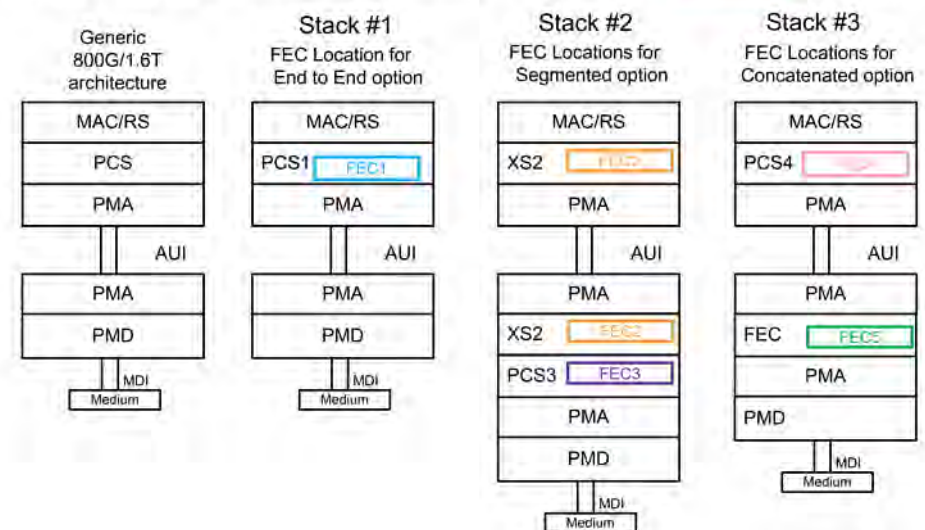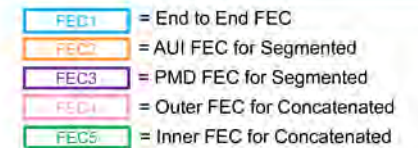
Concatenated Scheme for 200 Gb/s per Lambda

▫ Key aspects of inner code to be considered for PCS/PMA solution in P802.3dj:

RS(544,514)   **BCH(144,136)**
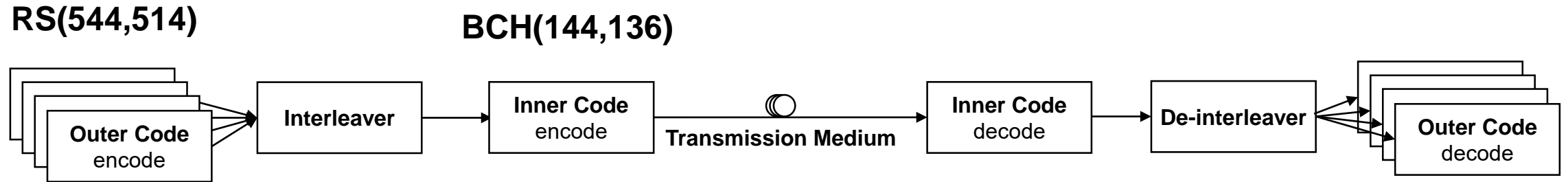
➤ #1: Inner code rate, performance, latency, power, as in bliss_3df_01b_2211, he_b400g_01_210426.

➤ #2: Breakout support is preferred.

➤ #3: Protocol agnostic optical module?

➤ #4: Interleaver depth between outer and inner code, as in bliss_3df_01a_220517.

➤ #4: Channel interleaver for optical PMDs, as in bliss_3df_01a_220517.

➤ #5: FEC frame synchronization.

Revisit: Breakout Support as in 802.3bs

- In [dambrosia_400_01a_1113](#), support of breakout is suggested.

Conclusions

- The market is adopting this "breakout functionality" with 10GbE / 40GbE
  - Breakout functionality – the ability to use a port in a lower rate / higher density mode of operation
- Providing an upgrade path forward could further improve this scenario for lower speeds
- "Breakout functionality" will enhance broad market potential of 400GbE by enabling adoption to support higher density / lower rate lower speeds to enable lower 400GbE cost.
- Proposed objective–
  - Provide appropriate support for breakout functionality

IEEE 802.3 400 Gb/s Ethernet Study Group
IEEE 802 Nov 2013 Plenary, Dallas, TX, USA.

13

Revisit: Logic Architecture to Support Breakout

□ Even breakout is not an objective in 802.3bs for 200/400GbE, it was **ENABLED** by the PCS(FEC)/PMA architecture as multi-instance sub-PMA function blocks, e.g., 8:4 implemented as $4 \times$ 2:1 in oDSP.

   ➢ **Bonded**: all PMD lanes running together to support a single MAC/PHY at a higher rate, e.g. 1×400 GbE.

   ➢ **Isolated**: breakout mode, single or multi lanes of PMA/PMD carries a single flow of lower rate MAC/PHY, e.g. 4×100 GbE.

As is (802.3bs)

MAC
RS
MII
PCS(FEC)
PMA — PMA
PMD — PMD
Optical Module

To be (P802.3dj)

MAC
RS
xMII
PCS(Outer code)/PMA
Inner code — Inner code
PMA — PMA
PMD — PMD
Optical Module
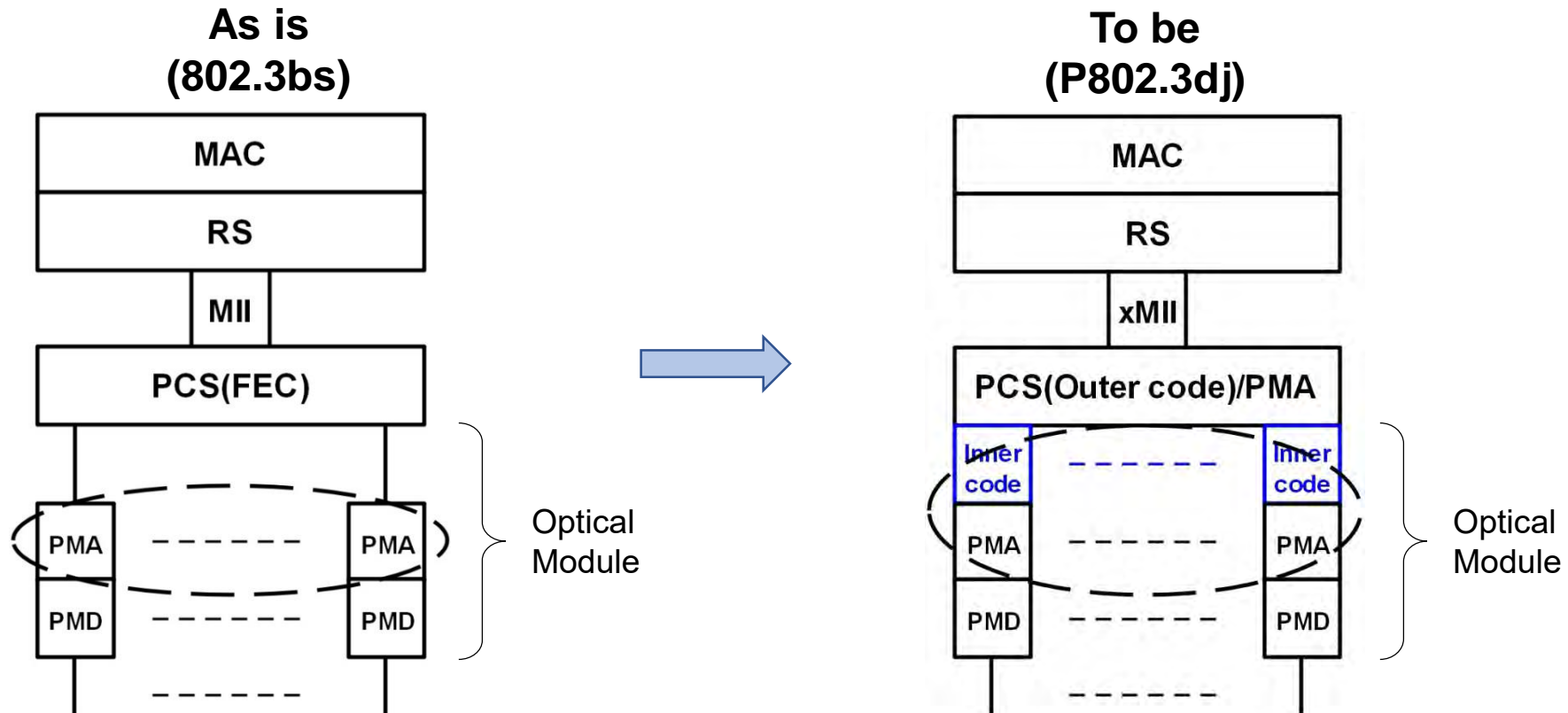
Revisit: PMA Muxing for Protocol Agnostic Optical Module

❑ During 802.3ba development, protocol agnostic optical module was enabled by MLD and bit muxing, with the following benefits:

➢ Optical modules work at "**Layer 0**" without awareness of complex data pattern (protocol) carried on each AUI and PMD lane, simplifying validation and test during manufacture to lower cost.

➢ Friendly to be reused in OTN etc, sharing the overall Ethernet eco-system to lower cost with broader applications.

❑ In 802.3bs, RS(544,514) was adopted for all of PMDs as the first step.

➢ Bit muxing was adopted for the PMA to enable protocol agnostic modules, with the support of **any logical lane to any physical lane**.

➢ The FEC performance degradation due to bit muxing was compensated by 2-way codeword interleaving.

❑ Is it still feasible to support protocol agnostic optical modules in P802.3dj?

➢ More investigation is needed.

➢ Module should less aware protocol, as simple as possible.

#1: Inner Code: BCH/Hamming(144,136)

- Inner code rate 17/18 to enable integer PLL.

  - Keeps the simple historic Xtal references, **clear** rate number at $720 \times 156.25M = 112.5\ GBd$.

  - No dummy/padding bits, the corresponding gearbox lead additional latency/power/cost.

  - **Avoids** further line bit rate increases and their associated losses and costs.
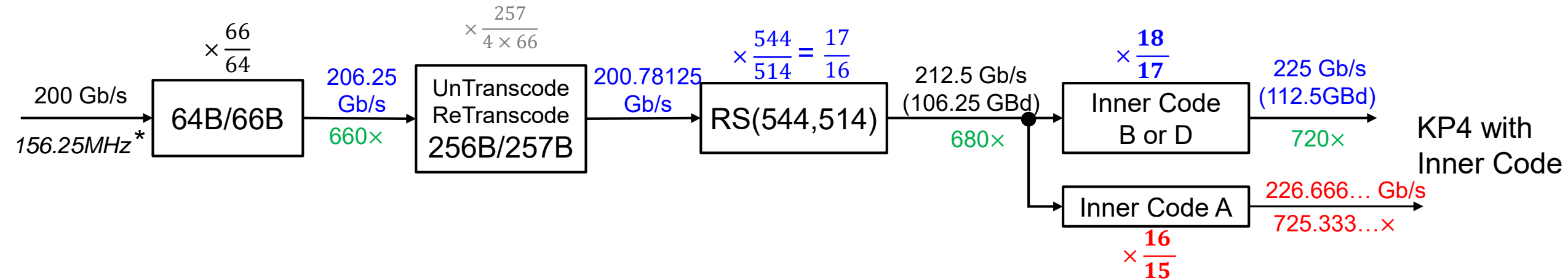
- Hamming(128,120) results fractional PLL.

- 1% higher overhead of Hamming(128,120) w/ padding will cause performance degradation due to limited bandwidth, brings a negative impact on overall coding gain, as in he_3dj_01_230206.

#2: Breakout with Inner Code Working at Per Lambda

❑ Each 200 Gb/s per lambda related PMA/PMD in optical module has its own inner code encoder, decoder, interleaver, etc. (That is, PMD per lambda dependent only, not PHY dependent.)
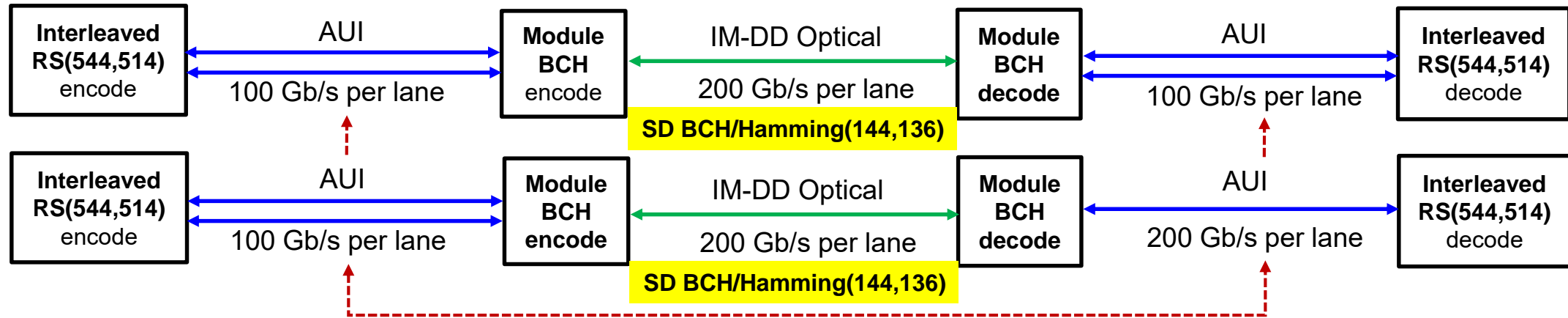
  ➢ PMA/PMD based inner code naturally supports **BREAKOUT** as no data interaction/redistribution between lanes.

  ➢ PCS lane based inner code relies on PCS lane rate, which requires lane reorder and is PHY dependent.

As is in 802.3bs/cn/cu

AUI
50 Gb/s per lane
AUI
100 Gb/s per lane

PMA — PMA — PMA
PMD — PMD — PMD

100 Gb/s per lambda
100 Gb/s per lambda
100 Gb/s per lambda

To be for 200 Gb/s per lambda

AUI
100 Gb/s per lane
AUI
200 Gb/s per lane

PMA — BCH/Hamming — PMD
PMA — BCH/Hamming — PMD
PMA — BCH/Hamming — PMD

200 Gb/s per lambda
200 Gb/s per lambda
200 Gb/s per lambda

*For illustration purpose only. Interleaver is omitted in the diagram.

#3: PMA Muxing Options and Protocol Agnostic Modules

- 2:1 muxing (Tx module) and 1:2 demuxing (Rx module) are required during the transition period when 100 Gb/s per lane AUI and 200 Gb/s per lambda PMD are interoperating.

	Module Muxing Scheme	Performance	Complexity	TX module AM Lock	RX module AM lock	Deskew?	Breakout Friendly?
Symbol Mux (800 GbE and 1.6 TbE)	Specific/Optimal symbol mux (Fully aligned codewords)	Highest	Highest	CM+UM	CM+UM	Full deskew of AUI lanes	No?
	Half-blind symbol mux (Aligned to 4x RS-symbol boundary)	Highest	Higher	CM+UM	CM+UM	40-b deskew	Yes
	Blind symbol mux (Aligned to 1x RS-symbol boundary)	High	High	CM only	CM only	10-b deskew	Yes
	Blind 10-bit/40-bit mux (Un-aligned, arbitrary position)	High	Lower	None	CM only	No	Yes
Hybrid (800 GbE only)	4:1 symbol mux + 2:1 bit mux (802.3df Mux changed)	Low	Lower	None	None	No	Yes
Bit Mux (800 GbE and 1.6 TbE)	2:1 bit mux (1.6TbE assuming 16x100G PCS lanes)	Low	Lower	None	None	No	Yes
	8:1 bit mux (Same as in 802.3df)	Lowest	Lowest	None	None	No	Yes

More protocol agnostic

#4: Interleaver Design Between Inner and Outer Codes

❑ The effect of interleavers has been covered in bliss_3df_01a_220517.

  ➢ Convolutional interleaver can deal with the "bursty" errors from inner code decoders and improve overall coding gain.

  ➢ Channel interleaver on inner code codewords was also discussed to mitigate burst errors from PMD.

❑ Interleaver design should support multiple Ethernet rates and muxing options.

  ➢ All Ethernet rates that could use 200G/lane PMD should be considered: 200 GbE, 400 GbE, 800 GbE and 1.6 TbE.

  ➢ With symbol-muxed AUI lanes, interleaver design for BCH/Hammming(144,136) could be simplified.

❑ Tradeoff needs to be made between implementation cost/latency/power and performance required based on the actual pre-FEC BER threshold for 200 Gb/s per lambda optical PMDs.

  ➢ For latency sensitive applications, interleavers with 50~100 ns extra latency penalty (more than RS(544,514) decoding latency) may not be practical.

❑ One possible approach is to allow bypass of the interleaver(s) for latency sensitive applications.

  ➢ Inner code itself only adds about 2~10ns on top of the RS(544,514) FEC, as shown in [he_b400g_01_210426](he_b400g_01_210426).

#5: Inner Code Delimiting: Blind FEC Frame Synchronization

- **Option C**, aka self-synchronization of inner code, can be achieved by testing a number of target codewords obtained by a sliding window of multiple n-bits, for example n=144 for BCH/Hamming(144,136).

  - **Protocol agnostic:** work with any inner code, independent to logic layer architecture, interleaving mechanism etc.

  - **Does not** require alignment of PCS lanes from AUIs which requires additional logic and buffer inside module.

  - **Does not** need additional alignment markers which requires more logic, low MTTLL and low reliability.

Option A: Fully re-use outer code AM patterns, mapping, insertion and removal mechanism. It will require the inner codeword length to be proportional to the outer codeword length. Bit-transparent optical module and breakout will not be supported.

Option B: Additional new AM for inner code, lead to additional overhead for PLL ratio from 18/17 or 19/17.

Option C: Blind FEC frame synchronization, similar as Clause 74.7.4.7: FEC block synchronization.
It is simpler and requires no special architecture, better in all ways. Preferred.

Conclusions:

- Proposal to adopt BCH/Hamming (144,136) based inner code for P802.3dj "200 Gb/s per lambda" optical PMDs.

  - The code simplifies optical modules design, resulting lower latency, power and cost.

  - Breakout is naturally supported when encoding/decoding is performed per lambda.

Thanks!