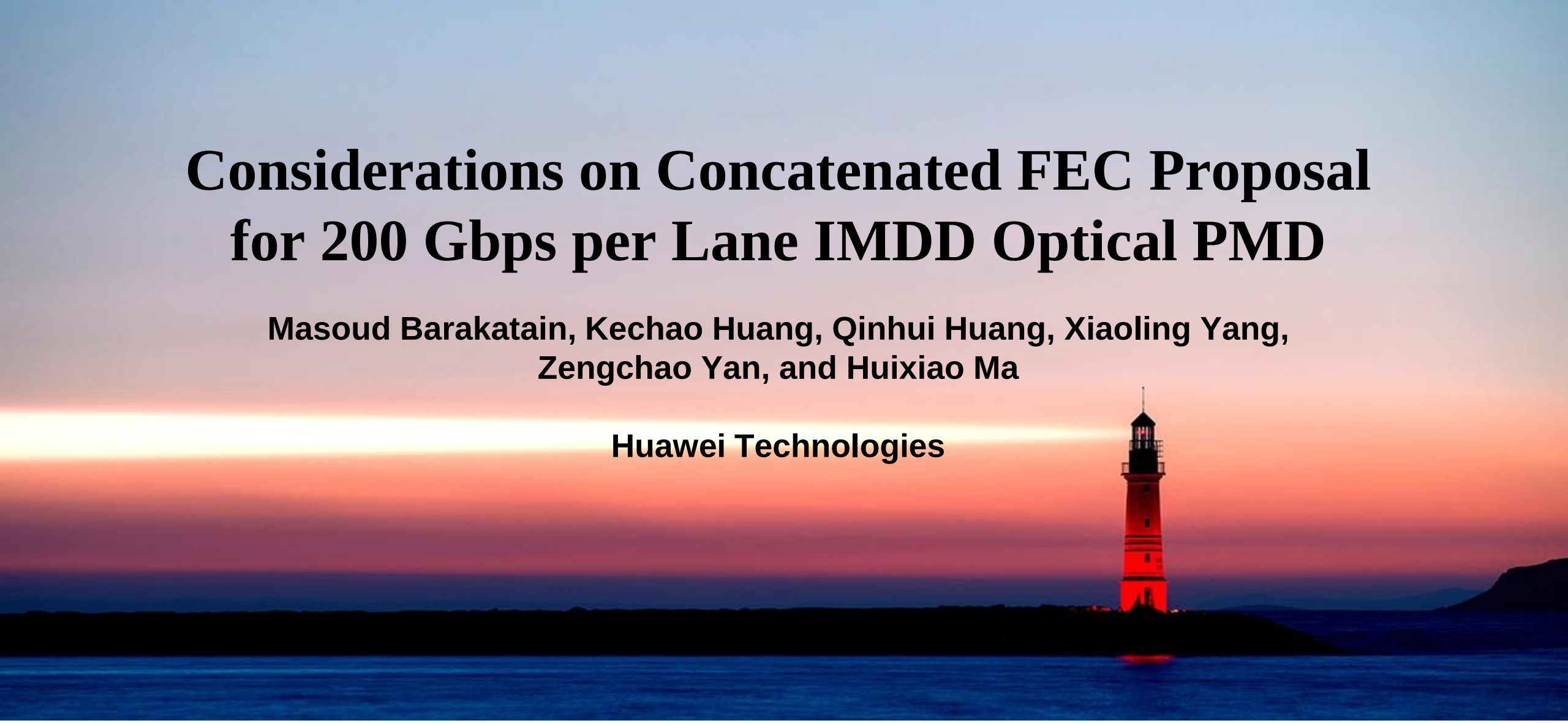


Considerations on Concatenated FEC Proposal for 200 Gbps per Lane IMDD Optical PMD

Masoud Barakatain, Kechao Huang, Qinhui Huang, Xiaoling Yang, Zengchao Yan, and Huixiao Ma

Huawei Technologies

HUAWEI

Background

- In farhood_3dj_01a_230206, an updated SFEC(128,120) proposal with padding was proposed:
  - SFEC(128,120) which acts on the XOR of LSB and MSB channels through a (68,60) Hamming Code
  - Convolutionally interleaved RS symbols passed to the inner code
  - Architecture mainly based on 25G/lane PCS
  - Introducing 384-bit (3x128 bits) padding
  - Padding bits removed at Rx before processing/decoding
  - Straw poll received good support, but some attendees need more information on this proposal:

Straw Poll #10 From motions_3dfdj_a_2301

I support the direction of Concatenated FEC approach, based on the Inner code (128,120) with Padding as per farhood_3dj_01a_230206 for -DR and -FR PMDs based on 200G/lambda IM-DD

Y: 50 , N: 18 , NMI: 45

- In ran_3df_01b_230130, symbol-pair multiplexing constraint was proposed for 200G/lane PMAs:
  - Ensures all RS codewords see LSB and MSB channels equally, avoiding performance degradation
  - Straw poll received strong support:

Straw Poll #7 From motions_3dfdj_a_2301

For 200GBASE-R, 400GBASE-R, and 800GBASE-R PMAs operating at 200 Gb/s per lane, I would support the direction of Symbol-pair multiplexing (as described in ran_3dj_01a_230206)

(choose one)

Y: 43 , N: 4 , NMI: 32

This Proposal

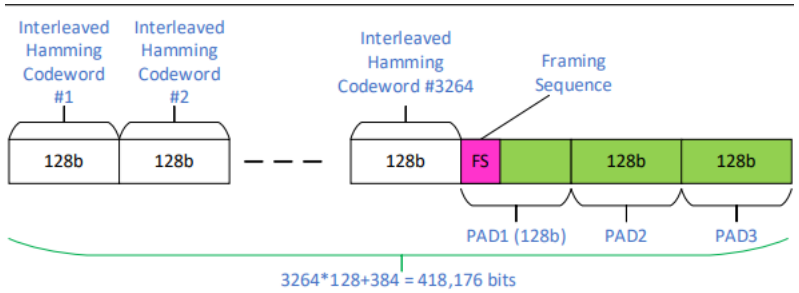
- Provides detailed analysis of the synchronization process in presence of SFEC(128,120) with padding
- Presents high-level architecture that supports 200G, 400G, 800G, and future 1.6T systems
- Details the performance/latency trade-offs involved in the choices we make for the architecture

Summary of the Target System Details

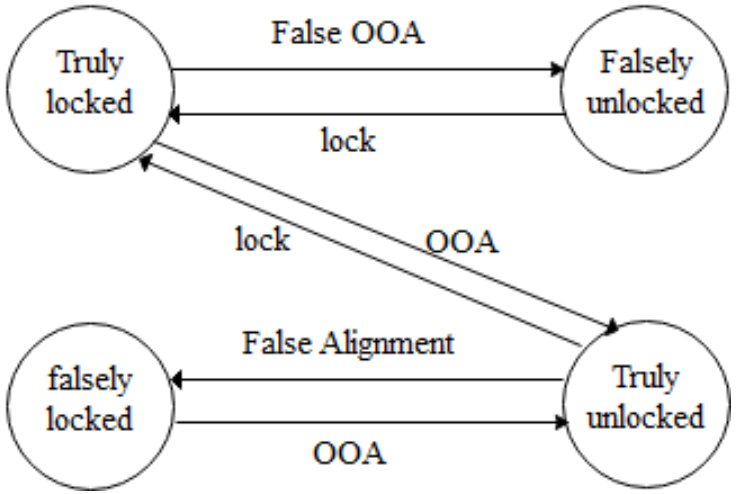
- 800GBASE-DR4, 800GBASE-FR4, and 800GBASE-LR4 PHY is addressed
- Type 2 PHY/FEC: Outer FEC spans multiple AUIs and PMD link (like Type 1), additional inner FEC spans PMD link
- Reported BER assuming no burst errors in the PMD link
- Inner SFEC(128,120) acting on the XOR of LSB and MSB channels through a (68,60) Hamming Code is considered
- Convolutional interleaving (with various latency figures) prior to inner FEC is considered

Analysis on Frame Sync

- Some concerns have been raised about the reliability of the proposed padding. We consider the following:
  - farhood_3dj_01a_230206 considers 48 bits Framing Sequence (FS)
  - FS Lock will be performed before SFEC decoding, where the BER is ~4.8 E-3
- Frame Sync process contains lock and unlock state, each has two sub-states as described below:
  - Locked:
    - Truly locked: frame aligned and the system knows it
    - Falsely unlocked: frame aligned but systems does not know it
  - Unlocked:
    - Truly unlocked: frame not aligned and the system keeps searching
    - Falsely locked: frame not aligned but the system believes it is locked
- Frame Sync mechanism should have the following characteristics:
  - Fast true lock, which implies a short expected time to reach a truly locked state from the truly unlocked state
  - Falsely locked and falsely unlocked states rarely happen. Equivalently, we want a long expected time to reach falsely locked and falsely unlocked states



From farhood_3dj_01a_230206



Recap on 400GE PCS alignment

- Each AM lock process looks for two valid alignment markers
- A valid alignment marker requires 9 or more half-byte nibbles that match (12 nibbles in total)
- Out of lock requires three uncorrectable code words or five alignment markers failures in a row

IEEE 802.3
Clause 119

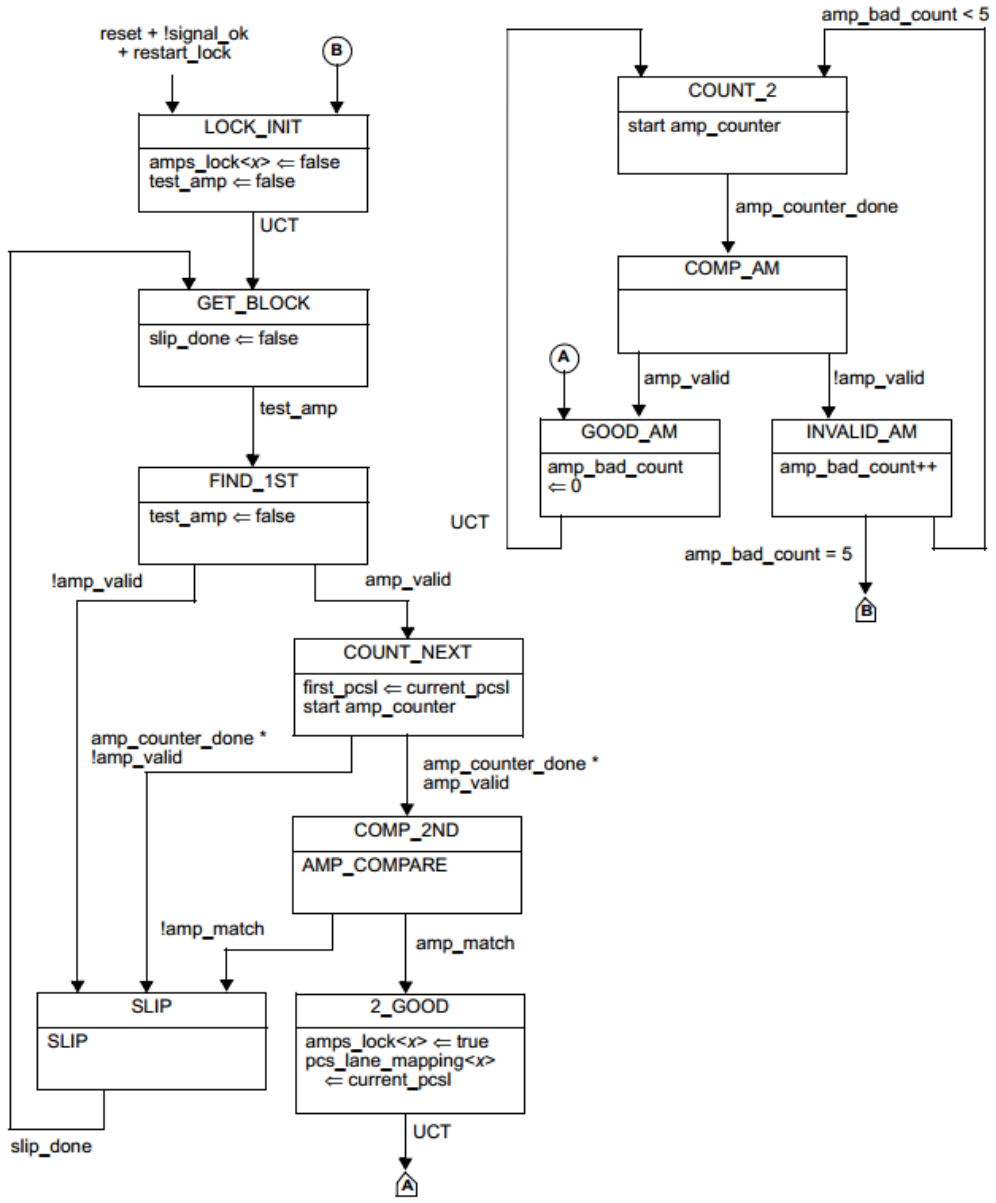
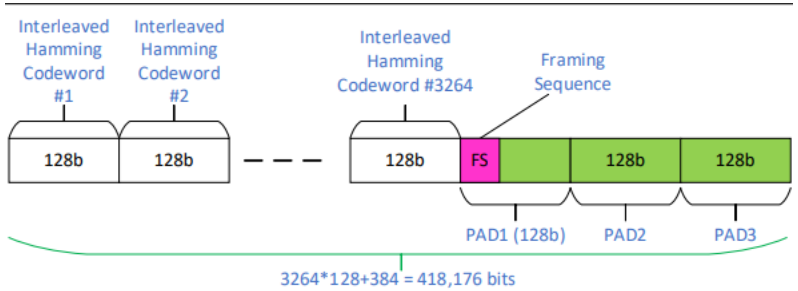


Figure 119–12—Alignment marker lock state diagram

Analysis on Frame Sync

- The analysis based on following assumption:
  - Reuse PCS AM sequence 0x9A4A2665B5D9, as also proposed in farhood_3dj_01a_230206
  - Use 400G PCS AM approach (with various parameters obtained)
    - 6 byte AM divided into 12 half-byte nibbles
    - When m or more nibbles match, it is called a valid FS
    - Each lock looks for n valid FS
    - Out of Lock is when k invalid FS observed



From farhood_3dj_01a_230206

- Probability Calculation:
  - Probability of falsely locked P_{fl}: equals to p_{fl}^{n}, where $p_{fl} = \sum_{i=m}^{12}\binom{12}{i}(1-p_0)^i * p_0^{12-i}$), with $p_0 = 15/16$ corresponding to a mismatched nibble.
  - Probability of falsely unlocked P_{fu}: equals to p_{fu}^{k}, where $p_{fu} = \sum_{i=0}^{m-1}\binom{12}{i} * p_1^{12-i} * (1-p_1)^i$, with $p_1 = 1-(1-\mathrm{BER})^4$, where BER=4.8e-3 is assumed in the tables below.
  - Mean time to truly locked state is roughly estimated by (n -0.5)×group delay, where group delay corresponds to ~1.8μs (418176 bits)

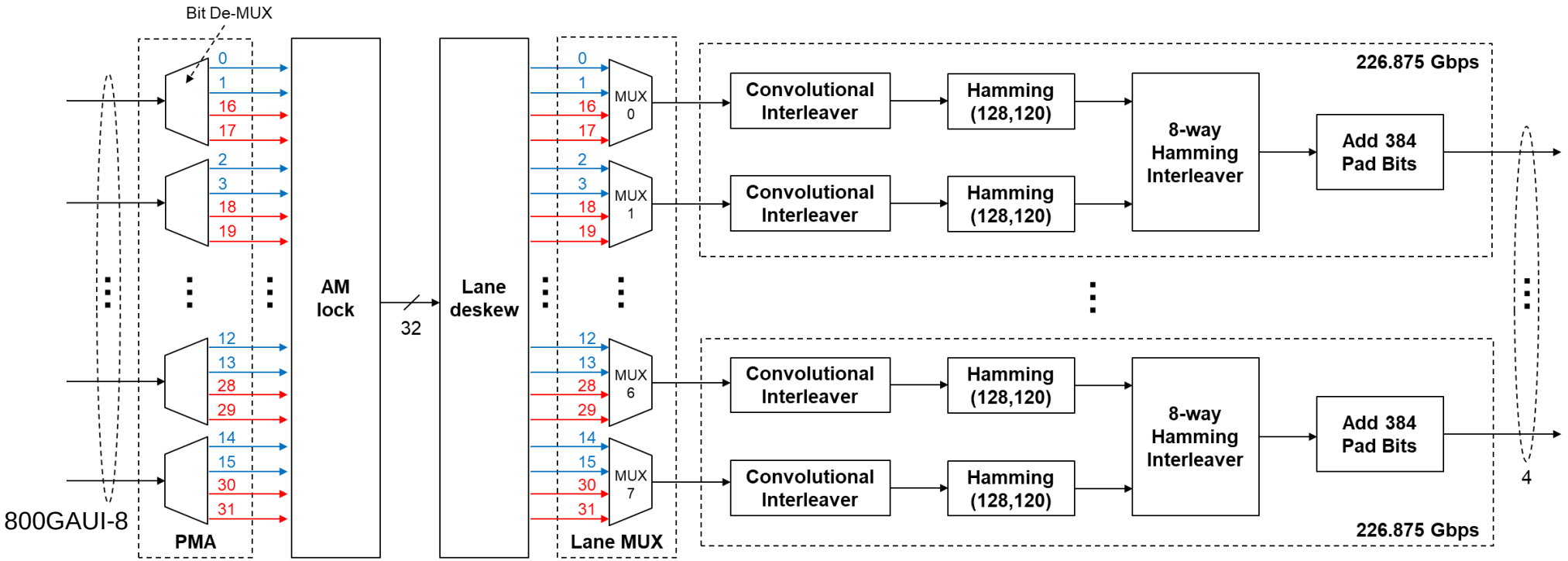
		Mean time to false alignment (years)		
threshold m	P_fl	n=2	n=3	n=4
12	3.55E-15	1.16E+15	3.26E+29	9.17E+43
11	6.43E-13	3.57E+10	5.59E+22	8.74E+34
10	5.34E-11	5.25E+06	9.95E+16	1.89E+27
9	2.69E-09	2.10E+03	7.96E+11	3.02E+20
8	9.17E-08	1.84E+00	2.07E+07	2.33E+14
7	2.23E-06	3.20E-03	1.50E+03	7.01E+08

		Mean time to false unlock (years)			
threshold m	P_fu	k=3	k=4	k=5	k=6
6	6.58E-10	2.05E+14	3.12E+23	4.74E+32	7.21E+41
7	4.02E-08	9.03E+08	2.25E+16	5.60E+23	1.39E+31
8	1.78E-06	1.03E+04	5.79E+09	3.25E+15	1.82E+21
9	5.78E-05	3.02E-01	5.23E+03	9.05E+07	1.57E+12
10	1.34E-03	2.43E-05	1.82E-02	1.36E+01	1.01E+04
11	2.11E-02	6.20E-09	2.94E-07	1.39E-05	6.58E-04
12	2.06E-01	6.66E-12	3.23E-11	1.57E-10	7.60E-10

Remark：highlighted with green represent greater than AOU.

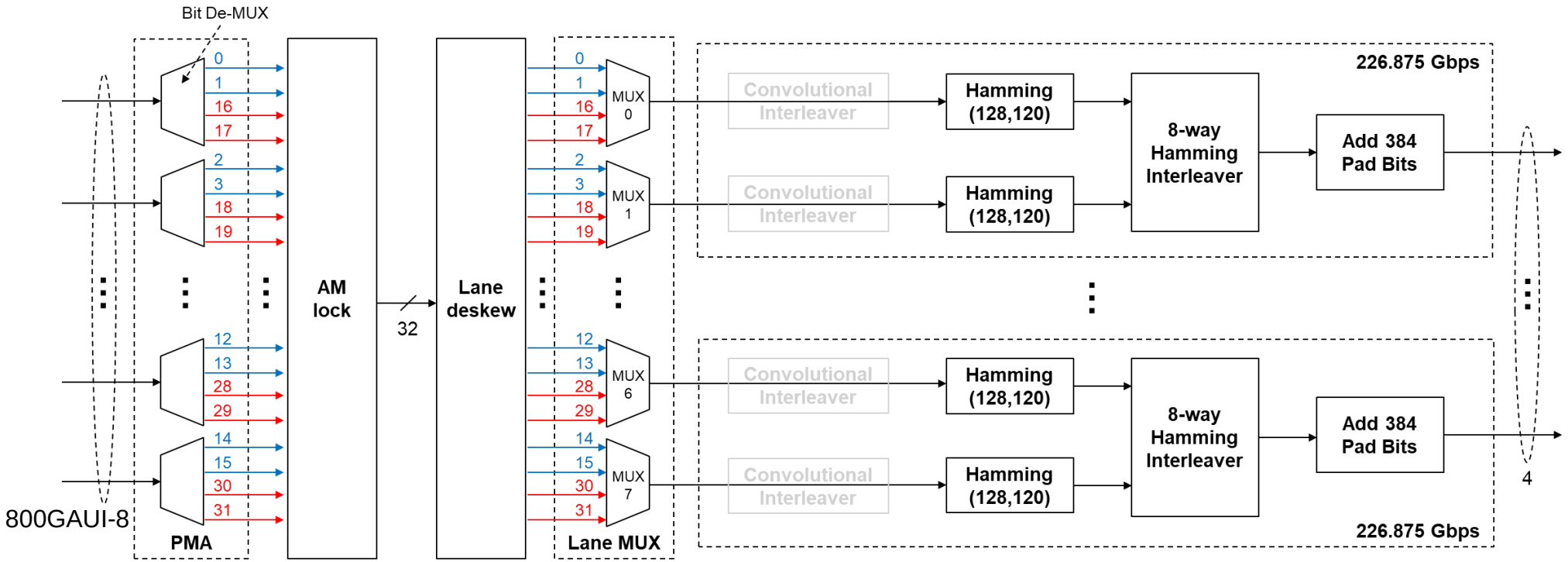
Concatenated FEC with 100G SFEC Lanes

- In huang_3df_01a_2211 an architecture was proposed with 100G SFEC lanes for 800G host with 100G or 200G per lane AUI
  - 100G PCS lanes preferred for future 1.6T system architectures; see gustlin_3dj_01b_230206 baseline proposal, passed with unanimous consent at motion #10 in motions_3dfdj_2301
  - The proposal in farhood_3dj_01a_230206 is based on 25G SFEC lanes which may not be forward-compatible with the 1.6T baseline
  - huang_3df_01a_2211 proposes 8 SFEC lanes each carrying 100G through the convolutional interleaver and SFEC(128,120)
  - Naturally supports breakout as data on each lambda is not commingled with data on other lambdas



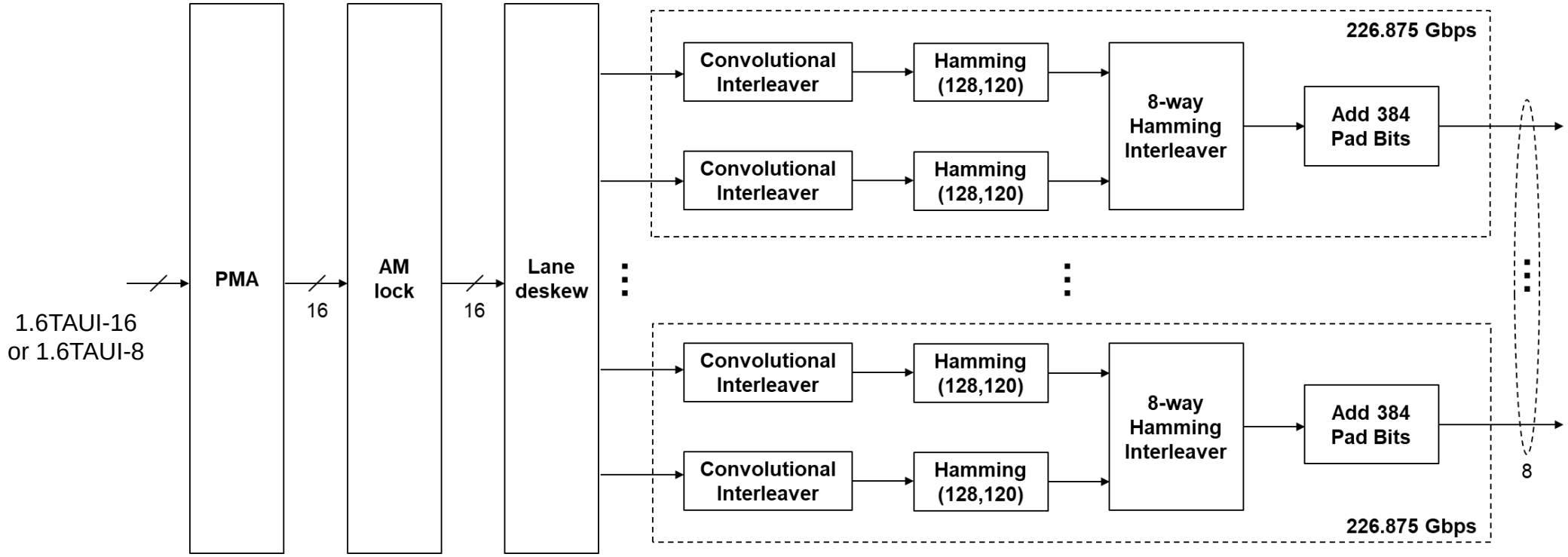
Concatenated FEC with 100G SFEC Lanes

- huang_3df_01a_2211 proposal supports bypassing the convolutional interleaver to achieve low latency
  - Bypassing interleaver does not depend on the choice of the inner code
  - However, a bypass architecture cannot interoperate other modules with convolutional interleaver



Concatenated FEC with 100G SFEC Lanes

- Forward compatibility with future 1.6TbE with 16x100G/PCS lane baseline



It can easily be extended to 200G SFEC Lanes.

SFEC and Interleaver Details for 100G SFEC Lanes

Detailed parameters of SFEC and the interleaver in the concatenated FEC solution with 100G SFEC lanes

Ethernet Rate (GbE)		# of SFEC Lanes	# of Intlvr. Delay Lines	Intlvr. Storage Element (# of bits)	Intlvr. Latency	Pre-FEC BER
High Performance	400	4	6	23*20	~130 ns (13,800 b)	4.8E-3
	800 (2-way interleaved)	8	6	23*20	~130 ns (13,800 b)	
	800 (4-way interleaved)	8	3	23*40	~52 ns (5,520 b)	
	1600 (TBD)	16	3	23*40	~52 ns (5,520 b)	
Low Latency	400	4	3	23*40	~52 ns (5,520 b)	4E-3
	800 (2-way interleaved)	8	3	23*40	~52 ns (5,520 b)	

Conclusions

- SFEC(128,120) + padding is considered and detailed analysis on the synchronization process for the padded bits is provided
  - Fast and true lock is desired for the alignment of the padding bits
  - A similar approach to that of AM lock in 400G PCS is adopted
  - A set of parameters is obtained guaranteeing true lock with very high probability, with expected time to failure > AOU
- A high-level architecture is proposed for the optical module based on 100G SFEC lanes
  - Supports 200G, 400G, 800G
  - Forward-compatible with the 1.6T baseline
  - Supports bypassing the interleaver for ultra-low latency
  - Supports breakout
- Parameters of choice are laid out for interleaver and SFEC in the concatenated solution with 100G SFEC lanes

Thank you