FEC Options for 200G/Lane DRn, DRn-2, and FR1

Piers Dawe, Bill Simms, and Vishnu Balan
NVIDIA

Acknowledgements

- Contributors
  - Bill Simms - NVIDIA
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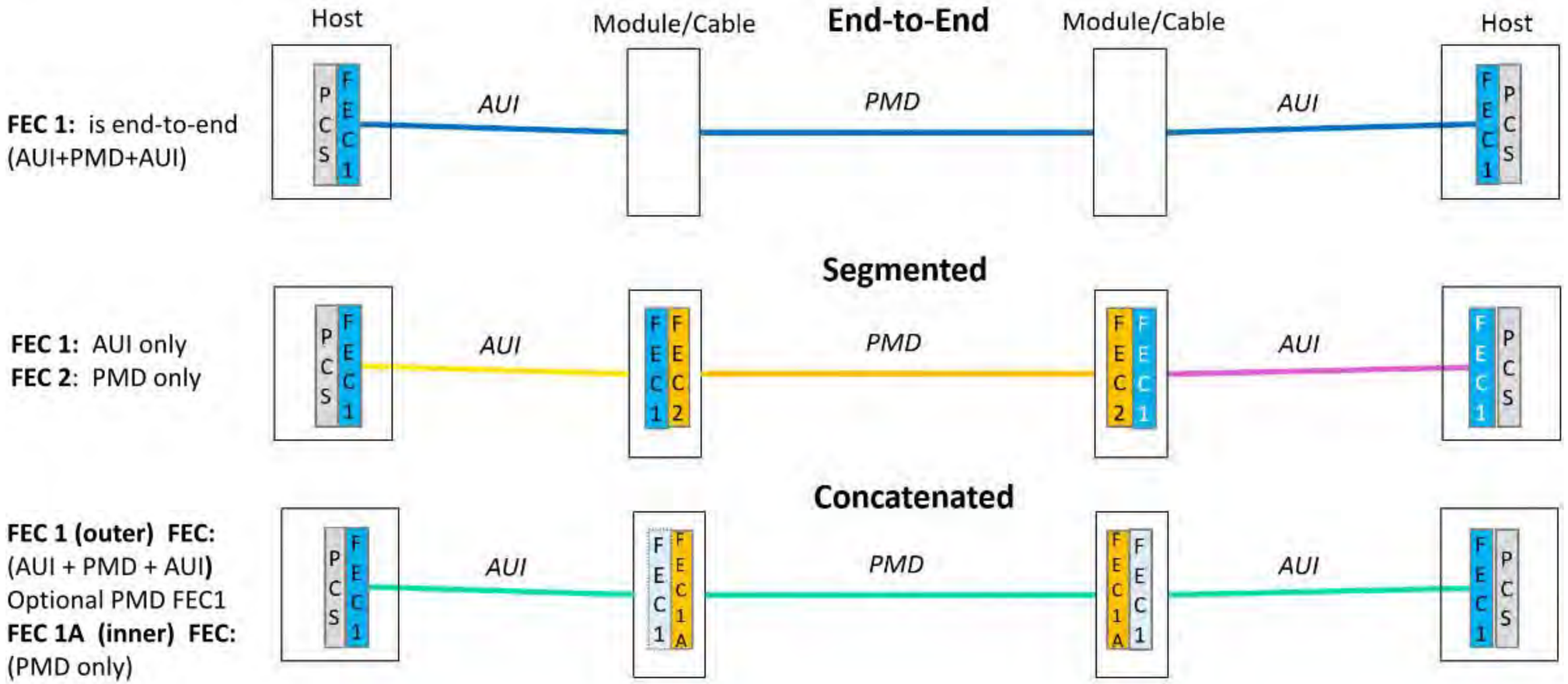
Objectives

- Revisit a low-latency end-to-end FEC option for DR channels at 200G/lane
  - Leverage existing 100G/lane infrastructure and simply double the bandwidth
- Add optional support for SD-FEC
  - Bypass when not needed to reduce power and latency
- Avoid convolutional interleaver to minimize latency

Review – farhood_3df_02b_2211

Reviewed FEC architectures
Concatenated FEC could be bypassed to provide End-to-End RS544

Refresh of FEC Architecture already discussed in this forum: End-to-End, Segmented, Concatenated scheme



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Review – he_3dj_02a_230206

Demonstrates latency increases due to use of convolutional interleaver, hard decision, and soft decision inner FEC

Tradeoff Between Latency and Pre-FEC BER Threshold

- Inner code itself does not require the convolutional interleaver to work.
  - Concatenated code performance without convolutional interleaver has been analyzed in he_3df_01_2211.pdf.
- For links that has lower pre-FEC BER levels, convolutional interleaver can be bypassed.
  - 800 GbE PCS layer provides 4 codewords interleaving (likely for 1.6 TbE, too), which can provide moderate protection.
- For links that meets RS(544,514) threshold, the inner code can be bypassed completely.
- Tradeoff between latency and pre-FEC BER threshold can be made.
  - Bypass configuration can either be static or configurable.

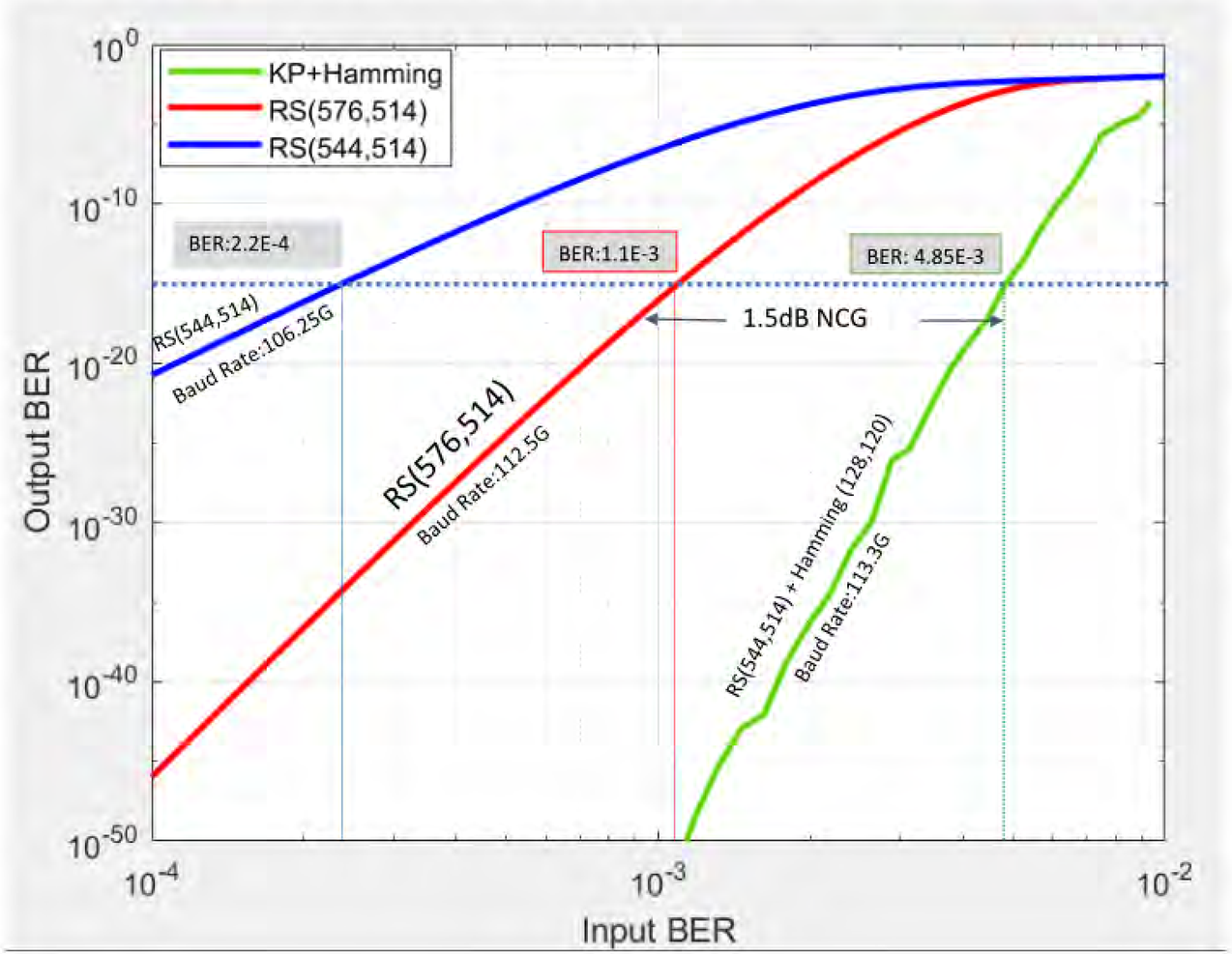
BER Threshold	Bypass Convo. Interleaver	Bypass Inner Code	Inner Code Decoder: Soft or Hard Decision	Inner Code Total Latency
4.6E-3	No	No	Soft	50~300 ns
3.3E-3	Yes	No	Soft	5~10 ns*
6.1E-4	Yes	No	Hard	1~2 ns*
2.4E-4	Yes	Yes**	--	0 ns*

*Based on 200G/lane throughput, same for all Ethernet rates from 200 GbE to 1.6 TbE.
**Bypassing inner code will lead to different PMD rate.

Review – patra_3df_01_220518

Demonstrates performance of RS(544,514)+Hamming(128,120) over RS(544,514) alone

Performance of KP4 FEC Vs RS(576,514) Vs KP4 + Hamming (128,120)



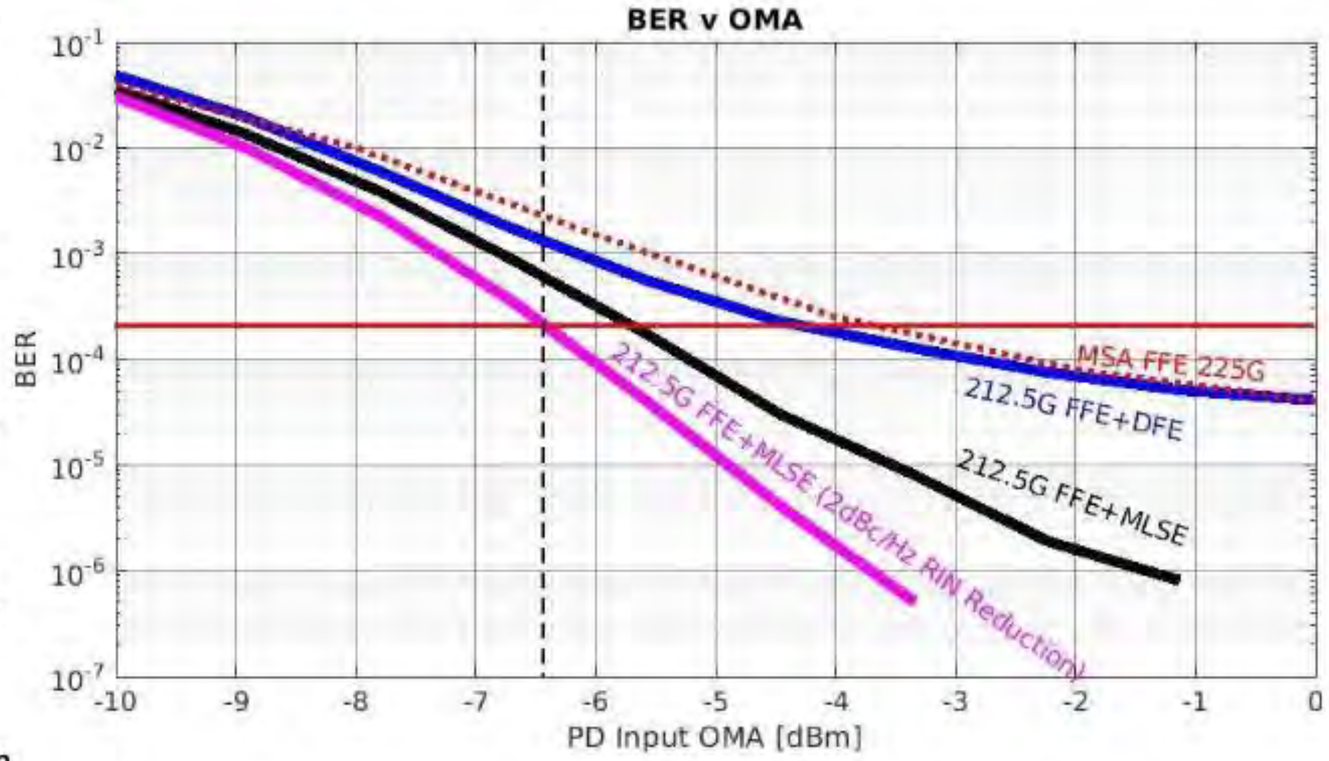
KP4 + Hamming (128,120)
Vs RS(576,514):

Net Coding gain increase : 1.5dB with very similar overhead

Review – simms_3df_01_221005

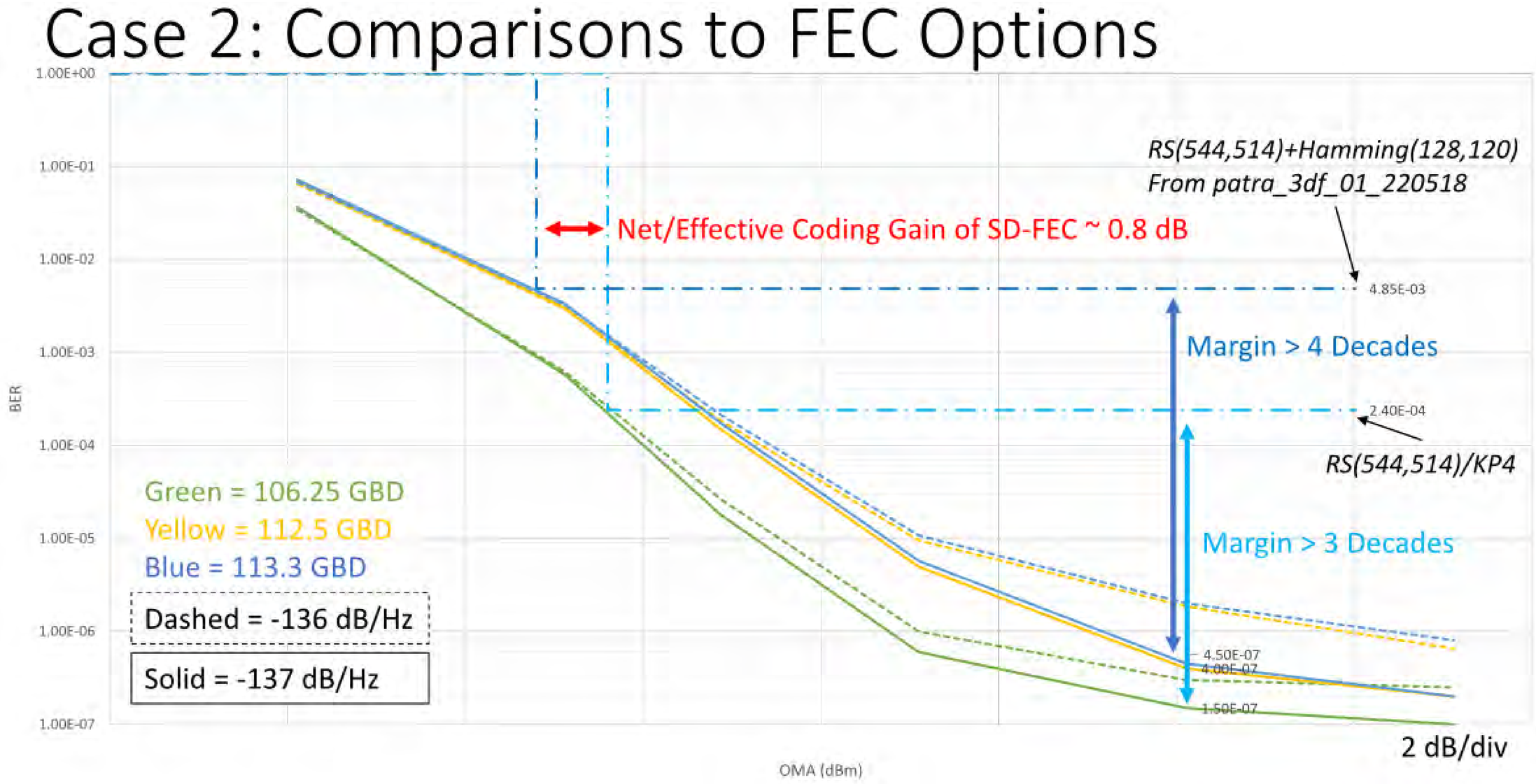
Demonstrated feasibility of end-to-end RS544 FEC using improved link parameters
No SD-FEC required to operate 800GBASE-DR4 links

- A plot of BER vs. OMA (at the Rx photo-diode) is shown for 212.5 Gbps:
  - Baseline EQ : FFE + 1-tap DFE (Blue)
  - Advanced EQ : FFE + MLSE (Black)
  - Advanced EQ : FFE + MLSE + Reduced RIN (Magenta)
  - 800G MSA shown for reference (Red dotted)
- BER target of 2 x 10^{-4} (Red) can be achieved under given conditions
- We can rely on end-to-end KP4 RS(544,514) FEC in the host under the usual assumptions that the AUI links can meet BER of 10^{-5} or better
- With this example the link budget is closed with -6.4dBm



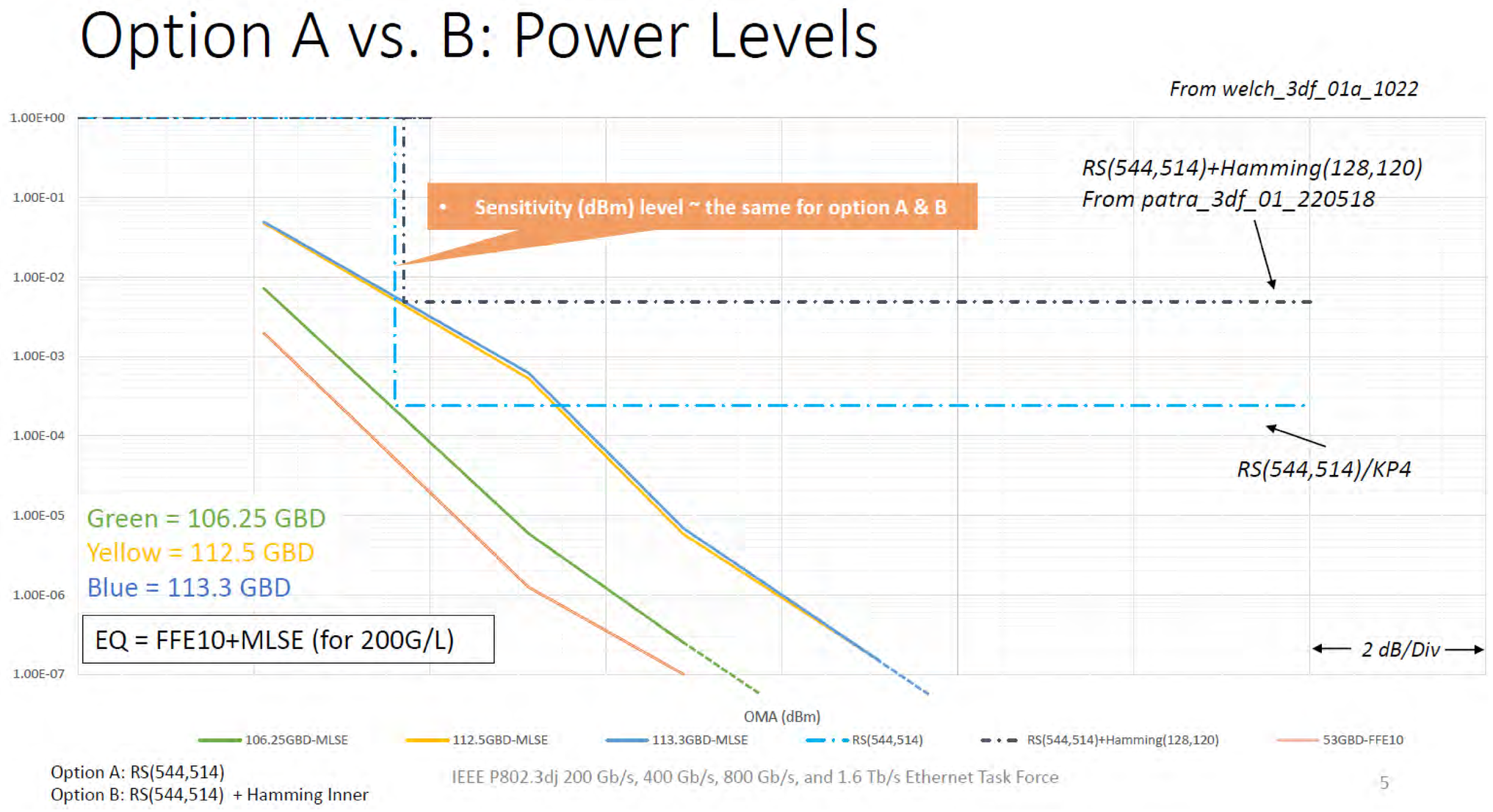
Review – welch_3df_01a_221011

Demonstrates FEC options with DFE1 and Rin improved to -137dB/Hz



Review – welch_3dj_01a_230206

Demonstrates closed link budget with OMA 1dB improved over 100G. SD_FEC has similar sensitivity level

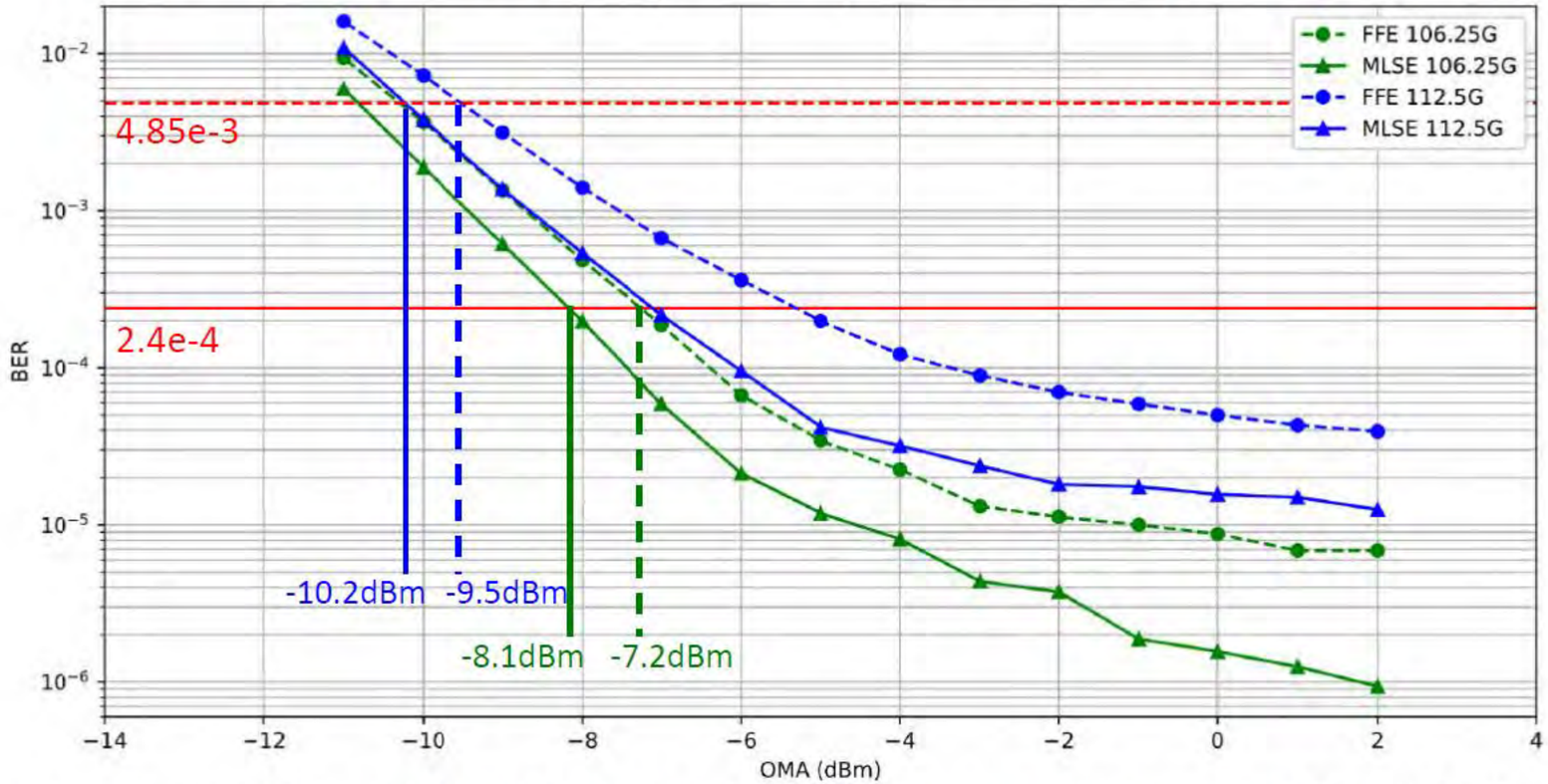


Option A: RS(544,514)
Option B: RS(544,514) + Hamming Inner

Review – li_3dj_01a_230206

Feasibility of 106.25 GBd MLSE and FFE (roughly 2 dB OMA margin for inner FEC)

Simulation results (2km, 106.25/112.5GBd)



- -8.1dBm Rx sensitivity with MLSE for 106.25GBd can meet RS(544,514) BER standard
- -10.2dBm Rx sensitivity for 112.5GBd of RS(544,514)+Hamming(128,120)
- Considering 1dB EOL aging margin, OMA Rx sensitivities of -7.1dBm and -9.2dBm could be feasible for two signaling rates, respectively

Conclusion

- Simulation results for a DR (500 m, SMF) channel which closes the link budget without requiring an SD-FEC in the module for pluggables
  - Best for low power and low latency operation
  - Reviewed prior presentations which arrive at same conclusion and similar results
- A bypassable SD-FEC (Hamming 128/120) may be used for higher loss systems (FR and DR4-2) where the extra power is needed to guarantee system operation and extra latency can be tolerated
  - May allow for design reuse between DR4 and FR4/DR4-2 systems
  - Requires BW increase and circuit optimization
- Avoid convolutional interleaver to reduce latency, area, and power

References

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Thank You