



# Architectural Considerations for Type 2 PHY/FEC Scheme (Concatenated FEC) for 200G per Lane IMDD

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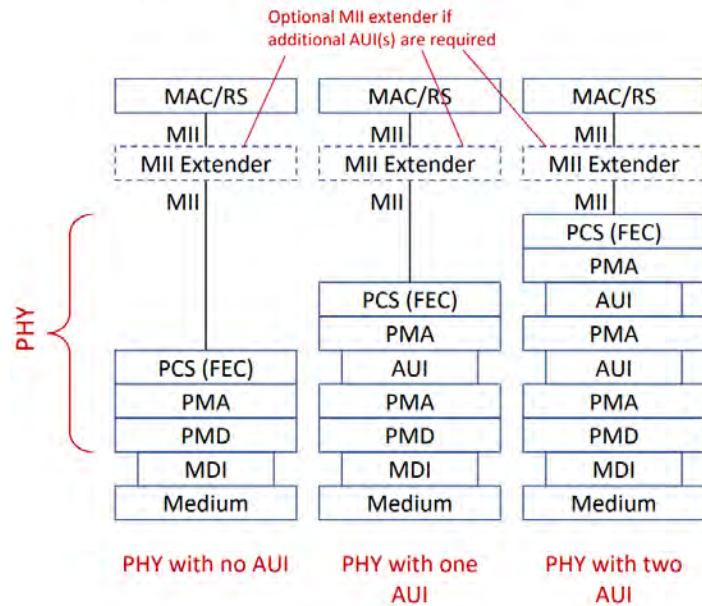
# Introduction

- Before we can develop a full baseline for Type 2 PHY/FEC, we need to reach consensus on the architecture first.
- The intention is to provide the architecture for all the Ethernet rates from 200GE to 1.6TE.
- The intention is to be inclusive of all proposals being considered.

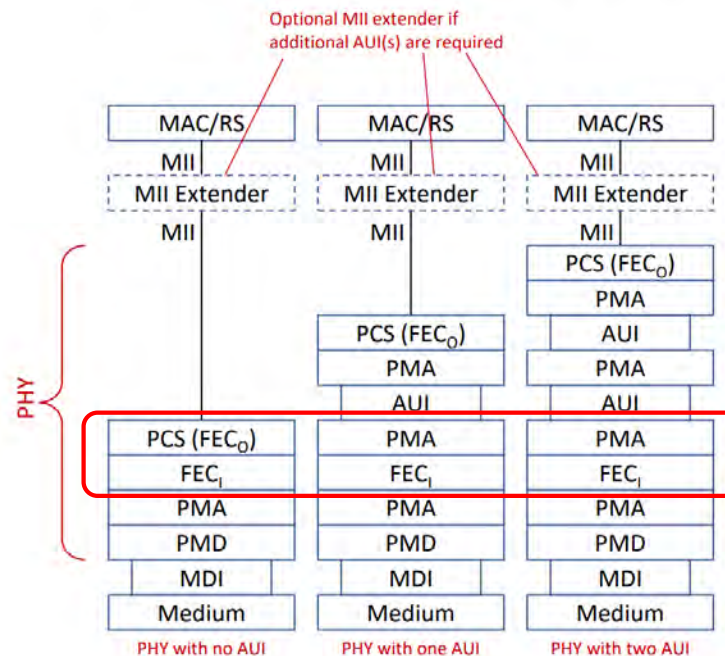
# Type 1/2/3 PHY/FEC Schemes

- In [brown\\_3dj\\_optx\\_adhoc\\_01a\\_230222](#), three types of PHY/FEC schemes were named and illustrated.
- The PMA below  $FEC_1$  is different from the BASE-R PMA, and requires dedicated clauses to describe the functions and service interfaces.
  - $FEC_1$  is referred to as  $FEC_I$ , and PMA below  $FEC_1$  is referred to as  $PMA_I$  in this presentation.

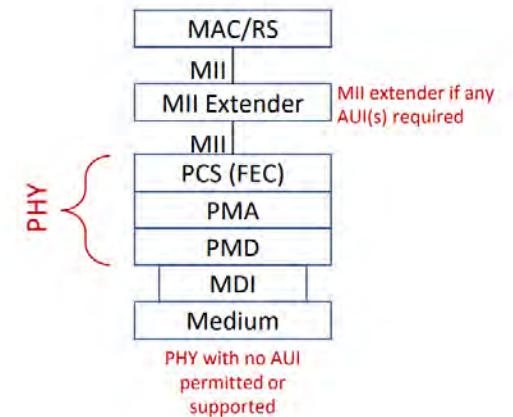
## Type 1 PHY/FEC scheme



## Type 2 PHY/FEC scheme



## Type 3 PHY/FEC scheme



# List of Things to Consider

1. PHYs being addressed
2. PHY/FEC type
3. # of AUIs per PHY link
4. Assumed BER per AUI and burst error characteristics
5. PMD Link Burst Error Characteristics
6. Inner FEC Encode
7. Inner FEC pre-encoding interleaving characteristics
8. Post-encoding interleaving

# PHYs Being Addressed

Ethernet Rate	Assumed Signaling Rate	AUI	BP	Cu Cable	MMF 50m	MMF 100m	SMF 500m	SMF 2km	SMF 10km	SMF 40km
200 Gb/s	200 Gb/s	1 lane		1 pair			1 pair	1 pair		
400 Gb/s	100 Gb/s							4 pairs		
	200 Gb/s	2 lanes		2 pairs			2 pairs			
800 Gb/s	100 Gb/s	8 lanes	8 lanes	8 pairs	8 pairs	8 pairs	8 pairs	8 pairs		
	200 Gb/s	4 lanes		4 pairs			4 pairs	1) 4 pairs 2) 4 λ's		
	200 Gb/s (TBD)								Single SMF 4 λ's (TBD)	
	800 Gb/s (TBD)								Single SMF 1 λ (TBD)	Single SMF 1 λ (TBD)
1.6 Tb/s	100 Gb/s	16 lanes								
	200 Gb/s	8 lanes		8 pairs			8 pairs	8 pairs		

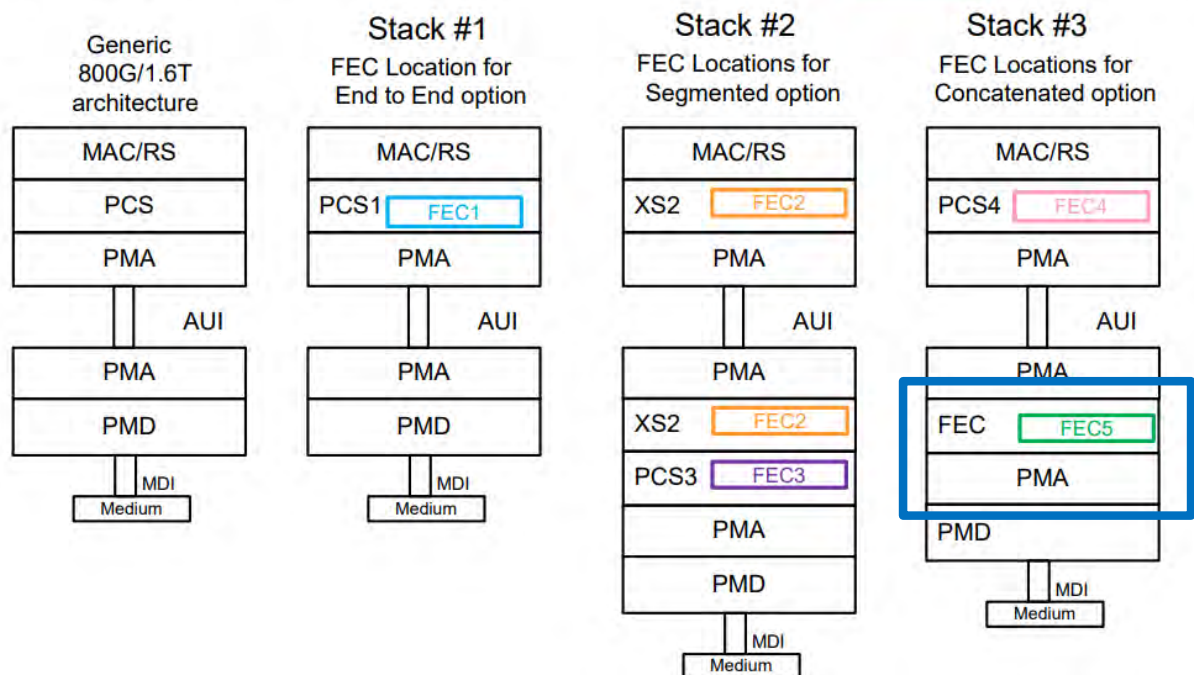
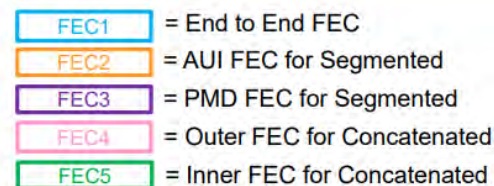
- Assuming that a concatenated inner FEC is required, this may apply to all PHYs highlighted.
- Two AUI segments each side can be supported if the BER for each is below 5E-5.
- One AUI segment with higher BER (<1E-4) can be allowed on each side.

# Fit Into the Adopted Architecture

- This proposal fits within the adopted 802.3dj logic architecture.

## Proposed 800GbE/1.6TbE Architecture

- How various FEC schemes fit into the architecture
- FECs might or might not be reused across schemes

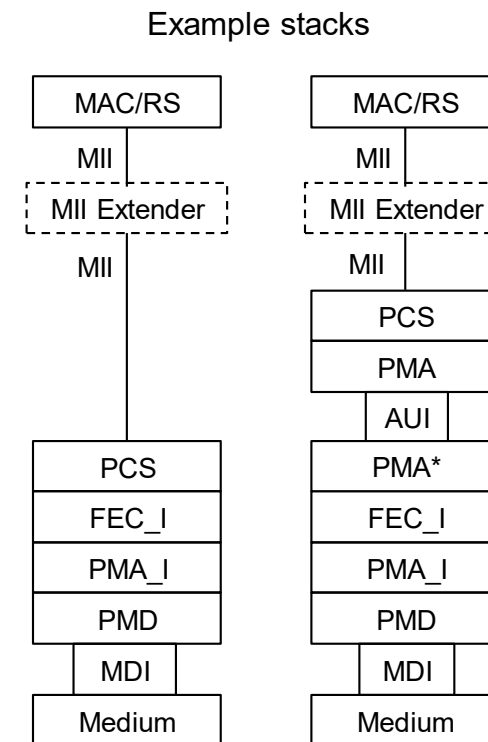
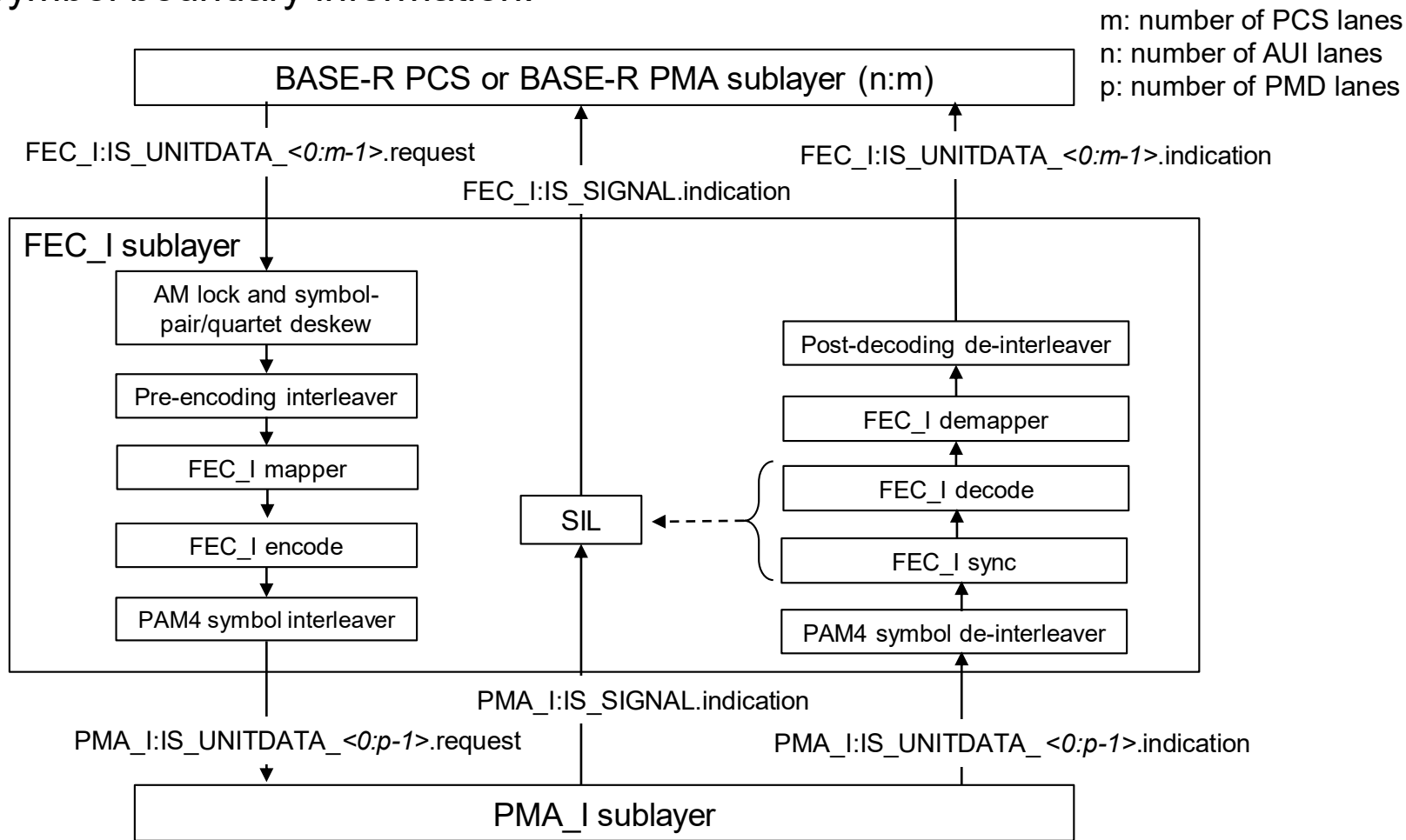


# New Clauses and Subclauses

- Overview
  - Scope of inner FEC (FEC\_I) and PMA\_I sublayer, type 200GBASE-DR1/FR1, 400GBASE-DR2, 800GBASE-DR4/DR4-2/FR4/LR4 and 1.6TBASE-DR8/DR8-2
  - Relationship of FEC\_I and PMA\_I sublayers to other standards
  - Inter-sublayer interfaces
  - Functional block diagram
- FEC\_I (Inner FEC) sublayer
  - Transmit: pre-encoding (convolutional) interleaver, FEC\_I encode and post-encoding (PAM4 symbol) interleaver
  - Receive: pre-decoding (PAM4 symbol) de-interleaver, FEC\_I sync, FEC\_I decode and post-decoding de-interleaver
  - Bypass of pre-encoding interleaver
  - FEC\_I degrade monitoring
- PMA\_I sublayer
  - Overview
  - Service interface
  - Functions within the PMA, including soft-decision information for FEC\_I decoding.
- Detailed functions and state diagrams
- Delay constraints

# Transmit and Receive Flow of FEC\_I Sublayer

- Rely on BASE-R PMA FEC-symbol-pair muxing discussions for 200G/lane PMDs.
- The “AM lock and symbol-pair/quartet deskew” function is required if BASE-R PMA does not provide symbol boundary information.

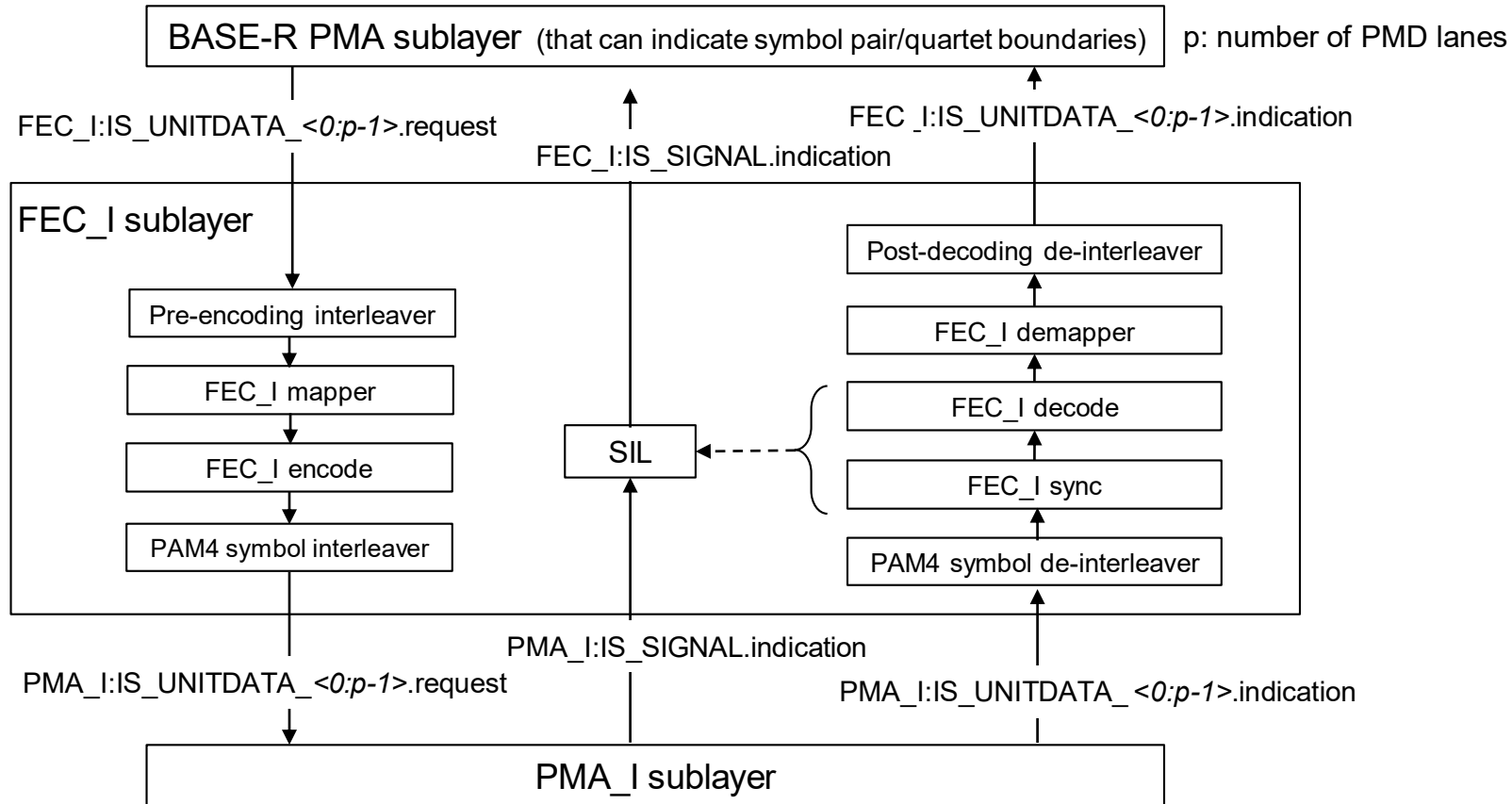


\* This BASE-R PMA is bit-muxing PMA

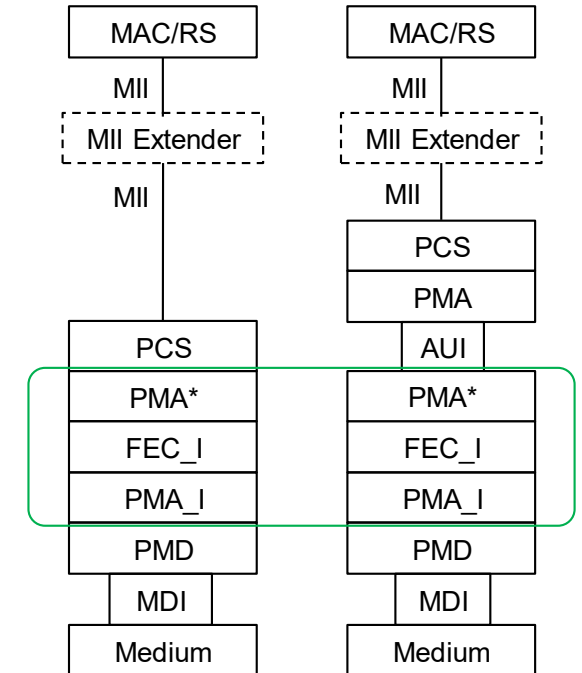


# Transmit and Receive Flow of FEC\_I Sublayer (alternate)

- Rely on BASE-R PMA FEC-symbol-pair muxing discussions for 200G/lane PMDs.
- The BASE-R PMA indicates the symbol-pair/quartet boundary, or transmit symbols in 20b/40b groups.



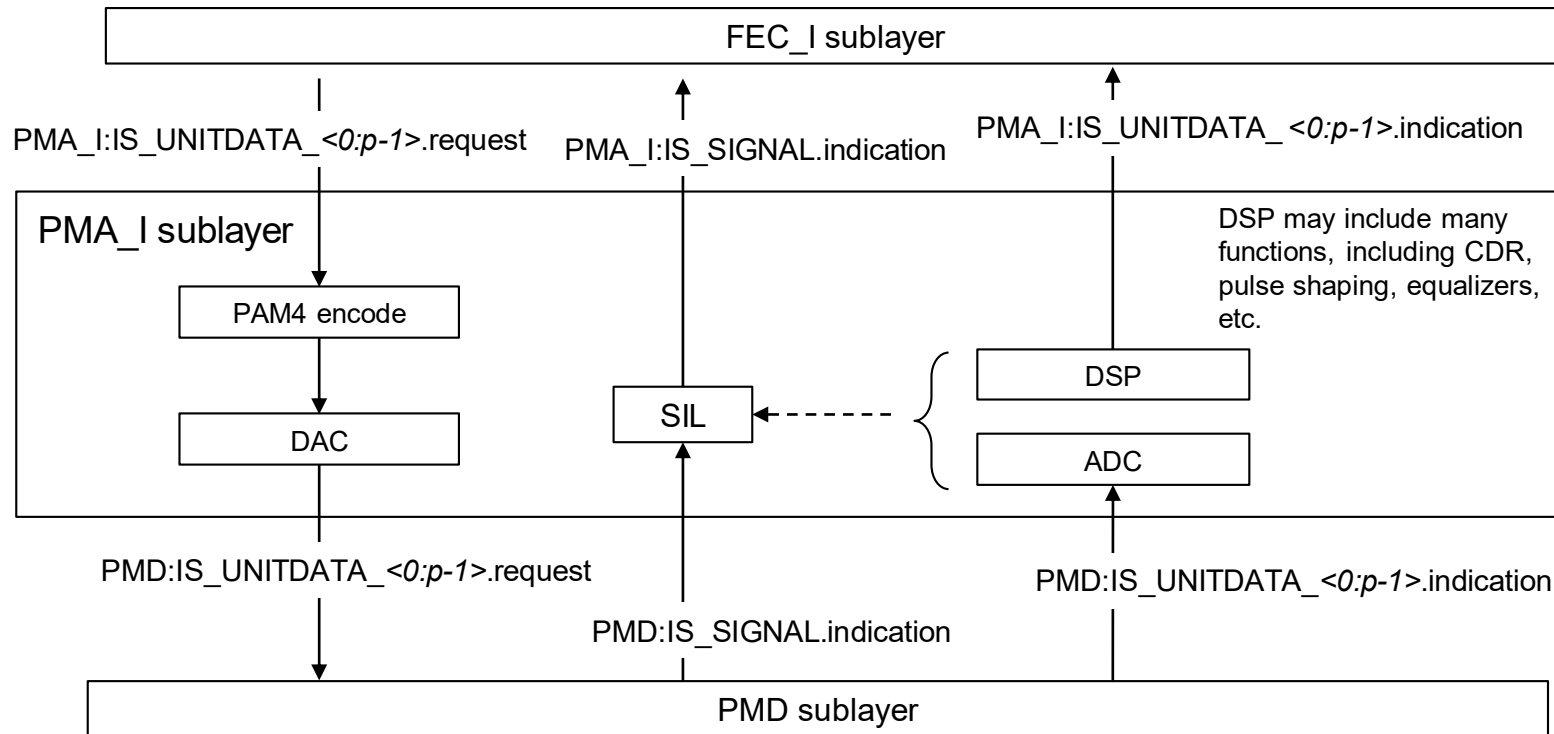
Example stacks



\*This BASE-R PMA is the new PMA discussed in ran\_3dj\_01\_2303.

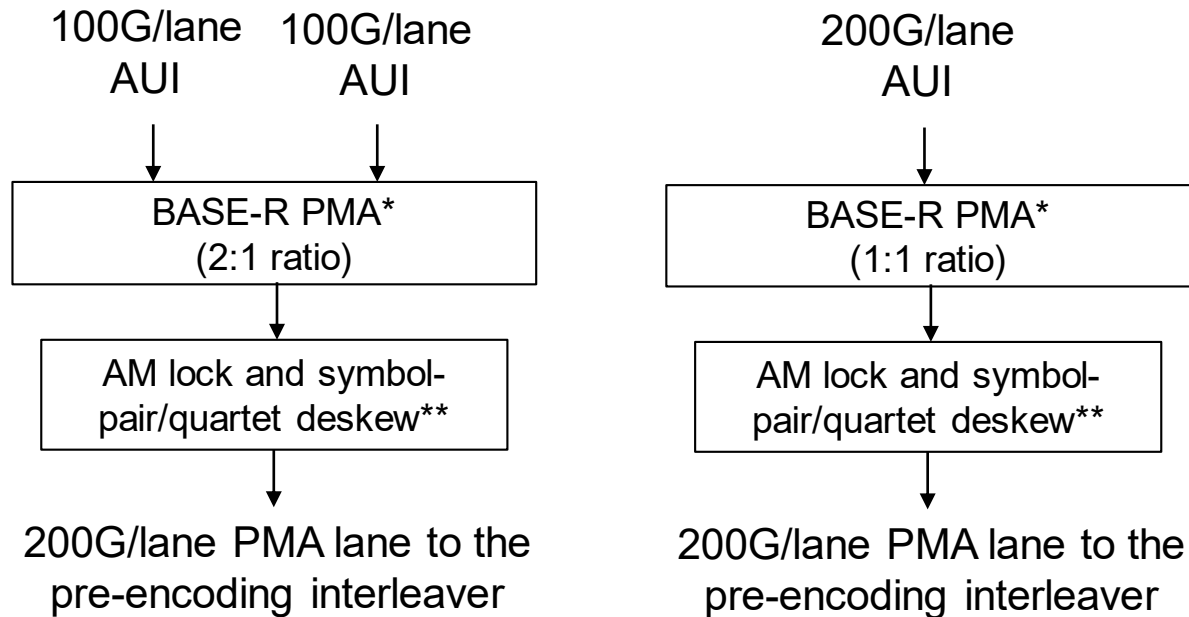
# Transmit and Receive Flow of PMA\_I Sublayer

- The PMA service interface is provided to allow the inner FEC sublayer to transfer information to and from the PMD sublayer.
- The PMA\_I:IS\_UNITDATA.indication primitive defines the transfer of a FEC\_I codeword from the PMA\_I to the FEC\_I sublayer via the (rx\_symbol) parameter.
  - The rx\_symbol parameter conveys the sampled PAM4 symbols, and the resolution is implementation dependent.



# Transmit Functions – AM lock and symbol-pair/quartet deskew

- Data obtained from PMA shall be aligned to symbol-pair (20b) boundary for 200 GbE and 400 GbE, or symbol-quartet (40b) boundary for 800 GbE and 1.6 TbE.
  - There is no need to perform full PCS lane deskew.
- It is recommended to include this function in the BASE-R PMA, and making the FEC\_I sublayer generic through all Ethernet rates with 200G/lane optical PMDs.

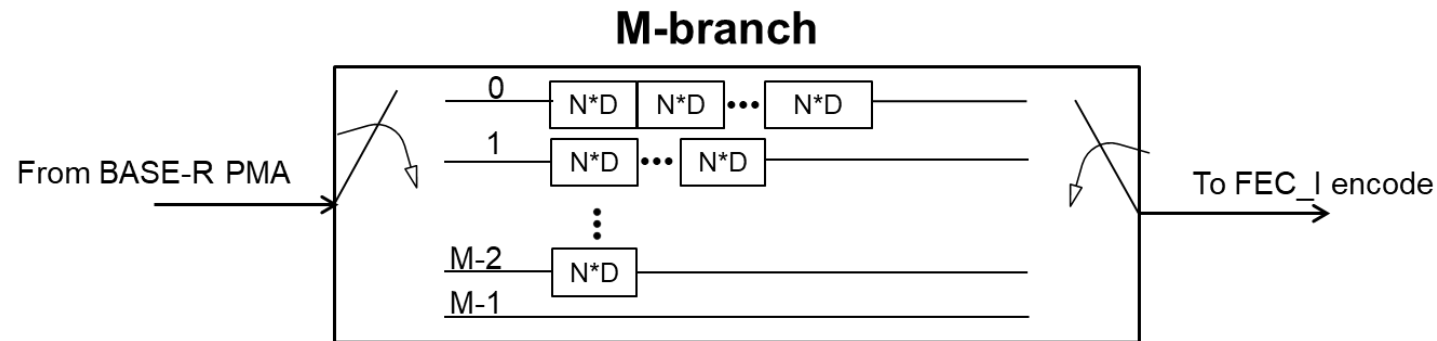


\* See ran\_3dj\_01\_2303

\*\* Not needed if pre-encoding interleaver is bypassed

# Transmit Functions – Pre-encoding interleaver

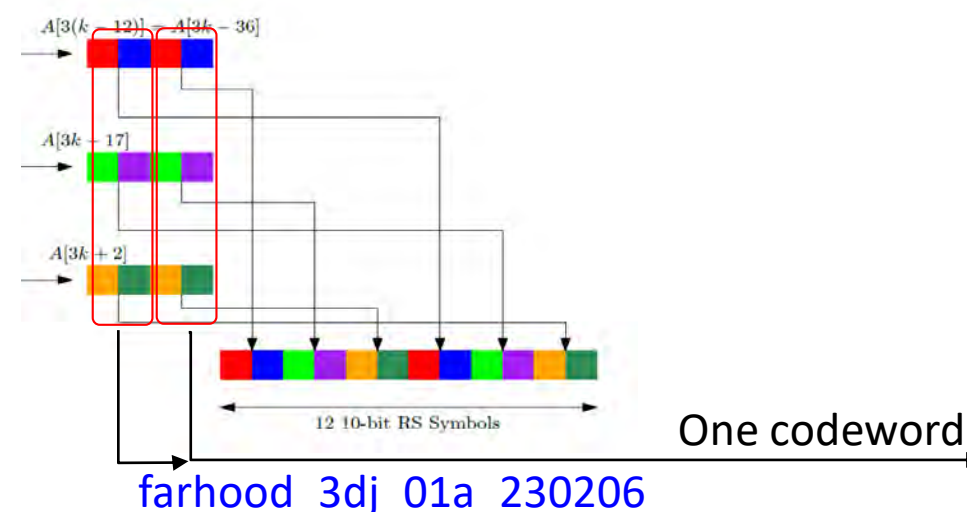
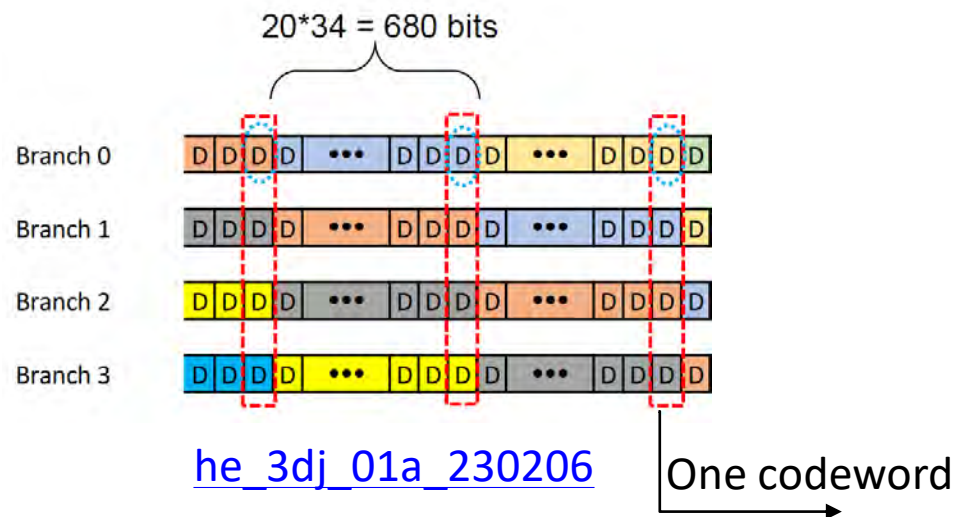
- The pre-encoding interleaver is a convolutional interleaver which could have a lower latency than a block interleaver with the same interleaving depth.
  - It contains  $M$  parallel delay lines (branches) with decreased delays from branch 0 to  $M-1$ .
  - Data sequence from the BASE-R PMA lane is distributed in fixed-size blocks to the  $M$  branches sequentially in a round-robin fashion.
  - The number  $M$ ,  $N$  and  $D$  are code dependent.



- The pre-coding interleaver should be excluded for DR/DR-2 links.
  - Preferred to be PMD dependent. It can also be transmitter controlled.
  - For DR/DR-2 links, data from BASE-R PMA can be directly encoded by FEC\_I.

# Transmit Functions – FEC\_I Mapping

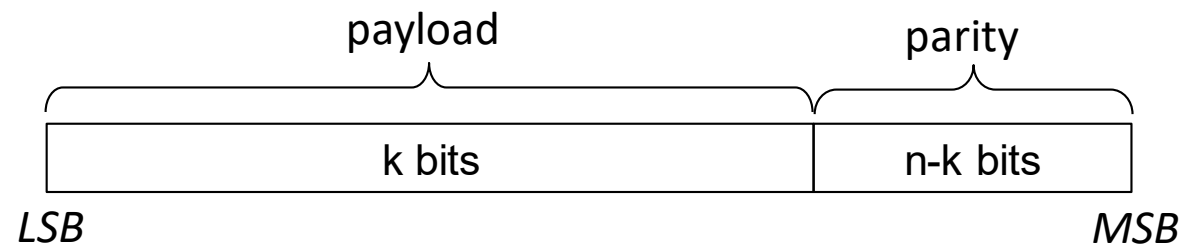
- Data mapping into FEC\_I payloads should be defined based on whether pre-encoding interleaver is used.
  - Based on convolutional interleaver design, mapping may be different. Existing proposals have given clear mapping methods.
  - If pre-encoding interleaver is used, FEC\_I payload should be aligned to symbol-pair/quartet boundary.



- If convolutional interleaver is excluded, the bit stream can be encoded directly.
- Padding bits, if needed, can be inserted before encoding as FEC\_I payloads.

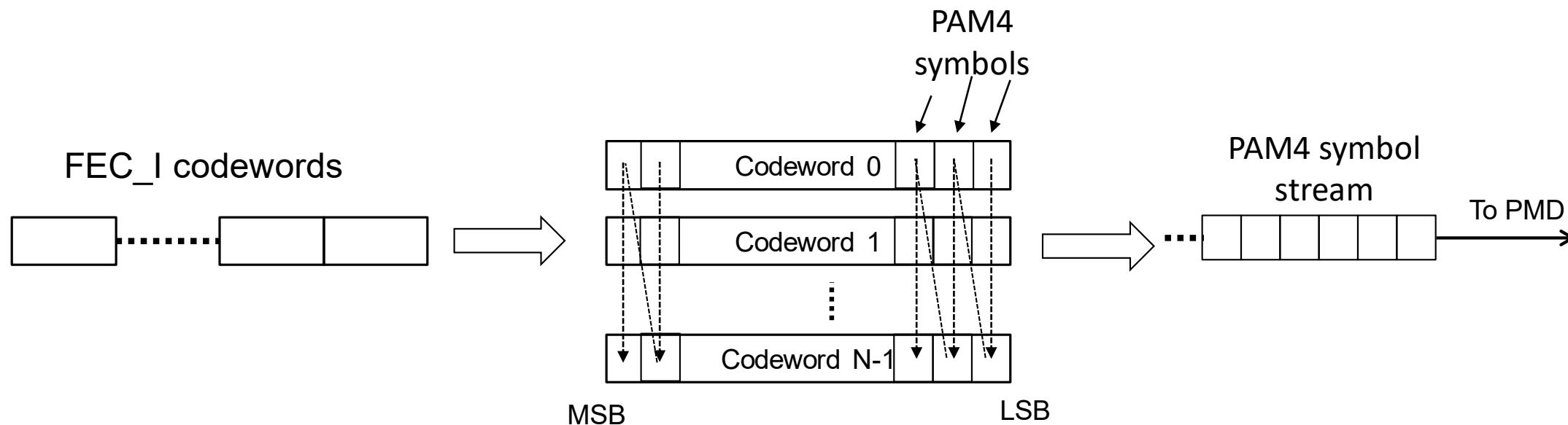
# Transmit Functions – FEC\_I Encode

- Different encoding methods have been proposed.
  - BCH polynomial as proposed in [he\\_3df\\_01\\_221005](#), and in [back up slide](#).
    - For 8-bit parity calculation, we could either use an 8<sup>th</sup> order polynomial as a primitive code, or use a 7<sup>th</sup> order poly times a (x+1) term as an extended code.
  - The XOR(MSB/LSB) method as proposed in [bliss\\_3df\\_01b\\_2211](#).
  - The Hamming generation matrix with XOR(MSB/LSB) as proposed in [farhood\\_3dj\\_01a\\_230206](#).
    - As proposed, there is not enough information for implementation.



# Transmit Functions – Post-encoding PAM4 symbol interleaver

- The PAM4 symbol interleaver (aka channel interleaver) can help light bursts on PMD.
  - Simulation result has been provided in back up [slide #27](#).
  - It can be deleted if later determined to be unnecessary based on optical track discussions on 200G/lane IMDD PMDs.
  - If not required, this function can be deleted and FEC\_I codewords are directly mapped to PAM4 symbols.



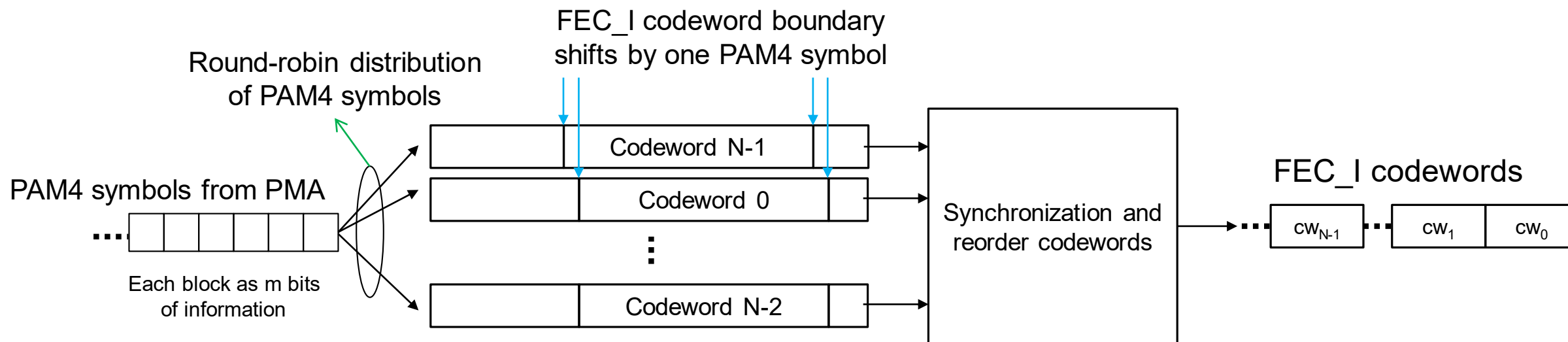
# Receive Functions – Soft information signaling

- Each PAM4 symbol is sampled into an implementation dependent format, with more than 2 bits of resolution for each PAM4 unit interval.
- Each sample is transferred to the FEC\_I sublayer through the PMA service interface.
  - Soft-decoding is required to achieve the PMD BER threshold.
  - Implementation can have the freedom to reduce the sample resolution or disable the soft-decoding to save power and latency, if it finds the BER is low enough.



# Receive Functions – pre-decoding de-interleaving and FEC\_I sync

- PAM4 de-interleaving can be performed arbitrarily, leaving the synchronization and reorder function to find the FEC\_I codeword boundaries and orders.
- Each row can use self-sync method as shown in [slide #26](#).
  - After each row of codewords are synchronized, the row where the boundary shifts one symbol ahead is the leading codeword for each group of N interleaved codewords.
- Synchronization can also be obtained by using alignment markers when padding is used.



PAM4 symbol de-interleave to N lanes of codeword streams.  
The order of codewords is intentionally shown out of order.

# Receive Functions – FEC\_I decode

- Decoding of FEC\_I is implementation dependent.
  - Using soft-decision or hard-decision is also implementation dependent and does not affect interoperation, but will result different BER thresholds.
  - BER thresholds shall be given explicitly with AUI BER taken into account. [Slide #25](#) in back up gives an example.

# Receive Functions – FEC\_I demapping

- Once decoded, the demapper restores the FEC\_I payload data into multiple branches for the convolutional de-interleaver.
- It is the reverse function of FEC\_I mapping.
  - Paddings, if used, can be removed here.

# Receive Functions – de-interleaver

- The convolutional de-interleaver shall perform the reverse function of the interleaver and produces data sequence as it was sent out of the BASE-R PMA.
- When the pre-encoding interleaver (convolutional interleaver) is excluded, the de-interleaver is also excluded.
- The synchronized FEC\_I codewords can guarantee a successful de-interleaving.

# FEC\_I Degrade Monitoring

- Counters can be used to monitor the codeword error ratio of FEC\_I for a given period of time.
  - Detailed usage can be further discussed.
- The propagation of FEC\_I degrade signals is implementation dependent.

# Summary

- This presentation illustrates the concatenated FEC may be fit into the 802.3 architecture.
- A complete baseline should include all transmit and receive functions.
- Leveraging the symbol-pair muxing PMA work may simplify the FEC\_I sublayer.

Thank you

# Back up slides



# PMD BER Threshold Considering AUI

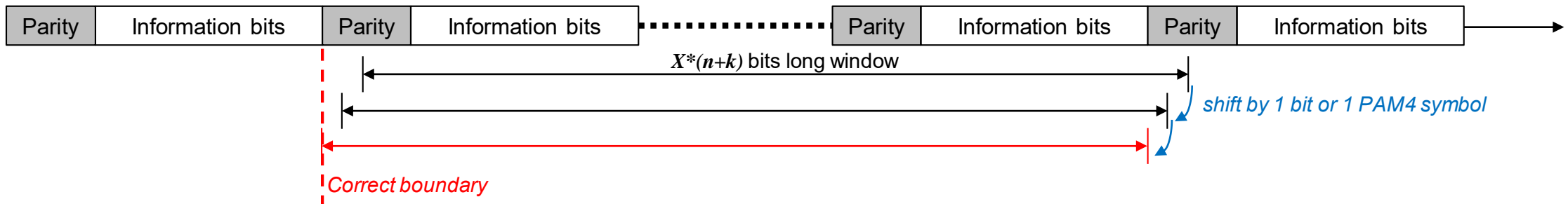
- Up to 2 segments of AUI on each side, not including MII Extenders, shall be supported.
- The combined effect of  $FEC_I$  and  $FEC_O$  results in the target frame loss ratio (FLR) for the PHY.
  - AUI BER threshold will affect the PMD BER allowed.
  - BER threshold listed below are updated data based on [he\\_3dj\\_01a\\_230206.pdf](#) and [he\\_3df\\_01\\_2211.pdf](#).

AUI BER (each segment)	PMD (w/ Convo. Int.)	PMD (w/o Convo. Int.)
1E-5	4.4E-3*	3.1E-3*
5E-5	3.5E-3*	2.4E-3*

\*Assuming the error statistics are sufficiently random. If the error statistics are not sufficiently random, the BER allowed shall be lower.

# Receive Functions – FEC\_I self-sync

- Follows Firecode methodology.
- Steps:
  1. **Search and Test:** Check  $N$  codewords, see if at least  $n$  of them are correct.
    - More preferably, we can try all possible positions, check  $N$  codewords for each position, and pick the position that has the most correct codewords. This may require less iterations.
  2. **Validate:** See in the following  $P$  codewords, if at least  $p$  codewords are also good.
    - If so, sync established. If not, go back to step 1.
    - If the number  $N$  in step 1 is large enough, step 2 may not be needed.
  3. **Monitor and Drop:** When there are  $m$  codewords with errors in the following  $M$  codewords.
    - Same methodology as hi\_ser.



# Effect of PAM4 Symbol Interleaver

- Following table lists BER threshold for BCH(144,136) with 8:1 post-encoding PAM4 symbol interleaver.
- The latency of 8:1 PAM4 interleaver is about ~5ns. The FEC\_I decoding latency is about ~10ns.

AUI (Fixed total BER)		Optical PMD					Coding Gain Improvement, dBe
"a"	4x AUI Total BER	1-tap DFE value <sup>b</sup>	w/ 8:1 PAM4 symbol interleaver		w/o 8:1 PAM4 symbol interleaver		
			SNR, dBe	BER <sup>c</sup>	SNR, dBe	BER <sup>c</sup>	
0.5	4E-5 (4x1E-5)	--	14.99	4.50E-03	14.99	4.50E-03	--
		0.28	15.15	4.38E-03	15.31	3.81E-03	0.16
		0.5	15.93	3.07E-03	16.52	1.64E-03	0.59
0.75 <sup>a</sup>	4E-5 (4x1E-5)	--	15.01	4.43E-03	15.01	4.43E-03	--
		0.28	15.16	4.34E-03	15.33	3.75E-03	0.17
		0.5	15.94	3.04E-03	16.53	1.62E-03	0.59
0.5	2E-4 (4x5E-5)	--	15.16	3.93E-03	15.16	3.93E-03	--
		0.28	15.30	3.85E-03	15.49	3.25E-03	0.19
		0.5	16.08	2.64E-03	16.78	1.21E-03	0.70
0.75 <sup>a</sup>	2E-4 (4x5E-5)	--	15.27	3.55E-03	15.27	3.55E-03	--
		0.28	15.41	3.49E-03	15.61	2.91E-03	0.20
		0.5	16.19	2.35E-03	16.97	9.63E-04	0.78

- Precoding is turned on.
- 1-tap DFE is used to simulate error propagation instead of using error propagation probability "a" value. Tap value of 0.28 is equivalent to a = 0.1, and tap value of 0.5 is equivalent to a = 0.375.
- The BER values includes additional errors due to bursts and the effect of precoding.