The Case for Concatenated Codes

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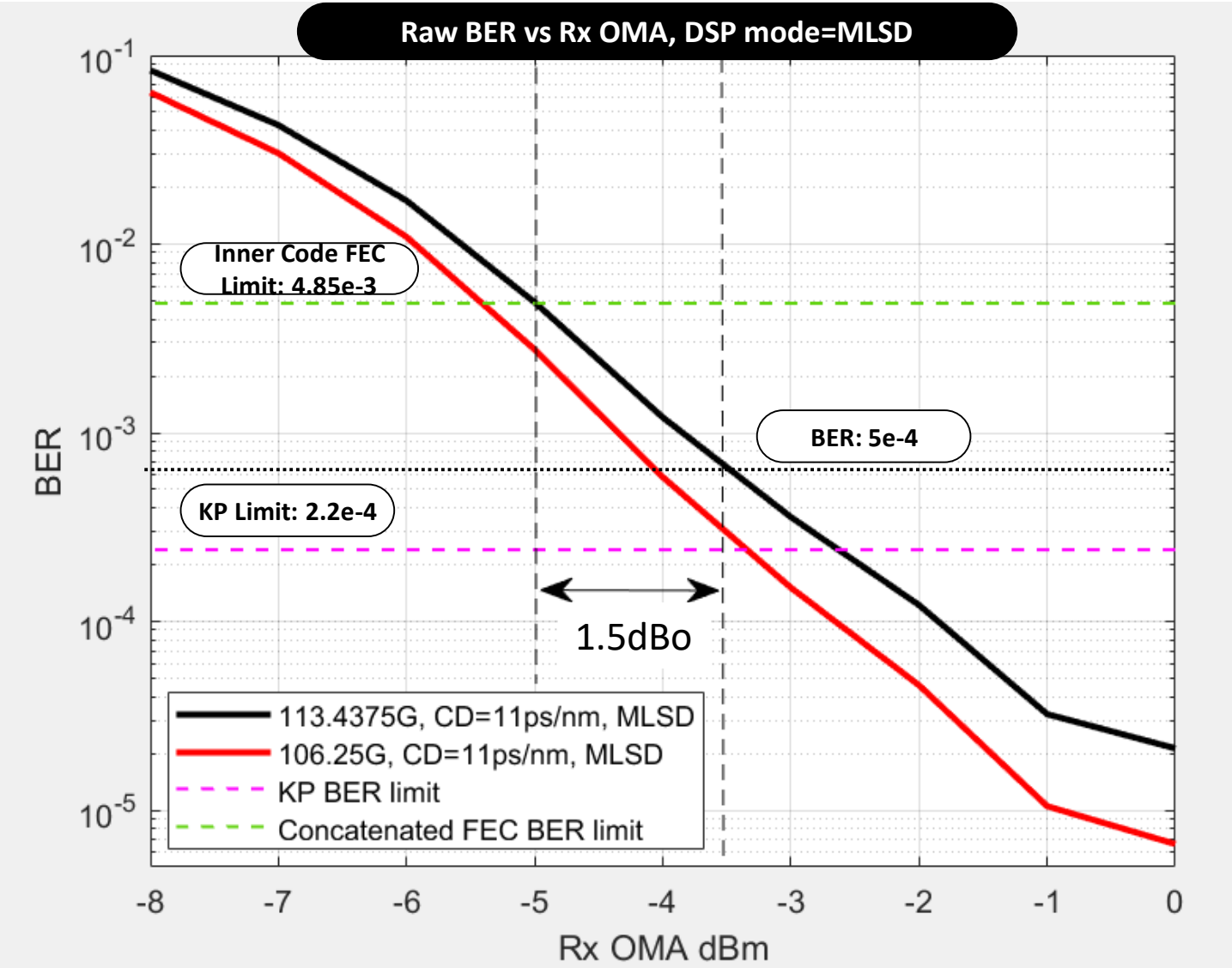
Introduction

- Simulations of FR4 systems
  - ‘KP4 only’ RS(544,514) @ 106.25GBaud/sec
  - With Hamming (128,120) at higher Baud rate
- Three independent teams simulating their own systems with independent estimates of both optical/electrical components
  - TX specification
  - Optical Modulator
  - Fiber specification
  - PIN responsivity
  - TIA noise
  - Limited bandwidths of components including components of TOSA and ROSA
  - Receiver architecture and parameterization

Simulation1 parameters

Parameter	FR4
Reach (meter)	2,000
Max. Fiber Loss (dB)	4.0
MPI penalty (dB)	0.3
Min TX OMA (dBm)	1.1
Max TX OMA	4.2dBm
ER	4.5
CD Max/Min (ps/nm)	{6.6,-11.7}
Rx Sensitivity (dBm)	-3.2

Simulation 1: RX OMA Vs BER sensitivity curve



- Baud rate: 113.4375Gbaud
- TX and RX parameters
  - TX BW=50GHz
  - TX RJ=125fs
  - ADC T&H BW = 50GHz
  - RX RJ=110fs, RX UDJ=400fs p2p.
  - ADC Physical number of bits = 7
- TIA:
  - O-E BW: 48GHz
  - NEP = 16pA/sq(Hz)
  - Effective responsivity: 0.45 A/W

SUMMARY:

- **RX BER: 5e-4 can be achieved with RX models with RX sensitivity target with 11ps/nm CD**
- **Concatenated FEC like Hamming (128,120) can enable this solution with better than one decade of BER margin**
- **Net coding gain including loss to higher Baud rate = 1.5dBo**

Simulation 2: Optical simulation parameters for FR-4

FR4 case also no inner FEC, only KP4 FEC

Model link: Detailed block diagram with optical simulation parameters

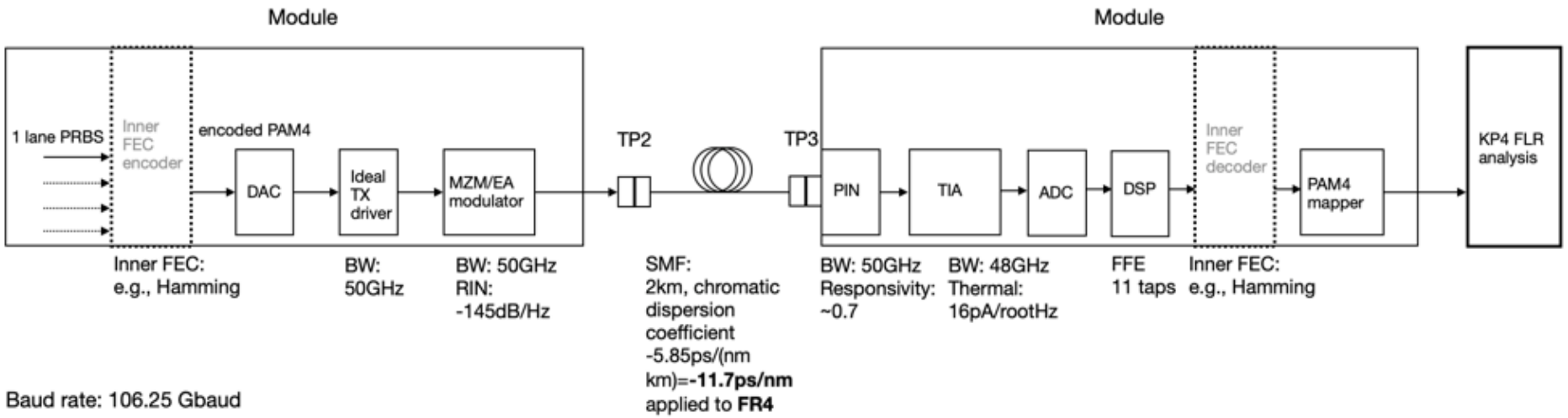
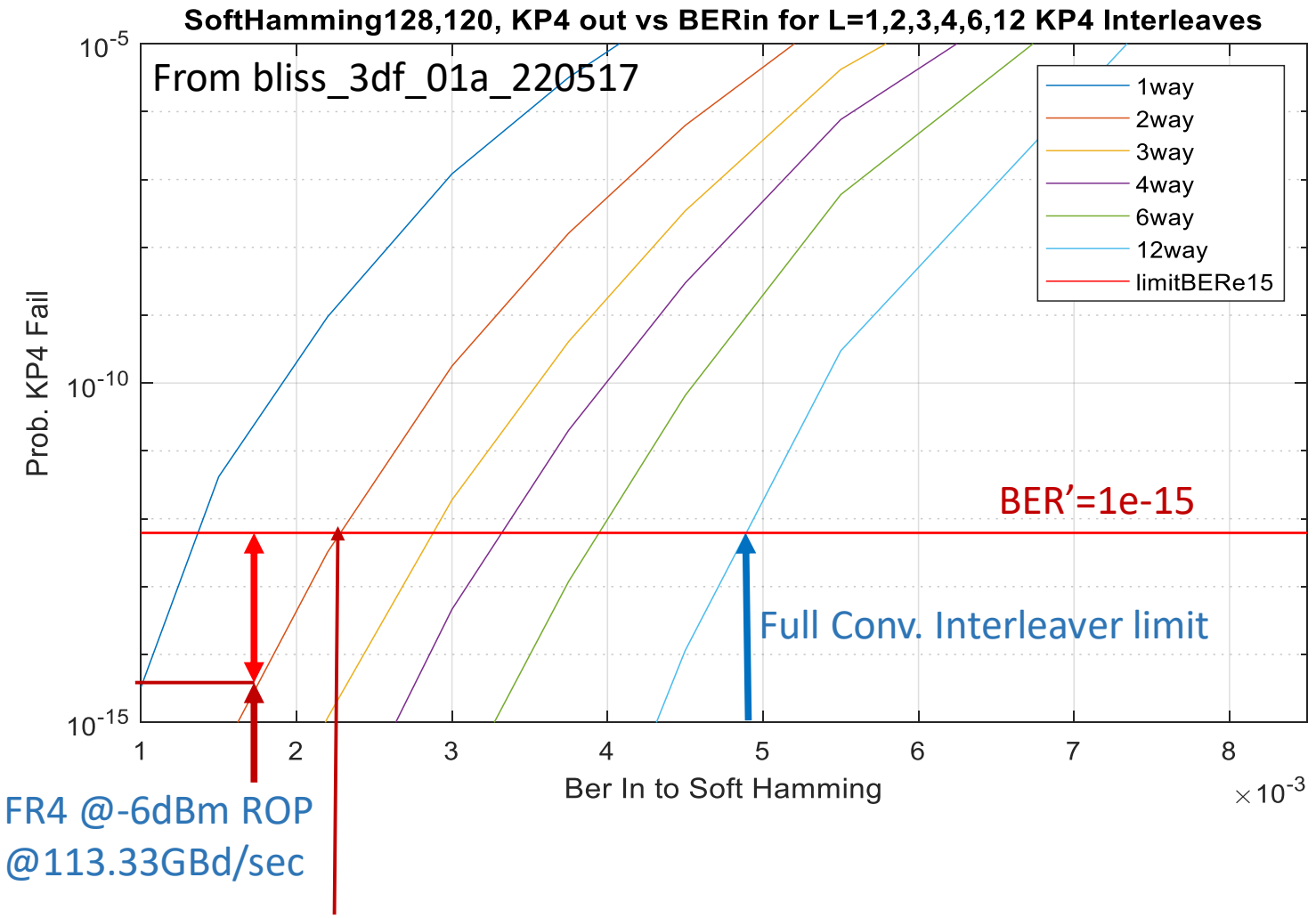


Table 2 Simulation Parameters

Baud rate KP4	106.25 Gbaud
O modulator BW	50 GHz
TIA BW	48 GHz
PD BW	Similar to TIA
RIN noise	-145 dB/Hz
ER	4 dB
TIA noise	16pA/root Hz
Responsivity	~0.45
ROP*	-6dBm

*OMA = -6.6dBm

Simulation 2: Concatenated code performance gain

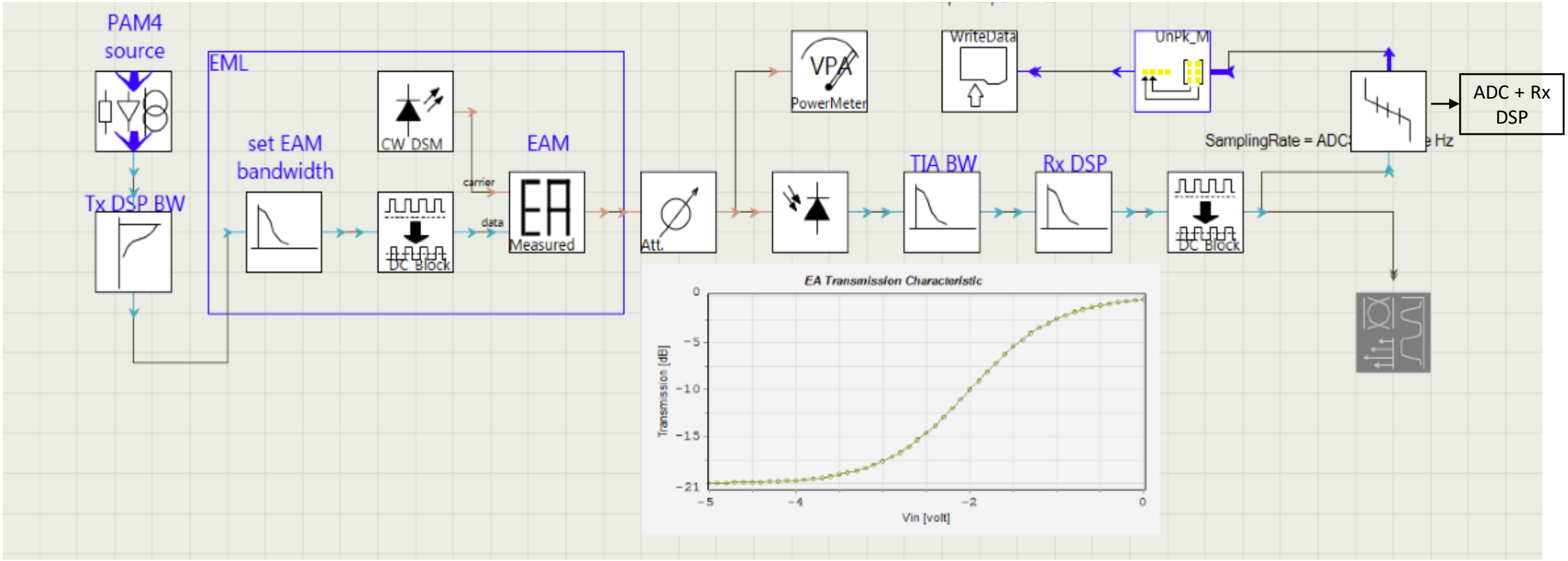


- Two Baud rates simulated, both at -6dBm ROP = -6.6dBm Rx OMA

Baud Rate simulated	106.25 G	113.33 G
BER raw	8.14e-4	1.70e-3
Code	KP4 RS(544,514)	+ Hamming (128,120)
Margin to FLR 1e-15	-0.7 dBo FAILS	+0.7 dBo WORKS

- KP4 (no Hamming) FAILS with 0.7dBo negative margin @106.25GBaud/sec
- With Hamming (128,120) @113.33 GBaud/sec has +0.7dBo margin

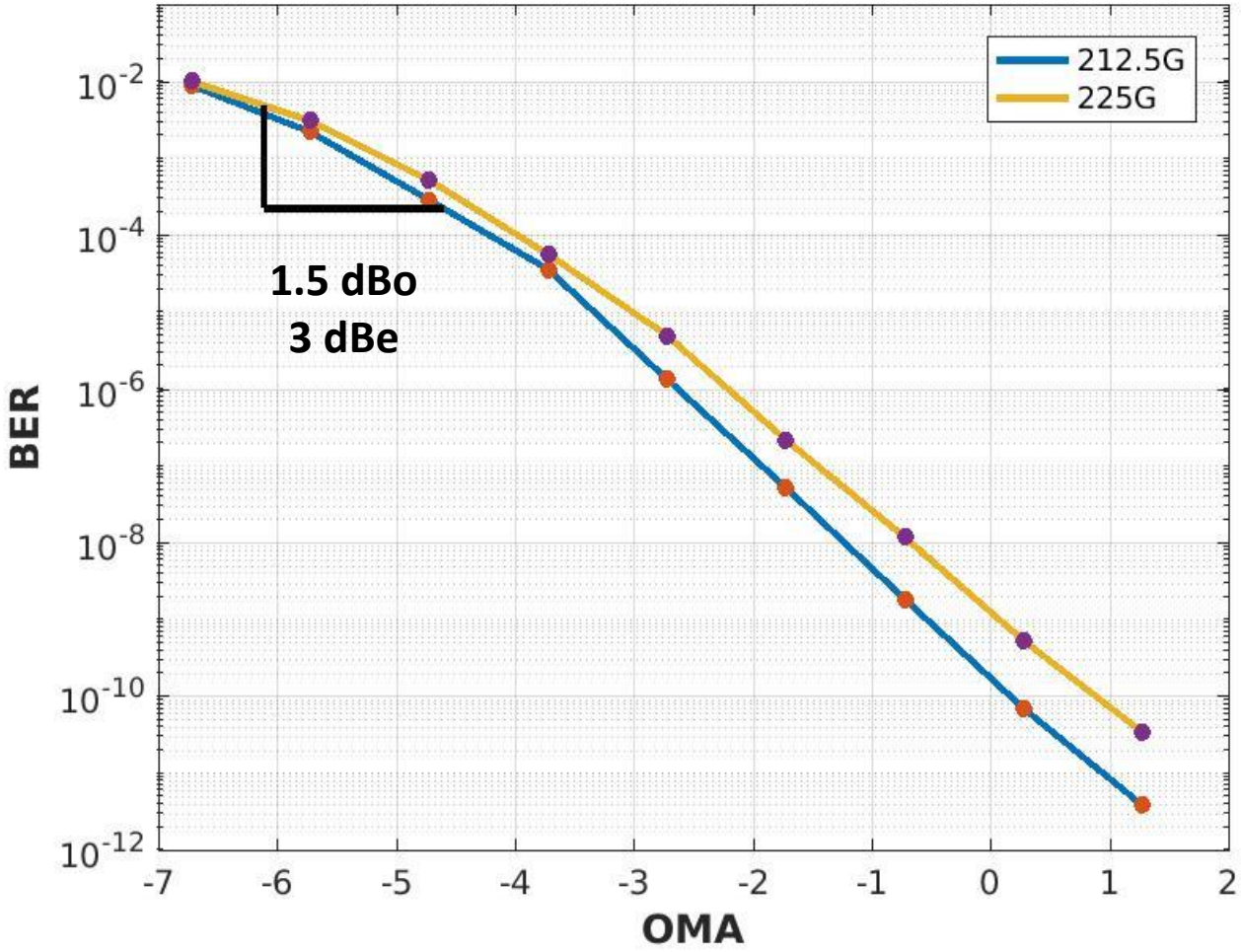
Simulation 3: Waveform Generation Topology

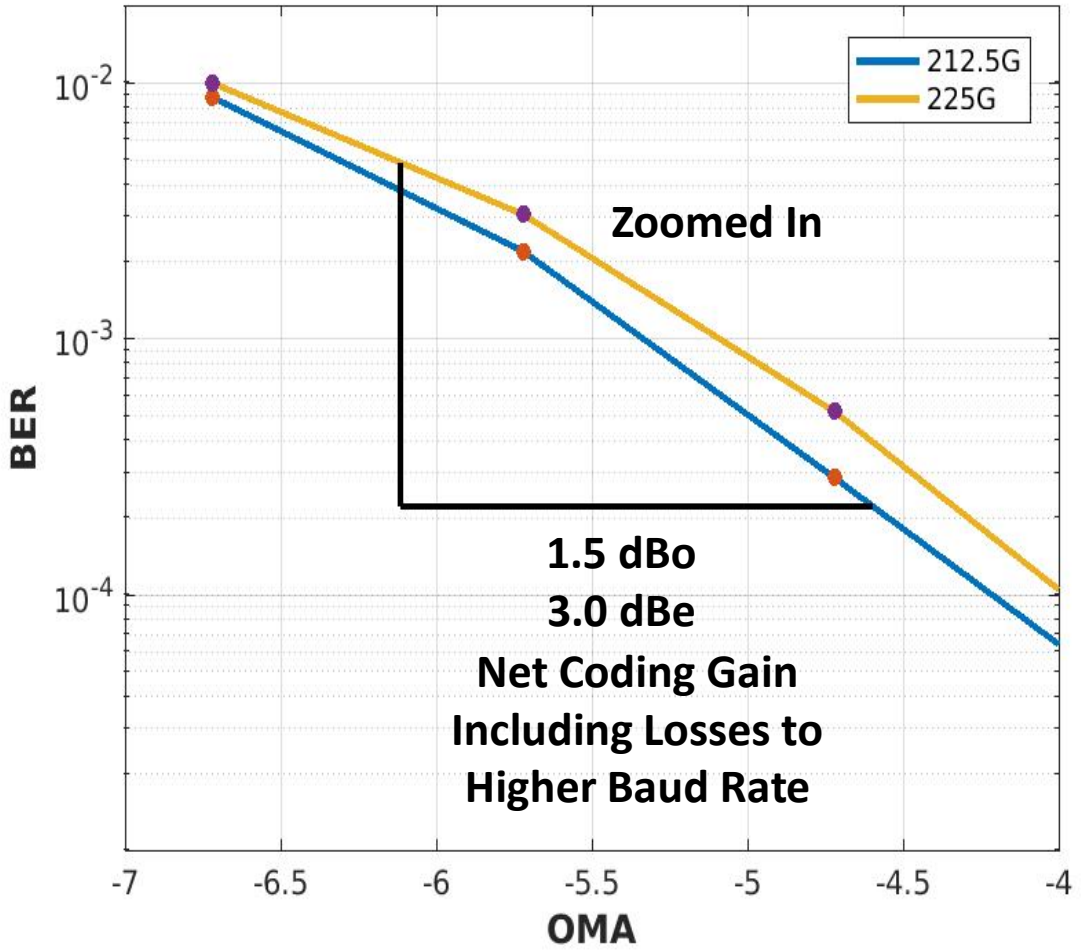


Simulation 3: Parameters

Parameter	Suggested value	Value	Comments
Baud-rate for Concatenated FEC	112.5Gbaud		
Baud-rate for Segmented FEC	106.25Gbaud		KP Only
TX DSP Bandwidth	50GHz		
TX DSP Filter type	BT4		
TX DSP RJ	125fs		
RX DSP Bandwidth	50GHz		
RX DSP RJ	110fs		
RX DSP DJ	400fs P2P		No TX DJ. All DJ modeled in RX
RX DSP ADC Physical bits	7 bits		
TIA Bandwidth	48GHz		
TIA NEP	16pA/rHz		
PD responsivity	0.45 A/W		
Optical modulator Bandwidth	50GHz		
Optical modulator filter type	RC		RC means Resistor/Capacitor
Reference DSP design	FFE_21+ DFE_2		

Simulation 3 Results: Pre-FEC BER vs OMA





Simulation conclusions

- Three independent simulations with realistic optical and electrical component parameters were run both at 106.25GBaud/sec, and at higher baud rate for the Hamming (128,120) code

- The Hamming code showed Net Coding Gains (after the loss to increased Baud rate) of 1.4 to 1.5 dBo
  - This is a >40% increase over the stand alone KP4 RS(544,514) raw coding gain

  - It's early in the component cycle to conclude exactly how much extra coding gain will be needed for different systems

- We can argue all we want but remember ***"If it looks like a duck, swims like a duck, and quacks like a duck, then it probably is a duck."***

Final thoughts on additional FEC margin

- **Additional FEC margin relaxes challenging transmitter and receiver requirements**
  - Optical/electrical parameters show KP4 struggles to close the link
  - Industry trends towards CMOS integrated drivers /TIA's stresses already challenging bandwidth specs
- **Numerous benefits of additional FEC Margin including risk mitigation**
  - Faster time to market
    - Adoption of a solution that provides extra margin facilitates use of early optics
  - Improved module yield
    - Performance hits due to module component variations absorbed into the enhanced FEC margin
    - Temperature, voltage variations absorbed into the additional FEC margin
    - Improved tolerance to SI issues
  - Lower module power and cost
    - Relaxed optical and analog specs lead to simpler development
    - Margin can be used to manage specs on TIA, SiP/EML, Driver bandwidth and TIA RIN
  - Allows operation at lower OMA
    - Provides extra margin to operate with higher mux/demux losses

SUMMARY: PREVENTING A POTENTIAL PROBLEM IS BETTER THAN FINDING A CURE LATER