Moving forward with FEC

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List of Supporters

- Shuang Yin, Google
- Reza Ekthfar, Amazon
- Lenin Patra, Marvell
- Arash Farhood, Marvell
- Drew Guckenberger, Maxlinear
- David Cassan, Alphawave
- Tony Chan, Alphawave
- Sridhar Ramesh, Maxlinear
- Will Bliss, Broadcom

Straw poll result interpretation

The primary issue that I think should be addressed with the baseline proposal in straw poll #5 is:

a.	AUI BER details	26
b.	1.6T support	9
c.	Convolutional interleaver	5
d.	Common FEC across the 200G/lane PMDs	27
e.	Latency	10
f.	FEC lane rate	6
g.	Other	4

- Desire for a common FEC approach
- Concern about AUI BER allocation
- Concerns about latency, support for 1.6T, and use of 25 Gb/s PCS lanes

To address these concerns, propose to...

- Adopt inner code for all optical PMDs listed in patra_3dj_01b_2303 slide 3
- Define the details of the convolutional interleaver at a later time
  - Bypass or tune parameters to trade-off between performance and latency as needed by each application
- Define the “FEC lanes” (e.g., 25 Gb/s PCS lanes or other) at a later time
- Define support for 1.6T at a later time
- Define AUI BER target at a later time
  - Adoption of inner code enables a higher (than 1e-5) AUI BER target
  - But the specific target needs to be based on AUI capabilities and acceptable allocation from the optical link budget
- It is very useful to adopt what we can agree upon in order to...
  - Focus future FEC discussions
  - Provide a fixed frame of reference for proposals impacted by FEC decision (AUI, PMD)
- **Many complex inter-relationships; decisions help the process converge!**

Straw poll

I would support patra_3dj_01a_2303 slides 6 to 8, 13, 14, and 20 to 23 as part of the FEC approach for

- 800GBASE-DR4, 800GBASE-DR4-2, 800GBASE-FR4
- 400GBASE-DR2, 400GBASE-DR2-2*
- 200GBASE-DR1, 200GBASE-FR1

with FEC lane rate, convolutional interleaver details, and 1.6T support to be determined later

* If an objective is adopted.