Impact of Burst Errors on Concatenated FEC scheme

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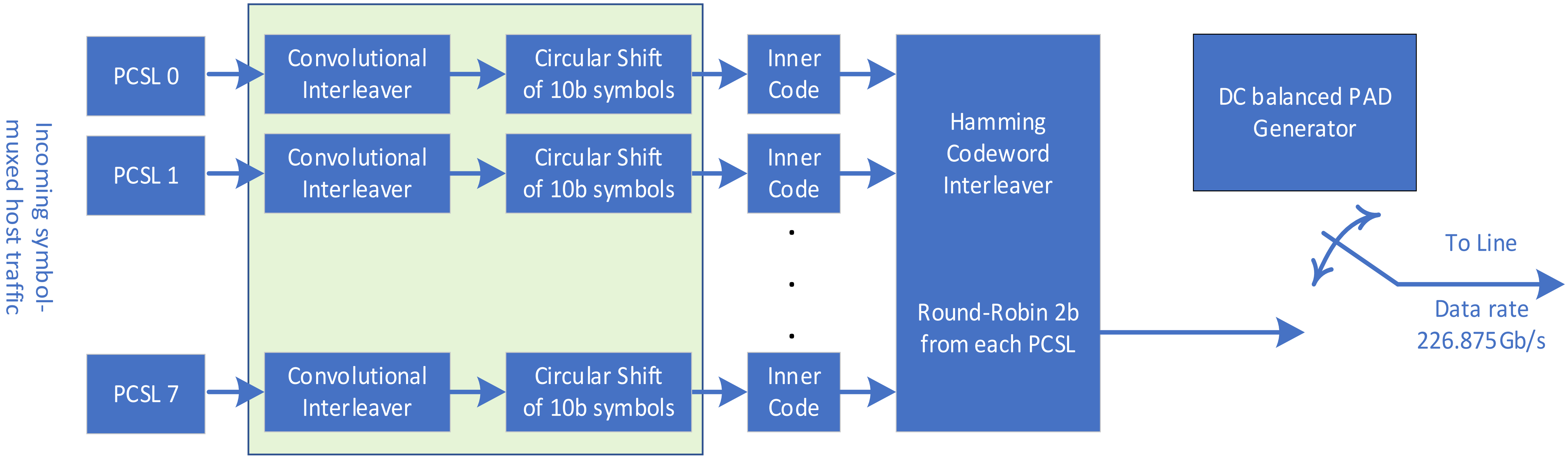
Outline

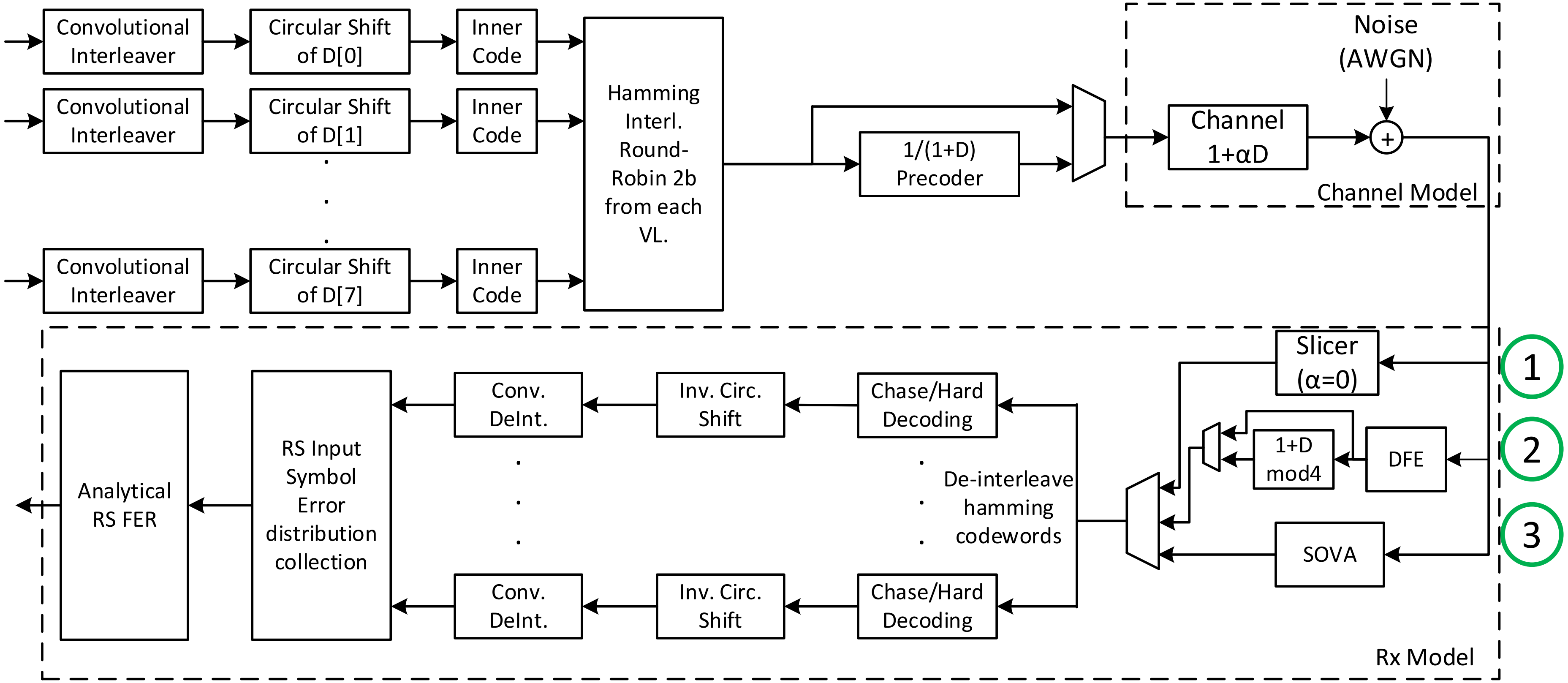
- Overview of the Concatenated FEC scheme
- Pseudo-Analytical Simulation Environment
- Optimizing burst tolerance
- Simulation results under different channel conditions
- Summary

TX Encoding Datapath with Inner Code (128,120)



PCSL re-order is not required. Lane order does not matter

Pseudo-Analytical Simulation Environment



- Representing various range of combined channel responses of interest, $0 \leq \alpha \leq 1$
- Representing various range of Rx implementations, from memoryless detection (for $\alpha = 0{,}1$), to DFE to full soft decoding using Soft Output Viterbi Algorithm (SOVA)*

* J. Hagenauer, A Viterbi Algorithm with Soft-Decision Outputs and its Applications, IEEE Global Telecom. Conf. 1989

Pseudo-Analytical Simulation Environment

- The RS symbol error distribution is collected from simulations as set L = $\{E_0, E_1, E_2, \ldots, E_M\}$

E_j is an error event of RS symbol span/burst duration $S(E_j)$ and number of errors $N(E_j)$
(E_0 is a special “zero” event with $S(E_0)=1$ and $N(E_0)=0$)

Using the list L and associated probabilities $P(E_j)$, spans $S(E_j)$, and number RS symbol errors $N(E_j)$, solve a recursive equation for **π(n,i)** representing the probability of i or more RS symbol errors in a block size n. Using Bayes’ rule, π(n,i) follows a simple recursive formula:

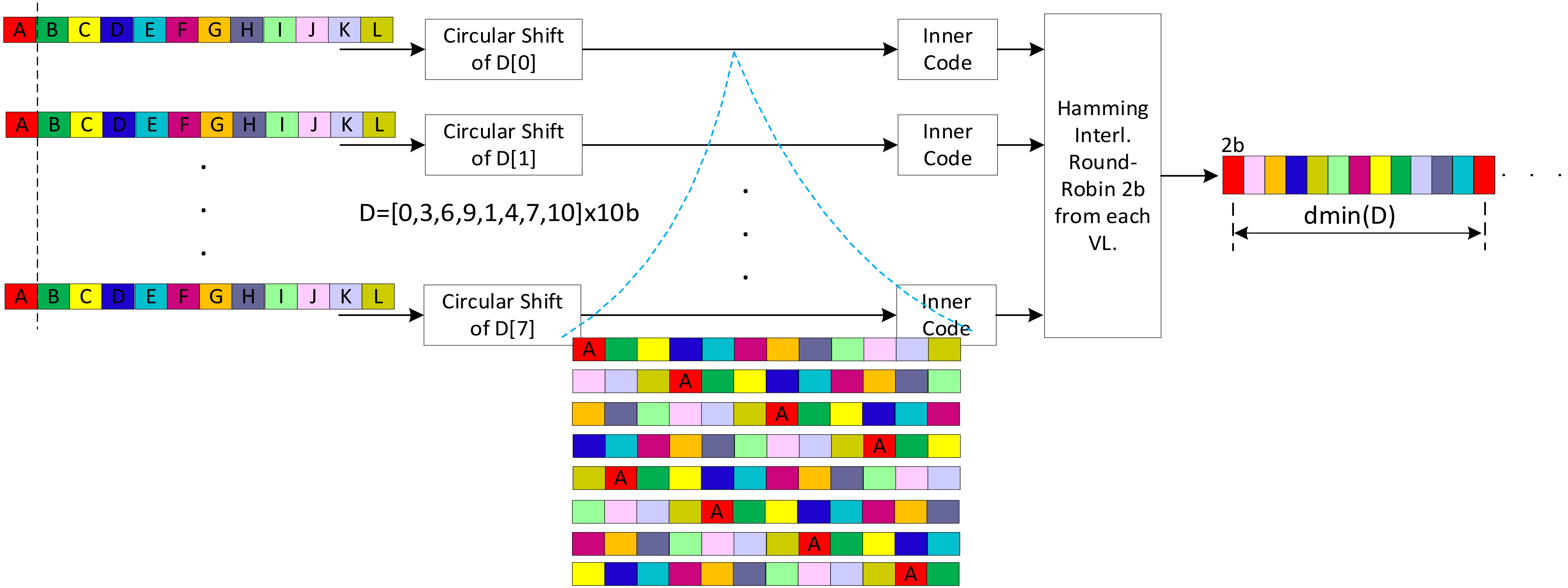
$$\boxed{\pi(n,i) = \sum_j P(E_j)\, \pi(n-S(E_j), i-N(E_j))}$$

With initial conditions: $\pi(1,0) = 1, \pi(1,1) = \sum_{j\neq 0} P(E_j), \pi(1,2{:}\mathrm{end}) = 0$

- Chase Decoding* Parameters in these sims: number of selected least reliable bits =6, number of maximum bit flips is 3 per codeword.

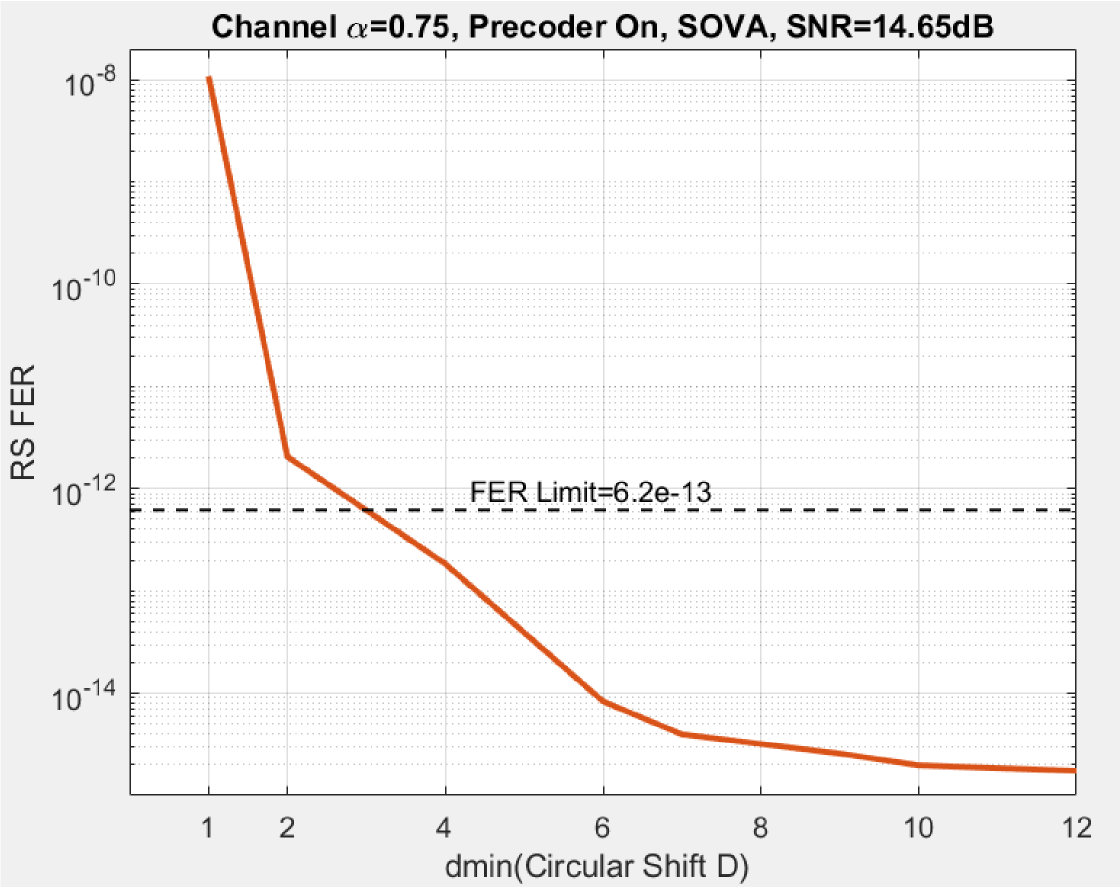
*Pyndiah, R. Near-optimum decoding of product codes: Block turbo codes. *IEEE Trans. Commun.* 1998, *46*, 1003–1010

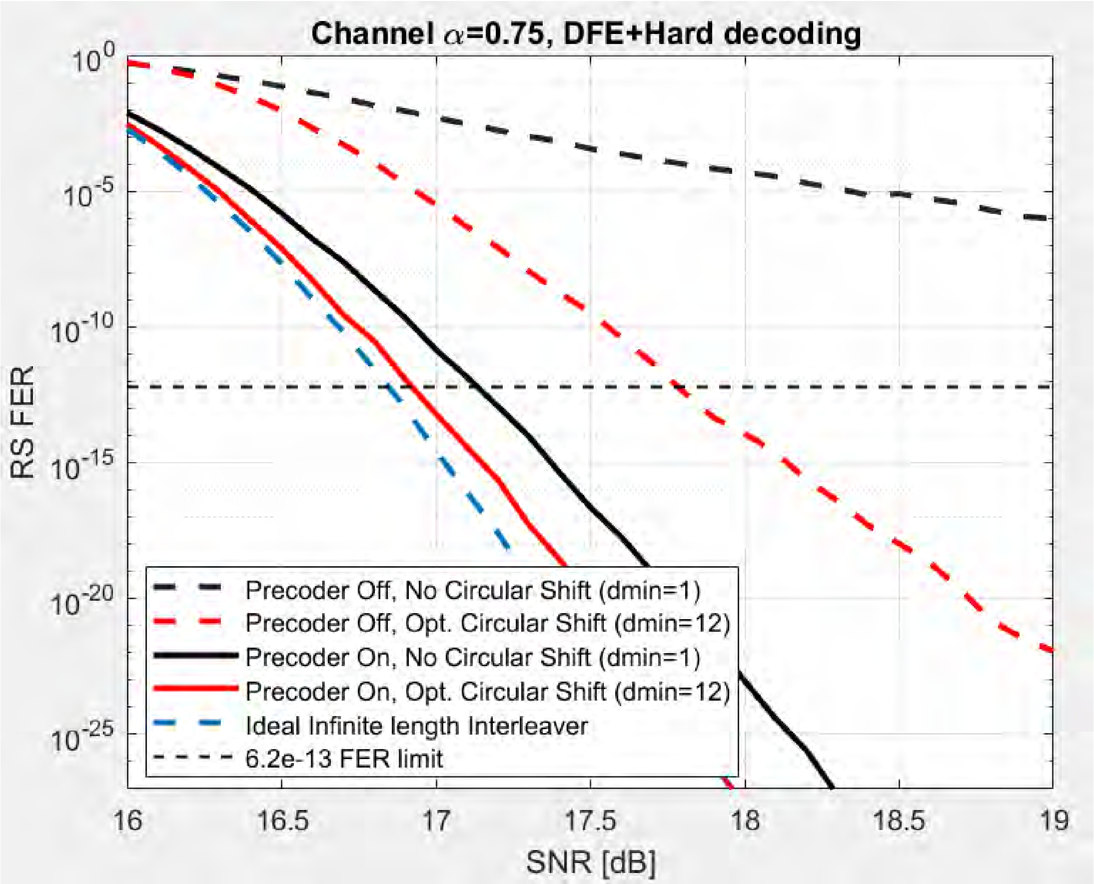
Functionality of the Circular Shift Block



- Goal is to improve burst error tolerance of the concatenated code
- Circular Shift block can be visualized as a simple rewiring of the 10b symbols (120b input bus)
- It maximizes the distance in Bauds between transmitted PAM4 symbols from two different RS symbols in the same KP Codeword

Effect of the Circular Shift Block

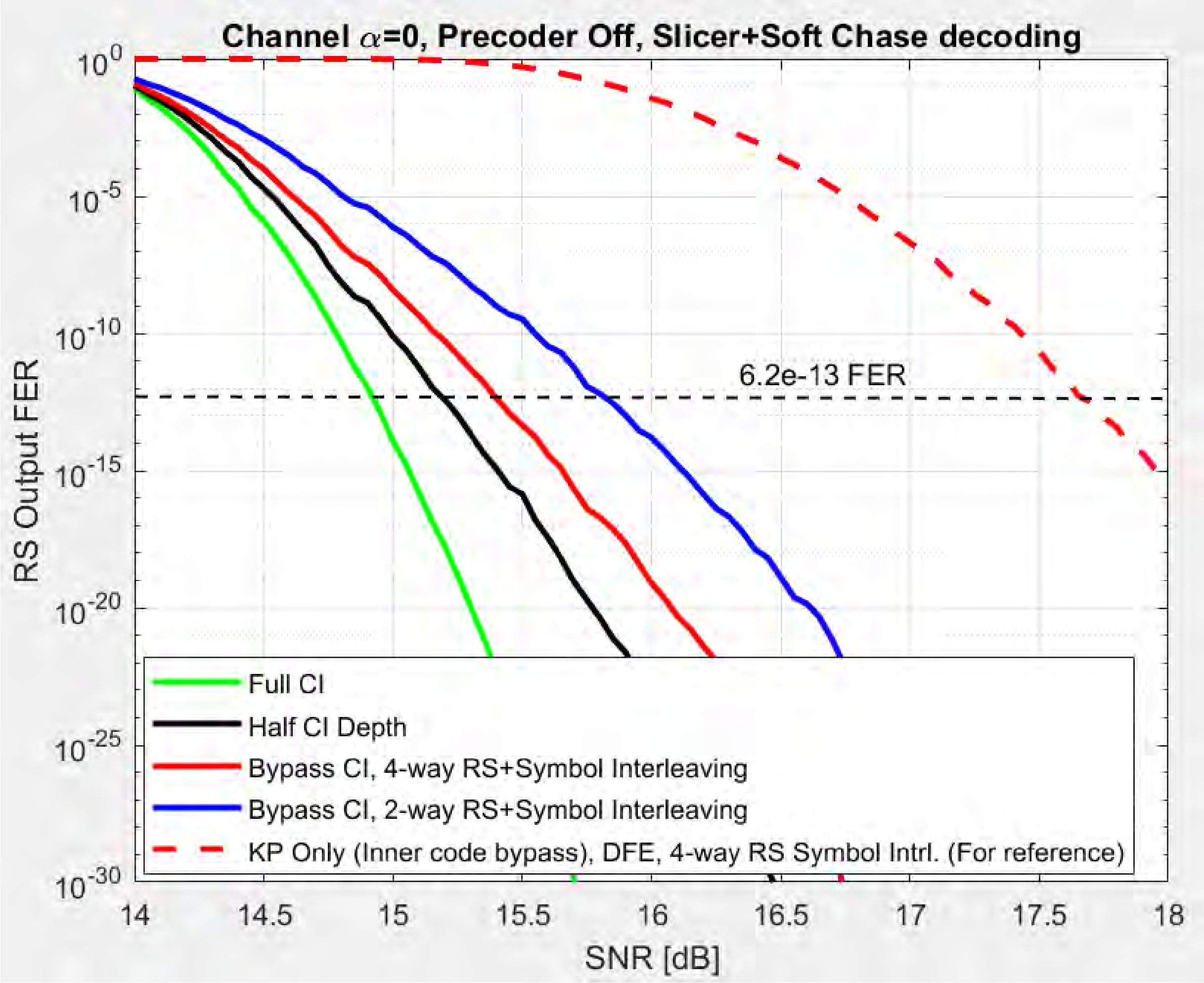




- Properly optimizing circular shifts (D), yields big improvement in the concatenated code burst tolerance at no/negligible HW cost in terms of latency or power consumption (pure rewiring)
- With DFE burst errors and 1/(1+D) precoding, the 8-way Hamming interleaving with Cyclic Shift D=[0,3,6,9,1,4,7,10], yields ~0.05dB SNR penalty compared to an ideal/infinite depth interleaver

Slicer Based Rx with Soft Decoding ($\alpha = 0$)

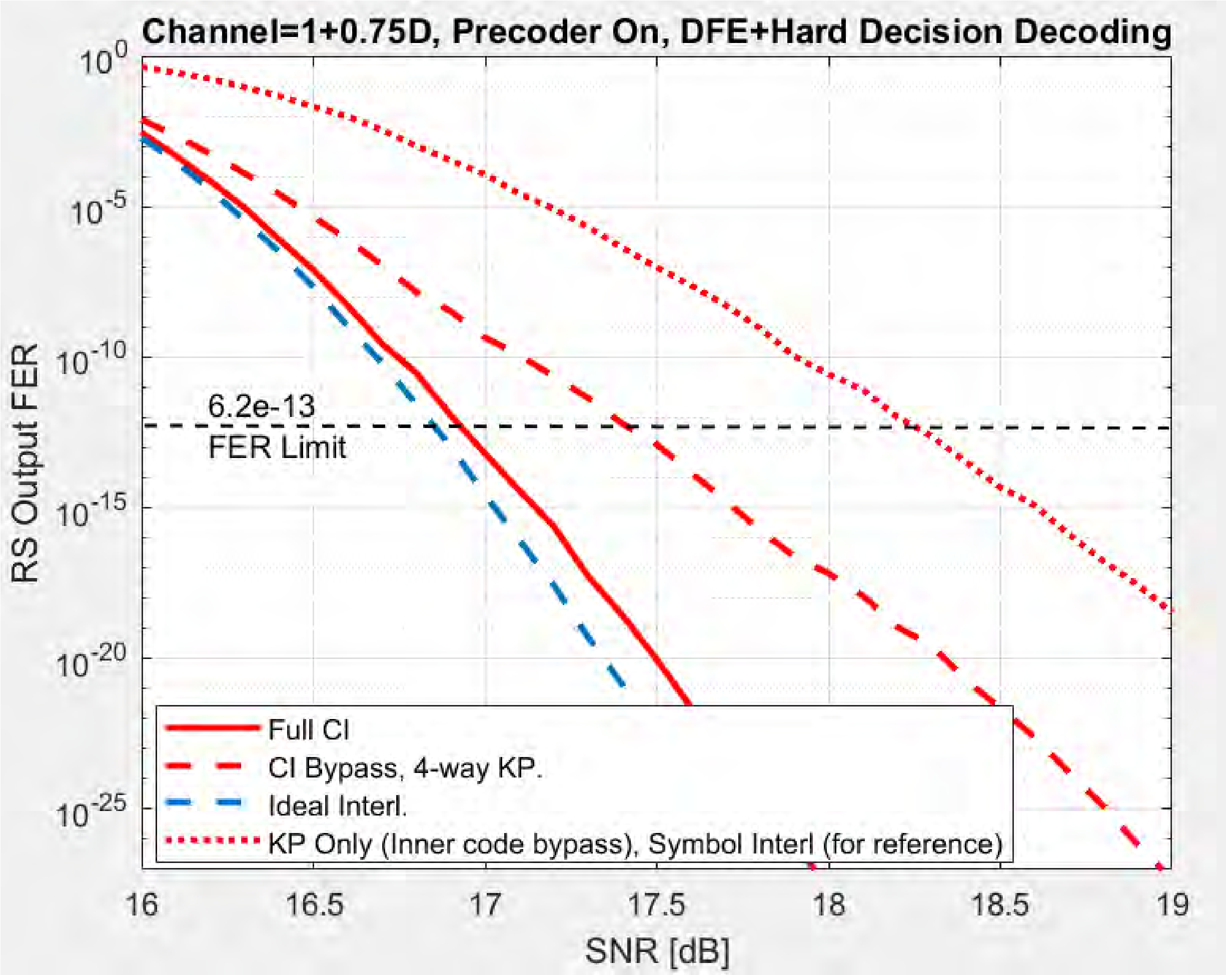
*No bursts, for reference only



- CI bypass yields SNR penalty in 0.5-0.85dB range compared to full depth CI
- Cutting CI depth by half only yields 0.25dB SNR penalty
- Bypassing CI still yields positive Net Coding Gain of >=1.6dB

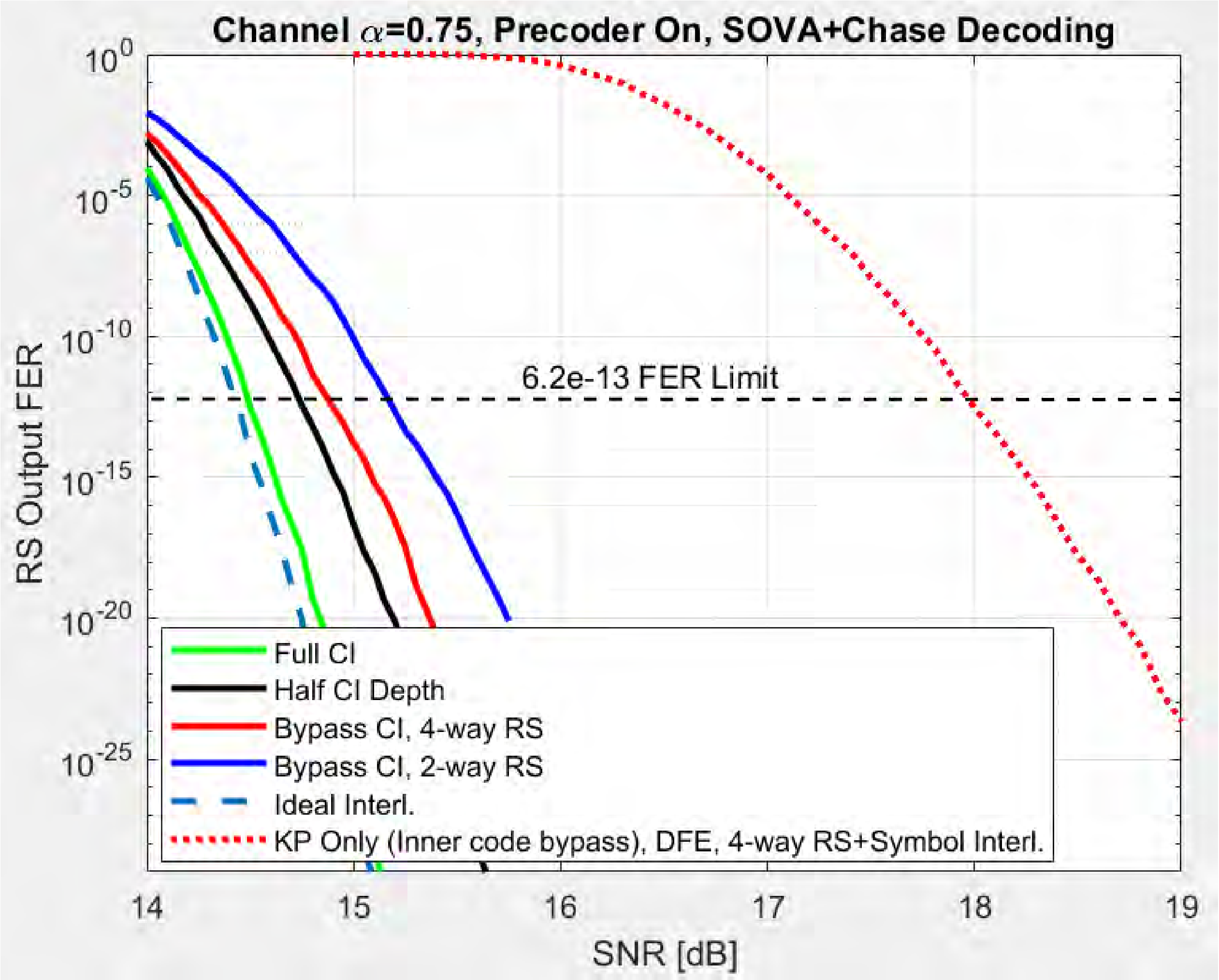
	Req. SNR for 6.2e-13 FER	Penalty wrst Full CI	Net Coding gain vs (HD DFE)	Req. Inner code Input BER
Full CI	14.9	0	2.47	4.85E-03
1/2 CI	15.15	0.25	2.22	3.90E-03
No CI, 4-way KP	15.4	0.5	1.97	3.30E-03
No CI, 2-way KP	15.75	0.85	1.62	2.40E-03
KP Only, 4-way KP+Symbol Int.	17.65	2.75	0	2.40E-04

DFE Based Rx with Hard Decoding



- Concatenated FEC Interleaving proposal yields close to ideal interleaving, i.e. ~0.05dB SNR penalty
- Bypassing Convolutional Interleaver, i.e. low latency mode, yields 0.5dB SNR penalty
- Bypassing Convolutional Interleaver, even with DFE and hard decoding of inner code, yields a positive coding gain of 0.8dB

SOVA Based Rx with Soft Decoding ($\alpha = 0.75$)



- Proposed Concatenated code Interleaving is within 0.05dB of ideal Interleaving
- CI bypass yields SNR penalty in 0.35-0.7dB range compared to full depth CI
- Bypassing CI still yields a big positive Net Coding Gain of >=2.5dB

	Req. SNR for 6.2e-13 FER	Penalty wrst Full CI	Net Coding gain vs (HD DFE)	Req. Inner code Input BER
Full CI	14.5	0	3.17	4.85E-03
1/2 CI	14.75	0.25	2.92	3.60E-03
No CI, 4-way KP	14.85	0.35	2.82	3.00E-03
No CI, 2-way KP	15.2	0.7	2.47	2.20E-03
KP Only, 4-way KP+Symbol Int.	17.95	3.45	0	

Summary

- In this presentation we introduced a simple, yet practical statistical system model to assess the effect of burst errors on the Concatenated FEC scheme

- This presentation shows the robust performance of the Concatenated FEC scheme in presence of bursts as well as AWGN error models

- The analysis also shows, the small to moderate coding gain penalty associated with variable depth of Convolutional Interleaver for applications that can tradeoff coding gain and latency