Supporting Channel Analysis for a Backplane Objective

Nathan Tracy
Megha Shanbhag

TE Connectivity
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EVERY CONNECTION COUNTS

Contributors

Regee Petaja, Broadcom

Adam Healey, Broadcom

Vivek Telang, Broadcom

Acknowledgements

Jim Weaver, Arista

Jason Chan, Arista

Overview

A preliminary investigation into passive copper backplane channels, based on a mix of conventional and unconventional architecture concepts, is presented to help support technical feasibility, enable multi-party analysis and provide guidance to P802.3dj discussions.

Development work is on-going, updates and refinements are anticipated in future contributions.

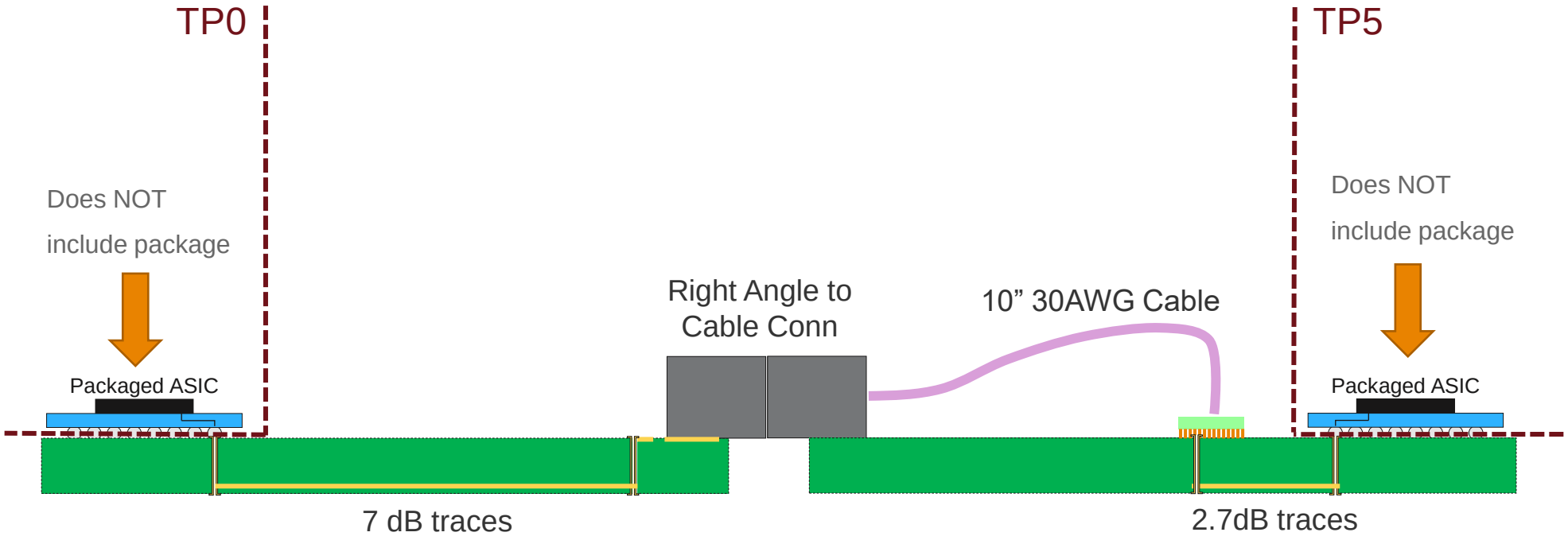
This is not intended to be a final position or a proposal on backplane channel performance.

The intent of this presentation is to provide technical support and directional input for adding a backplane objective and promote consensus among the participants.

Description

- Simulation for 200G KR channel using backplane concept connector and cabled backplane assembly with various host architecture options
- Includes BGA escape model provided by Regee Petaja of Broadcom
- Does NOT include silicon package
- Current view of backplane channel performance in various host implementations
- What this presentation is NOT:
  - Modulation proposal
  - Channel or Cable Assembly loss proposal
  - A specific host architecture proposal;
    - comparative performance options are presented, i.e., traces vs. cabled host to “near ASIC” vs. co-package copper
  - Asymmetric architecture proposal (managed deployment)

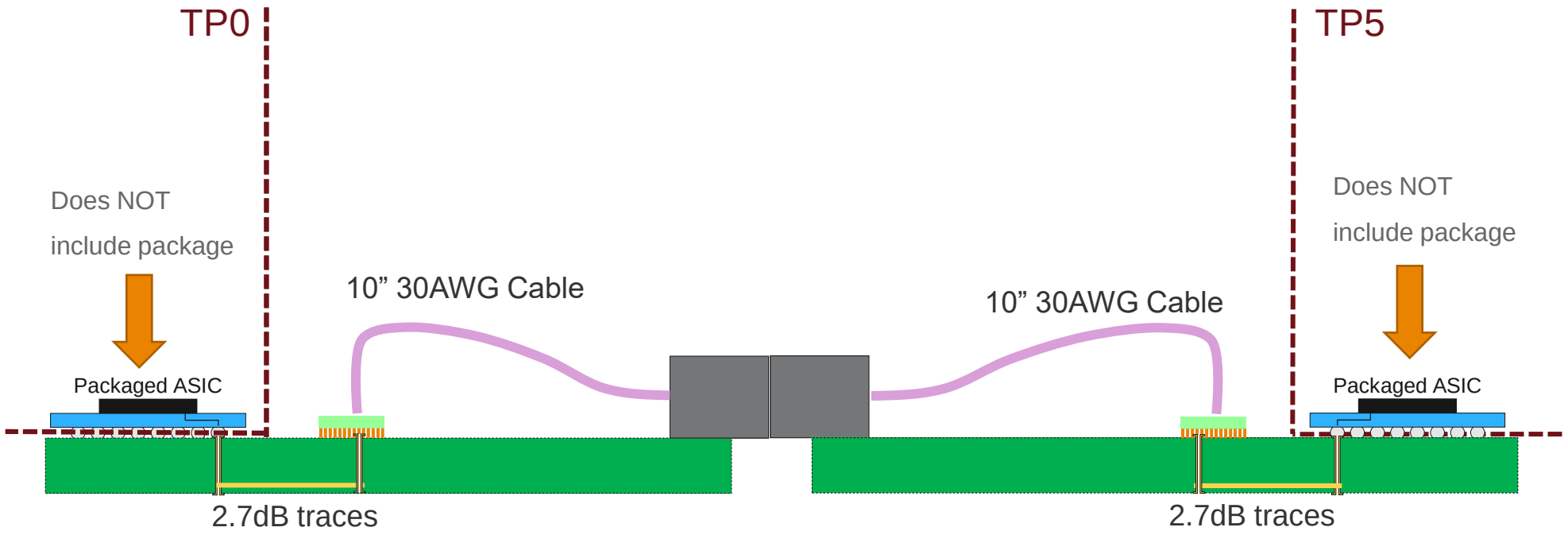
KR 1 (Switch Fabric PCB Routing)



Channel includes,

- Right Angle backplane SMT connector mated to cabled backplane connector
- SMT footprint includes via transition and breakout
- Cable Termination to cabled backplane connector
- 10”, 30AWG Cable
- Cable termination to near chip connector
- Near chip connector
- Near chip transition via and breakout traces
- BGA footprint + breakout
- 7dB traces from RA connector to BGA
- 2.7dB traces from near chip connector to BGA

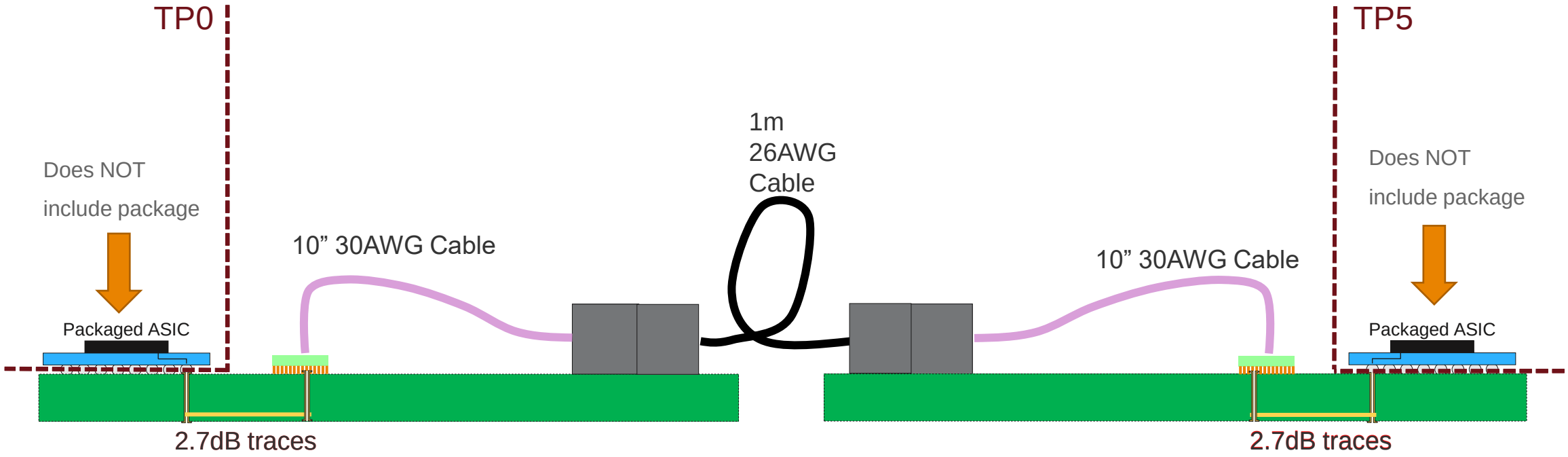
KR 2 (Medium Chassis, Near Chip Cables)



Channel includes at each end,

- Cabled backplane connector
- Cable Termination to cabled backplane connector
- 10”, 30AWG Cable
- Cable termination to near chip connector
- Near chip connector
- Near chip transition via and breakout traces
- BGA footprint + breakout
- 2.7dB traces from near chip connector to BGA

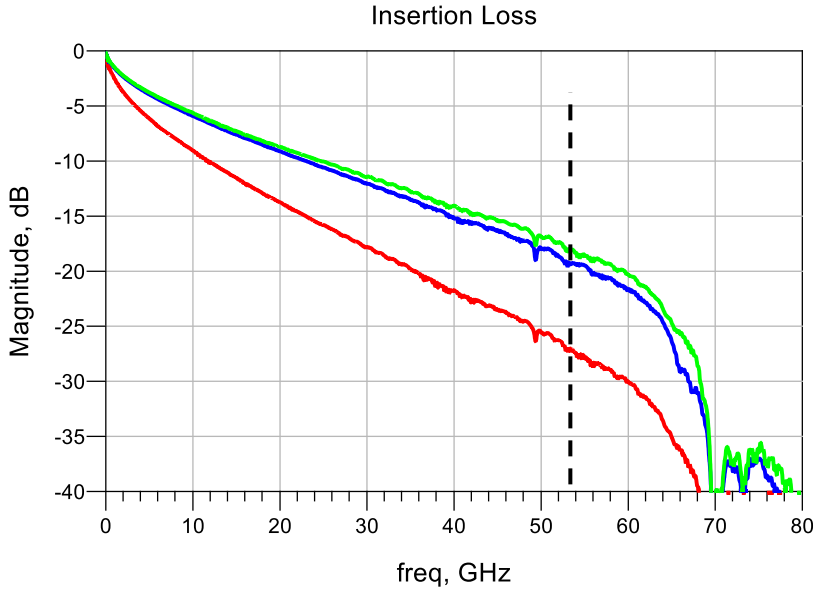
KR 3 (Large Chassis, Cabled Backplane, Near Chip Cables)

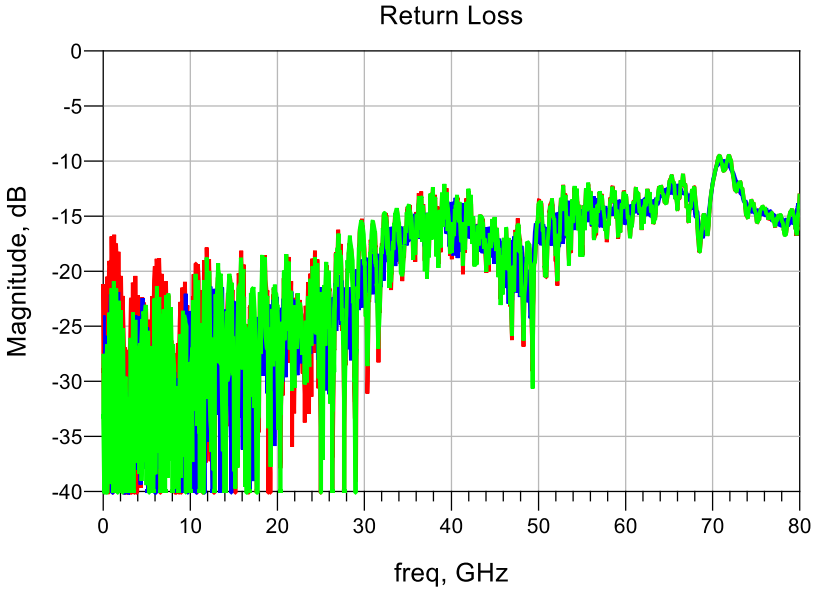


Channel includes at each end of 1m cable,

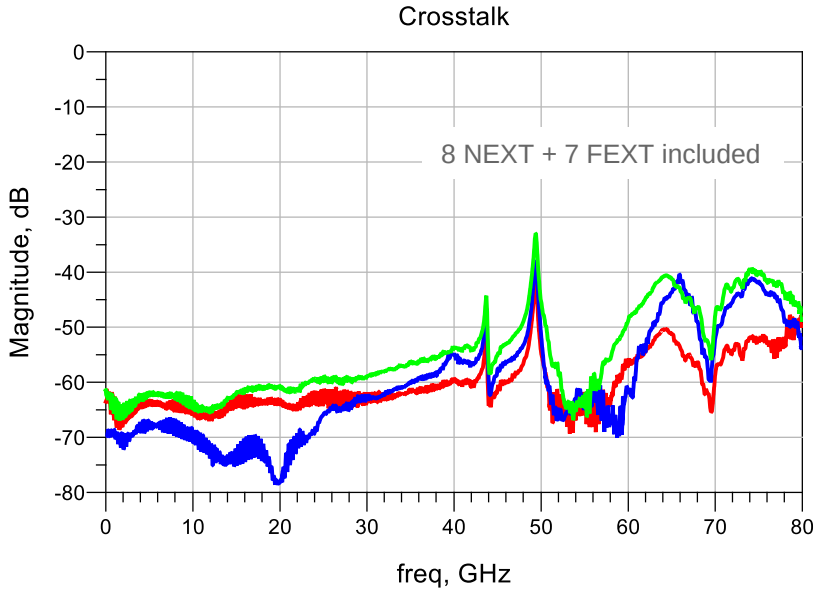
- Cabled backplane connector to cabled backplane connector
- Cable Termination to cabled backplane connector
- 10”, 30AWG Cable
- Cable termination to near chip connector
- Near chip connector
- Near chip transition via and breakout traces
- BGA footprint + breakout
- 2.7dB traces from near chip connector to BGA

Performance Comparison





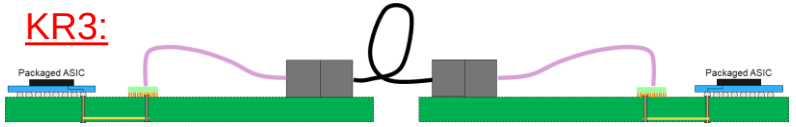
	TP0 – TP5 IL, dB @53.125GHz
KR1	19.3
KR2	18.3
KR3	27.4



KR1:

KR2:

KR3:



Crosstalk pinmap*

F F N N
F F N N
F V N N
F F N N

*BGA crosstalk contribution only includes FEXT

Summary

- Simulation results have been provided for 200G channels consisting of:
  - Backplane 200G concept connector, Both PCB right angle and cabled connector versions
  - Backplane concept connector includes footprint and via
  - 10 inches of internal cable assembly to NCC host connector and footprint
  - 2.7dB and 7 dB loss host traces
  - BGA footprint and breakout model
- Not a final position on component or channel performance, further development is in process
- Intent is to provide meaningful support for addition of an 802.3dj backplane objective
- A range of host implementation architectures/technologies may be useful to enable 200G based modular systems
  - Internal cables can provide meaningful channel improvement and reach