Benefits of a Coherent Solution Tailored for 800G-LR1

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Introduction

- There is uncertainty on whether to adopt a FEC and wavelength for 800G-LR1 consistent with 80km reach applications, or select a FEC and wavelength specifically tailored to short reaches.
  - Williams et al made the case that "A coherent implementation based on oFEC can support LR, ER and ZR enabling cost optimization for the lower volume applications through technology reuse and simplified testing" (slide 20).
  - Maniloff et al made the case for a distinct coherent solution for the 802.3dj 10 & 40 km SMF objectives based on a concatenated RS544/BCH(126,110) FEC which can support O-Band implementations
- The RS544/BCH(126,110) should allow 800LR1 to address latency sensitive applications, with significant FEC power reduction
- Adopting O-band can reduce power and latency further :
  - Low dispersion can translate to lower DSP power and latency
  - Enables dedicated low power DSP architecture

Baud rate sampling coherent architecture

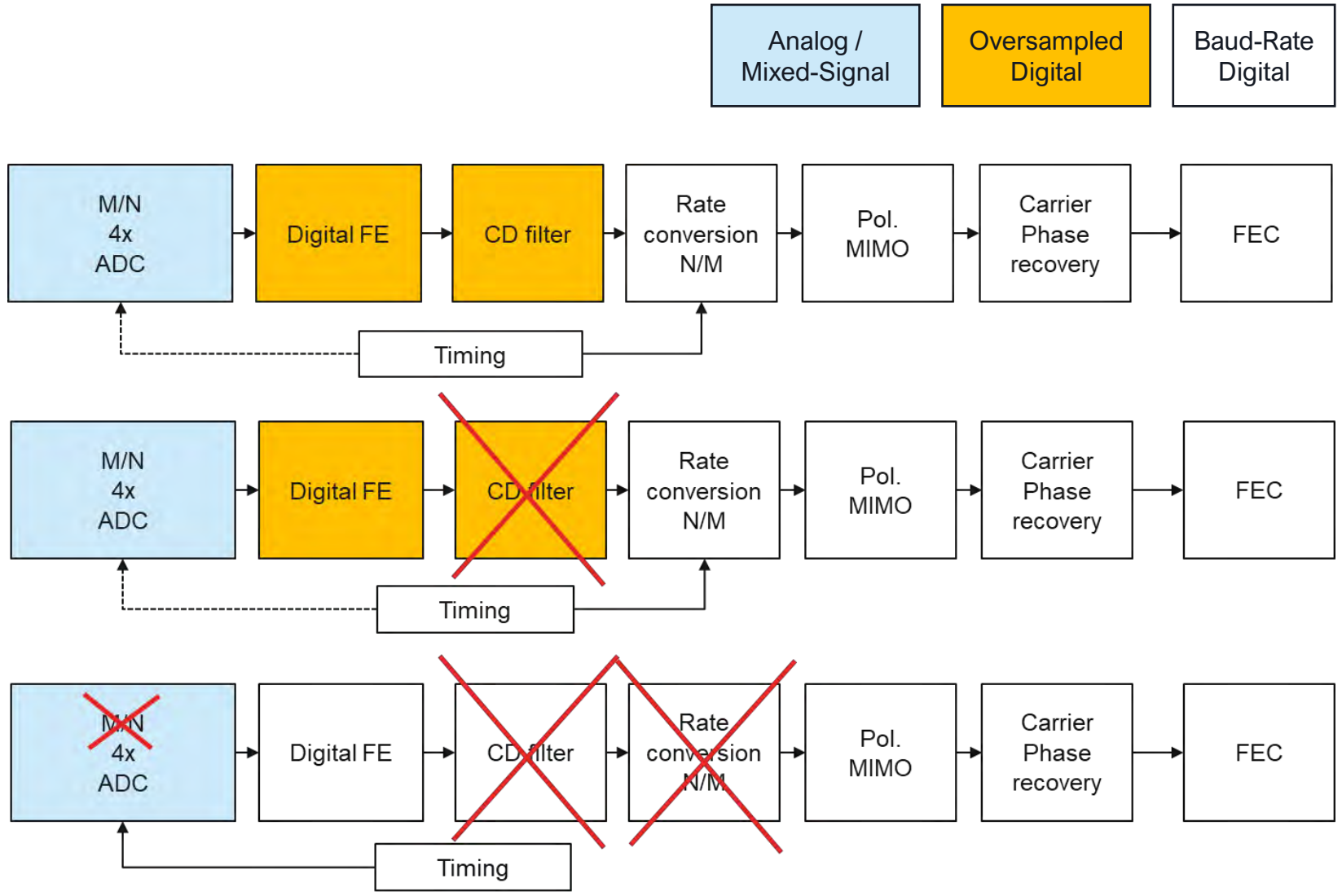
- Baud-rate coherent DSP and its benefits were discussed in:
  - X. Zhou, R. Urata, H. Liu, “Beyond 1 Tb/s Intra-Data Center Interconnect Technology: IM-DD or Coherent,” *IEEE JLT*, Jan 2020.
- Baud rate coherent is suitable for short reach applications, like LR, due to limited support for CD and DGD
  - The CD/DGD limitations of baud rate sampling need to be further explored
- This presentation helps to quantify how synchronous baud-rate sampling:
  - Reduces DSP power consumption
  - Can provide a low BER floor, compatible with low-latency and low-power FEC
  - Reduced DSP latency

Short-Reach Coherent DSP Alternatives

1. C-Band Coherent DSP
- Modest oversampling, M/N
- FFT based CD filter
- Rate conversion after the CD filter

2. O-Band Coherent DSP
- Greatly reduced CD filter
- Reduced DSP latency using time domain EQ

3. O-Band Coherent Synchronous Baud-Rate-Sampling DSP
- Significant further power savings
- Further reduction in DSP latency



Power Savings of Synchronous Baud-Rate Sampling

DSP

- Eliminate the need for resampling logic
  - Eliminates the associated aliasing
- Operate the equalization logic with a lower (baud-rate) clock frequency
- Time-domain equalizer tap count (hence, power) is proportional to reach

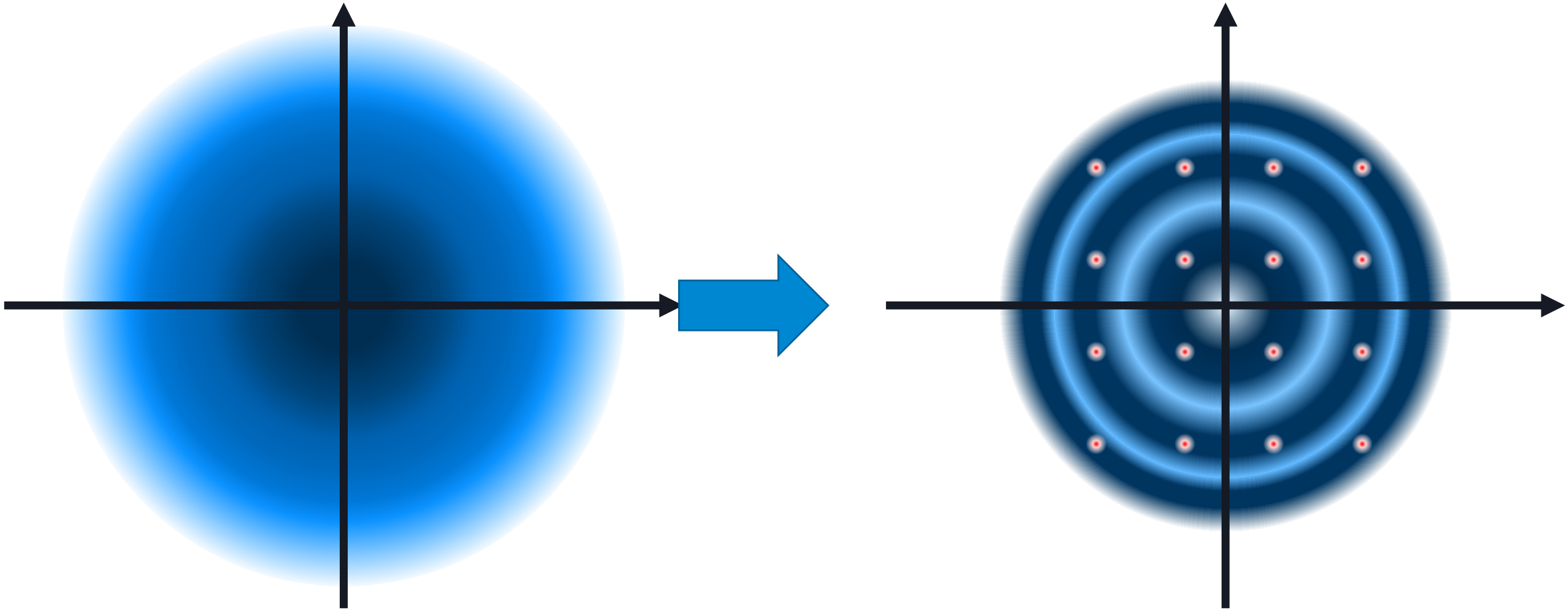
Analog Front-End

- ADC is one of the two main power consumers in coherent DSP, and it benefits from baud-rate sampling
- An ADC operating at the baud-rate instead of M/N higher than the baud rate reduces power by a factor of N/M
- Baud-rate sampling synchronized to the symbol timing improves the samples' peak-to-average power ratio (next slide)
- Allows for reduction in ADC effective resolution by ½ bit ⇒ at least 33% power savings
- Total power of the ADC can be reduced by approximately 50% (assuming M/N = 1.2)
- Clock generation (PLL) can also operate at a lower frequency

Cartoon Illustration of ENOB Advantage

Oversampled Constellation

Synchronous Baud-Rate-Sampled Constellation

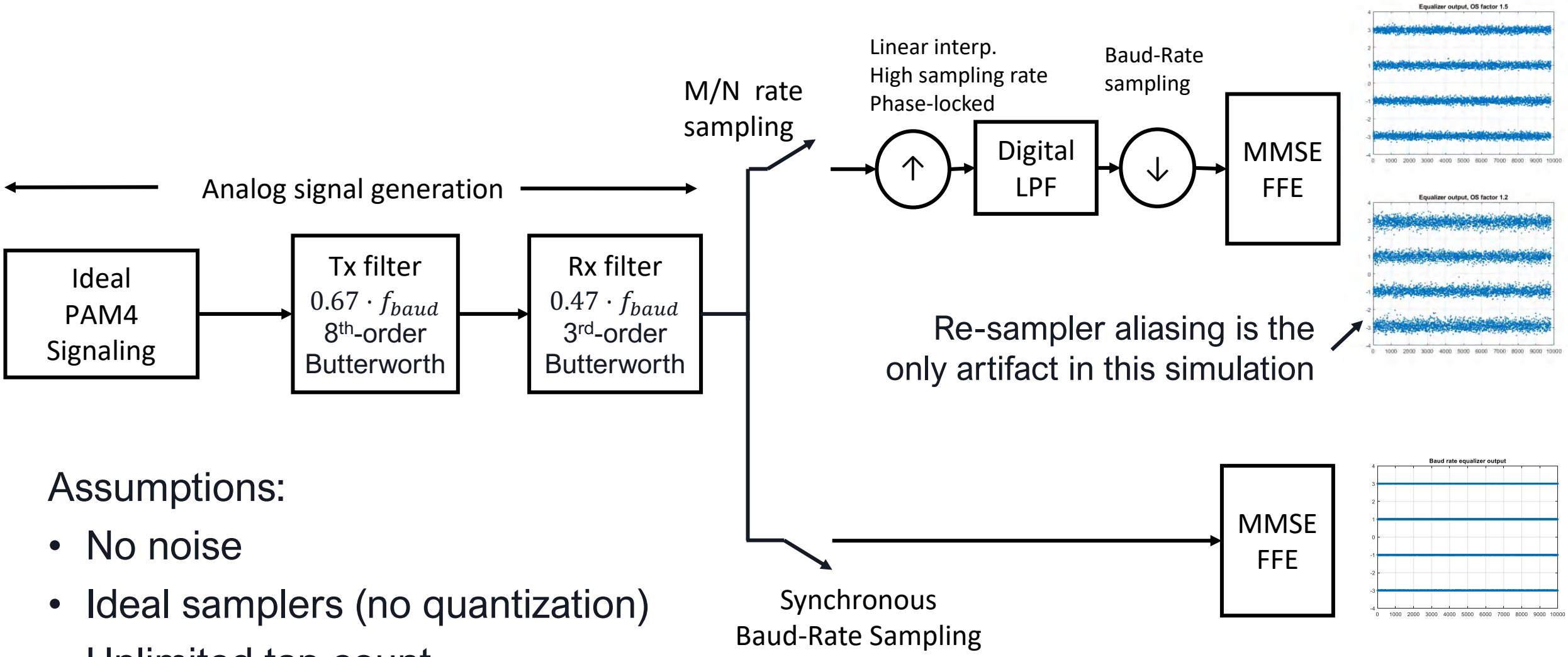


Lower peak-to-average power ratio

Comparison of Coherent Rx DSP Architectures

Block	Feature	Synchronous Baud-Rate Sampling	M/N x Oversampling
ADC	ADC sampling rate	f_{baud}	$f_{baud} \cdot \left(\frac{M}{N}\right)$
	ADC ENOB	5.5	6
Timing loop	Timing phase correction	Analog clock phase shifter	Digital Polyphase Re-sampler
	Timing error detection	Detector @1sps	Detector @1 or 2 sps
Data path	CD compensation	@1sps	@M/N sps
	Pol. MIMO	@1sps	@1 sps
	Phase recovery	@1sps	@1 sps

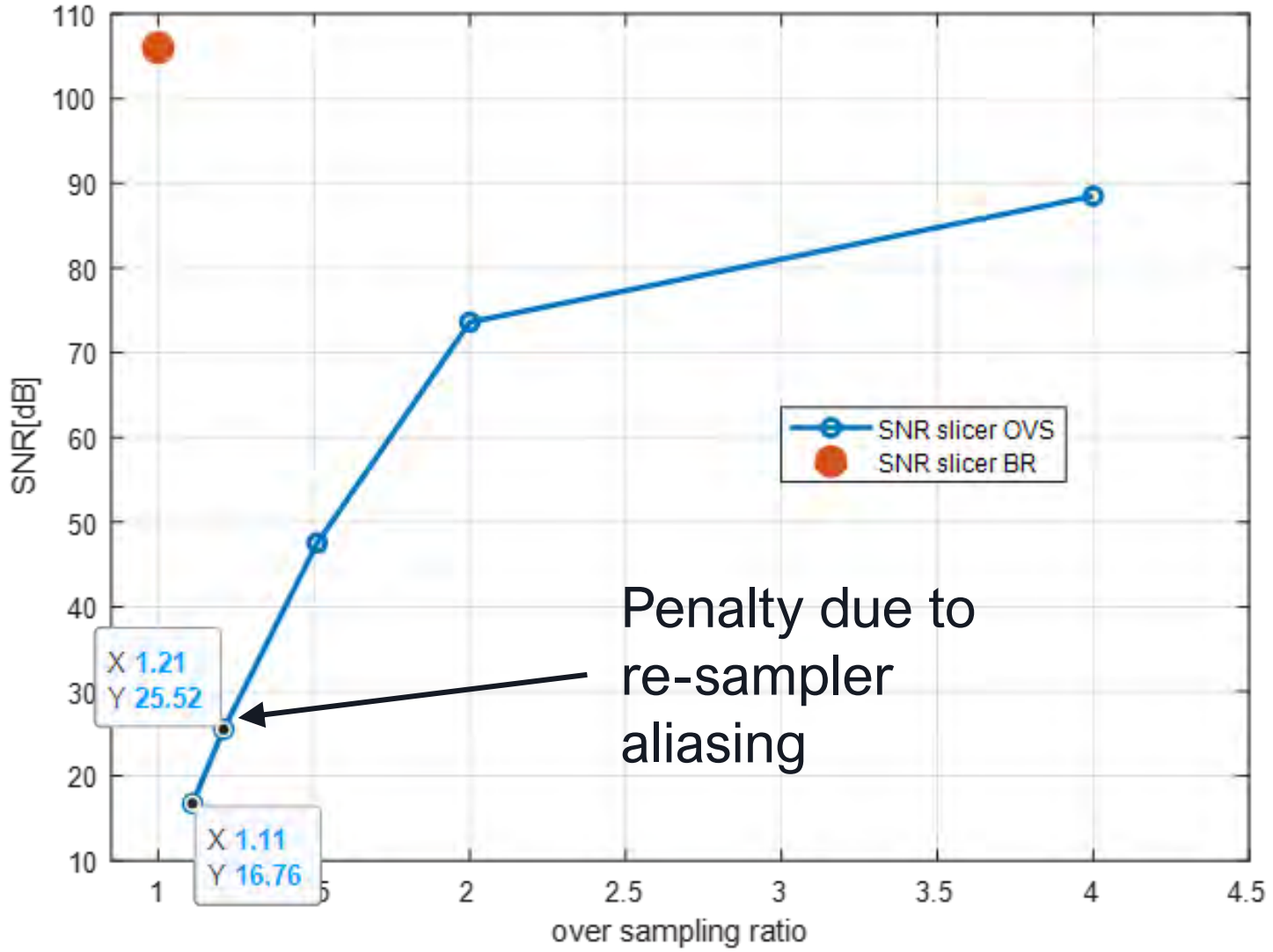
Simulation to Illustrate Re-sampler Aliasing



Assumptions:

- No noise
- Ideal samplers (no quantization)
- Unlimited tap count

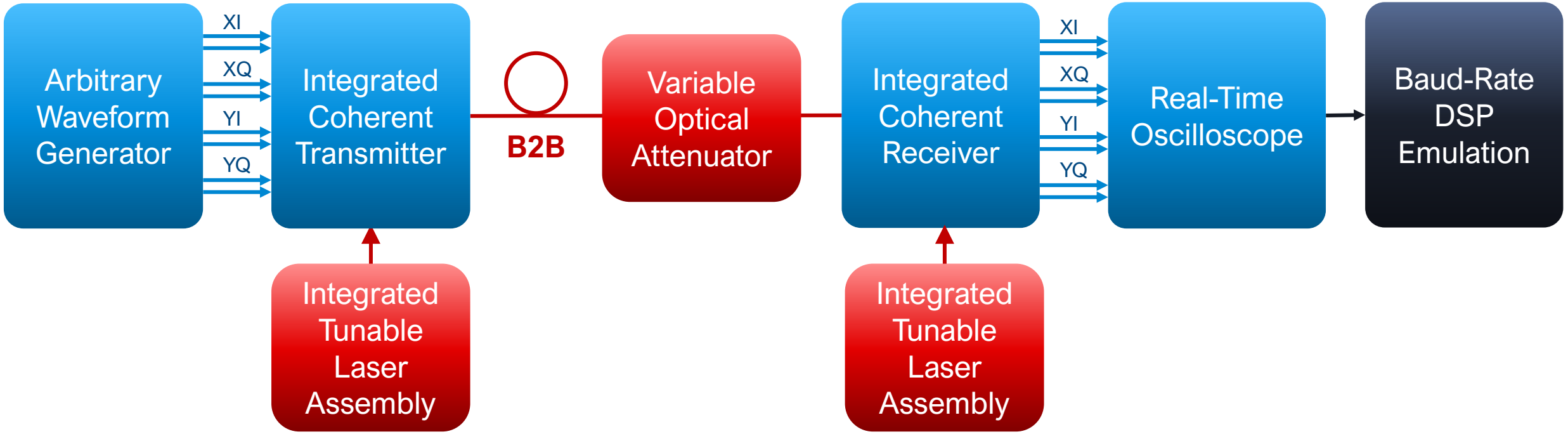
Aliasing Penalty of Low Over-Sampling Rate DSP



- Non-negligible penalty due to aliasing of the signal for oversampling ratios up to M/N = 1.2
- No penalty for synchronous baud-rate sampling
- Performance improvement noticeable over short reaches
- Performance improvement is increased with higher Tx BW

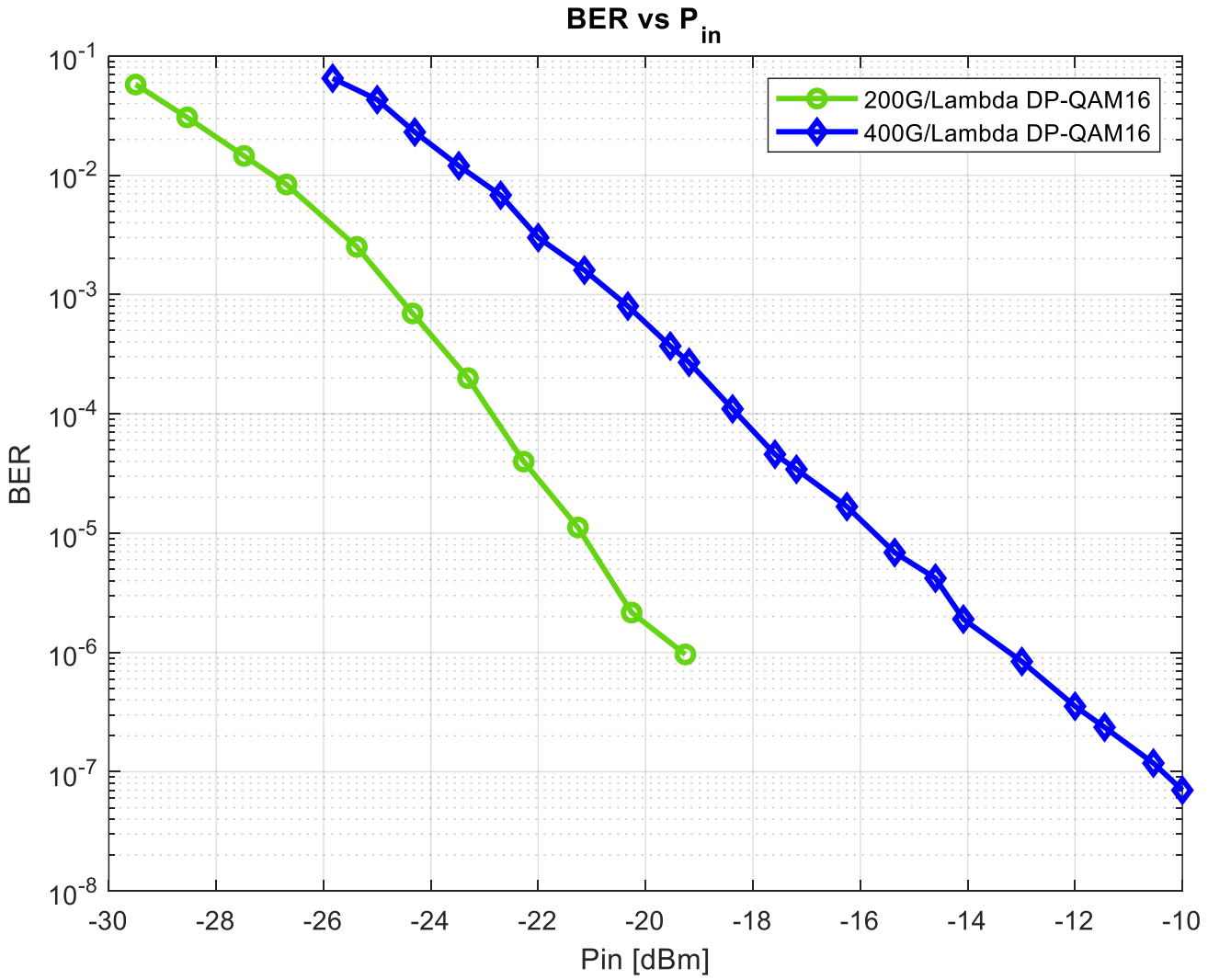
Experimental Demonstration of Baud-Rate Processing

Intradyne DP-QAM16 (200G/Lambda and 400G/lambda)



Experimental Demonstration of Low-BER Floor

- Low-BER floor in B2B experiment illustrates that a baud rate architecture can allow significant improvement in implementation loss
- Allows for potential lower power and lower latency modes in short-reach applications



What Would A Dedicated Short-Reach Coherent Solution Look Like?

- Low-latency, low-power FEC and framing
  - Concatenated (Type 2) RS(544,514)+BCH(126,110) + pilot frame
- O-Band
  - Reduced CD affords DSP power savings
  - Maximizes potential for low-cost lasers
- Low-cost laser scheme
  - Optionally with DSP feedback for accurate frequency control
- Synchronous baud-rate sampling DSP
  - Oversampling ratio of M/N = 1.2 would otherwise be required to prevent aliasing from significantly degrading performance
    - Consistent with analysis in [R. Nagarajan, I. Lyubomirsky and O. Agazzi, "Low Power DSP-Based Transceivers for Data Center Optical Fiber Communications," *IEEE JLT*, Aug. 2021]
  - ➢ Baud-rate sampling affords 17.5% reduction in sampling rate for the same baud rate with attendant savings in DSP and analog power consumption
- Low latency FEC with baud-rate sampling, affords 13% reduction in sampling rate compared with 1.2x oversampling and a segmented oFEC

Summary

- Adopting concatenated FEC and O-band for 800G-LR1 will open the door to potential reductions in power, cost, and latency
- Synchronous baud-rate sampling and processing can be a significant aspect of these savings
  - Reduced complexity of the digital signal processing
  - Relaxed specifications on the analog front-end
- Low bit error rates are demonstrable using synchronous baud-rate sampling

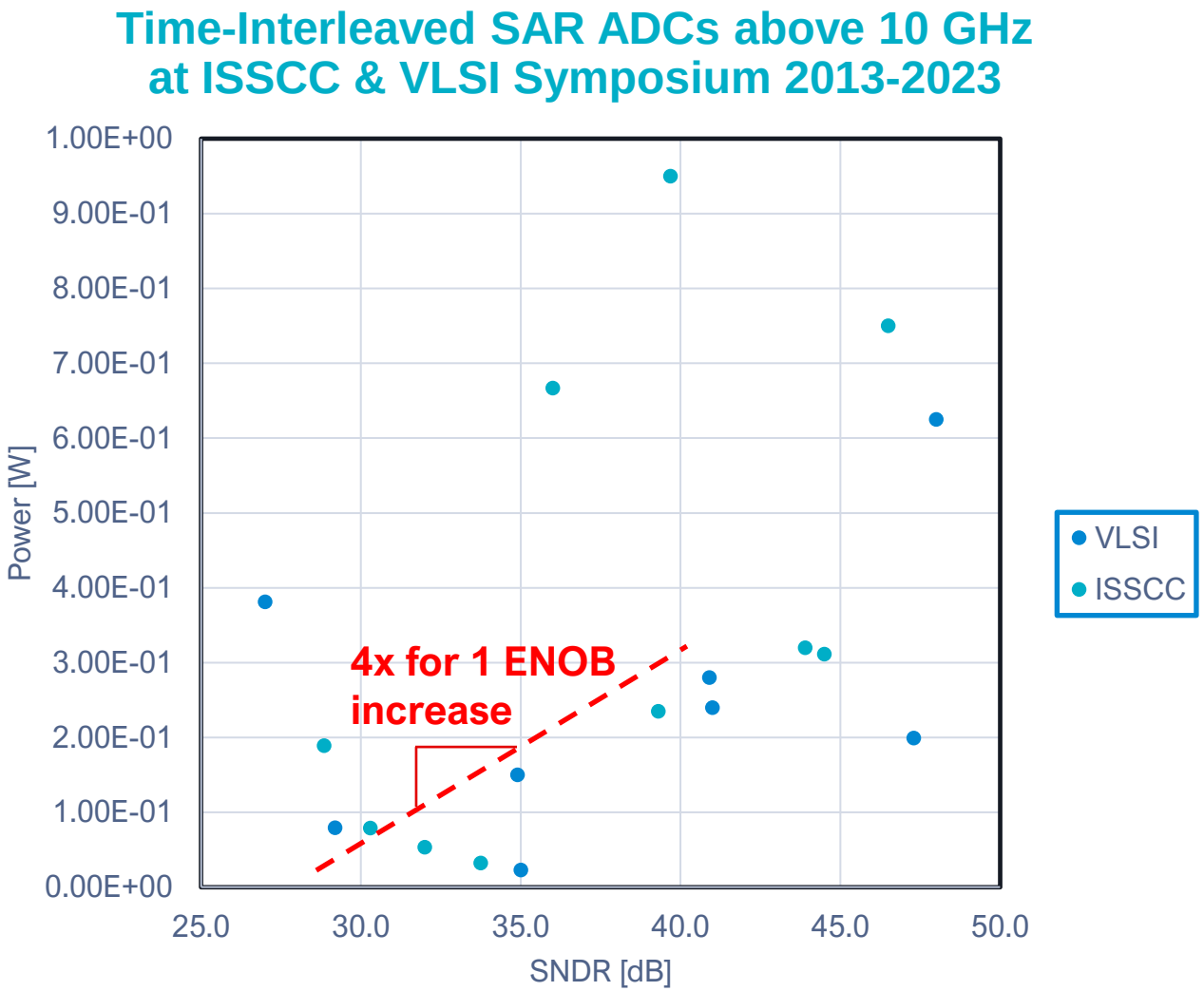
ADC Power vs. SNDR
(Backup)

- In noise-limited designs, for fixed bandwidth,

$$\text{ADC Power} \propto \text{SNR}$$

$\Rightarrow$ Power increases 4x per 6dB

- In spite of many challenges specific to high-speed designs, a survey of best-in-class ADCs in the range of interest on the right reveals this trend



B. Murmann, "ADC Performance Survey 1997-2023," [Online]. Available: https://github.com/bmurmann/ADC-survey