

Updated CRU Bandwidth Recommendation for 200G Interfaces

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Supporter List

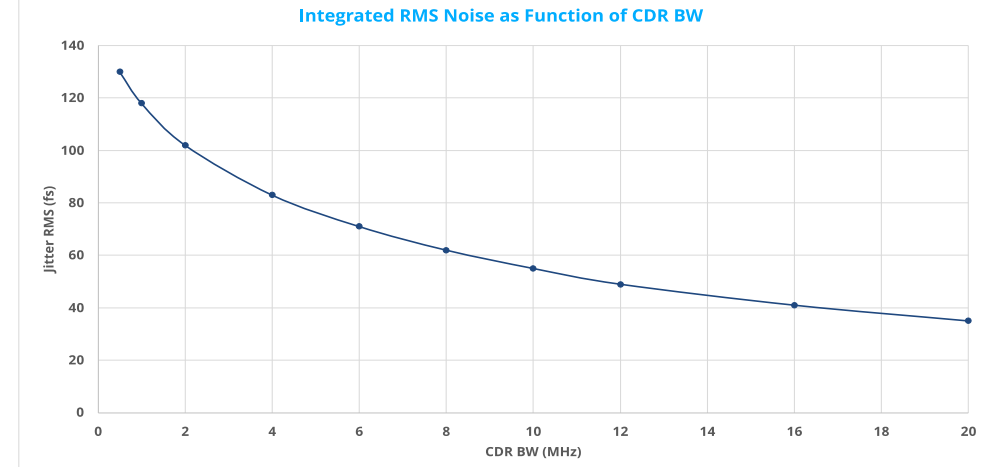
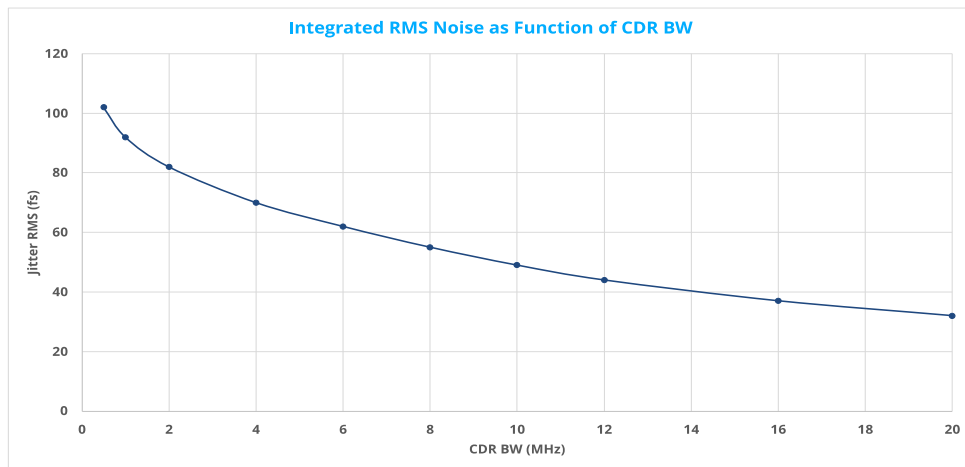
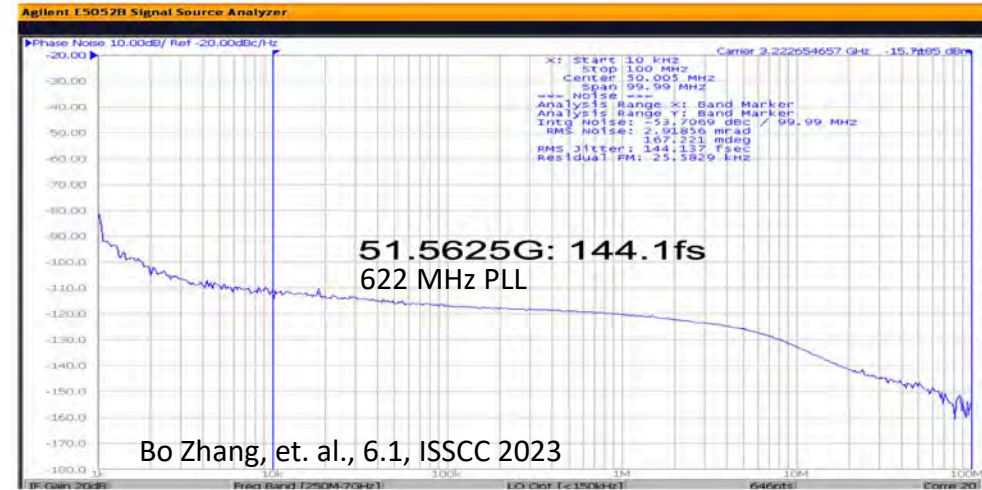
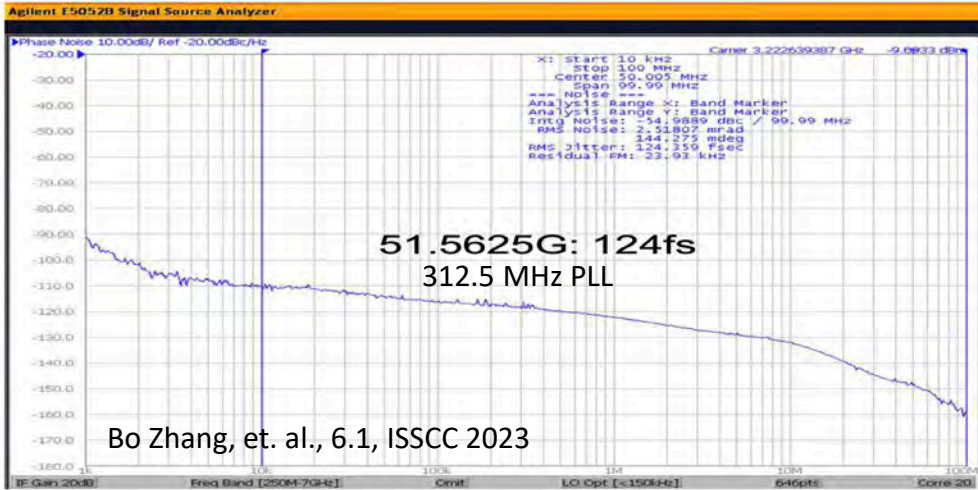
- Eric Maniloff – Ciena
- Adee Ran – Cisco
- Upen Kareti – Cisco
- Phil Sun – Credo
- Greg Le Cheminant – Keysight
- Arash Farhoodfar – Marvell
- Lenin Patra – Marvell
- Mike Dudek – Marvell
- Tobey P.-R. Li – MediaTek
- Piers Dawe – Nvidia

Background

- ❑ As a compromise 802.3bs task force selected 4 MHz CRU “Golden CRU or PLL” BW for both 26.5625 GBd and 53.125 GBd PAM4
- ❑ Following presentations in 802.3bs proposed reducing golden CDR BW from $f_{\text{Baud}}/2578$ to $f_{\text{Baud}}/6640.625$ (4 MHz) for 26.5625 GBd PAM4) and $f_{\text{Baud}}/13281.25$ (4 MHz) for 53.125 GBd PAM4
 - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
 - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
 - http://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf
- ❑ Following contributions from 802.3cd investigates if jitter/wander passing through 2:1 mux are bounded or not with f_{Baud}/X ratio reduced by $\frac{1}{2}$ in case of 53.125 GBd PAM4
 - https://www.ieee802.org/3/cd/public/Jan18/ghiasi_3cd_01_0118.pdf
 - https://www.ieee802.org/3/cd/public/July17/dawe_3cd_03_0717.pdf
- ❑ In 802.3dj we face the same set of questions to keep $f_{\text{Baud}}/13281.25$ “doubles CRU BW”, which adds complexity and power to 200G SerDes or yet again halve $f_{\text{Baud}}/13281.25$ ratio
- ❑ Contribution in 802.3dj previously proposed to reduce CRU BW to $f_{\text{Baud}}/26562.5$
 - https://www.ieee802.org/3/dj/public/23_03/ghiasi_3dj_02a_2303.pdf .

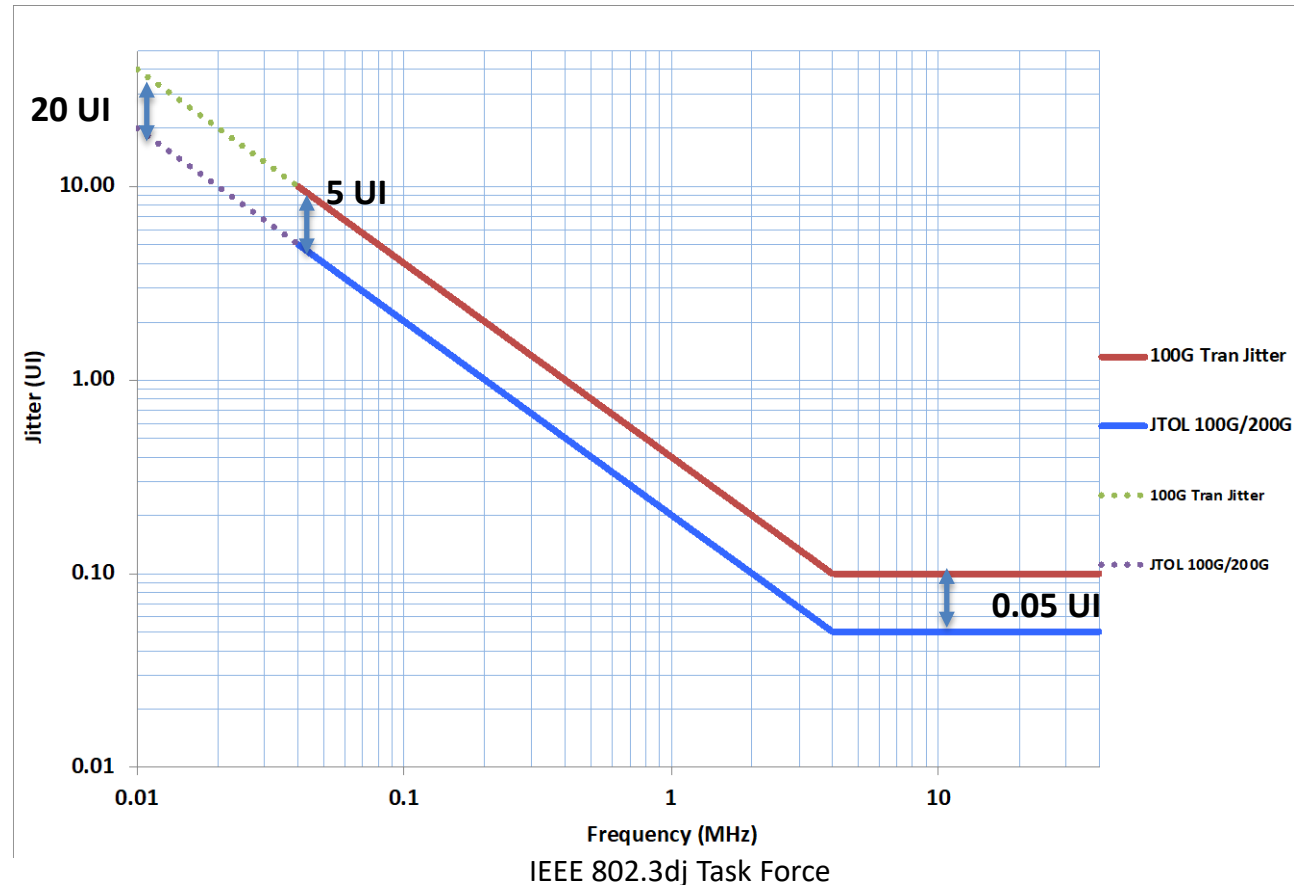
Typical Modern Low-Cost Oscillators

- Considering availability of low-cost oscillator doubling the CDR BW only provide small incremental relief to the transmitter, but doubling CDR BW is very substantial!



Implications of Staying with 802.3bs JTOL Limits

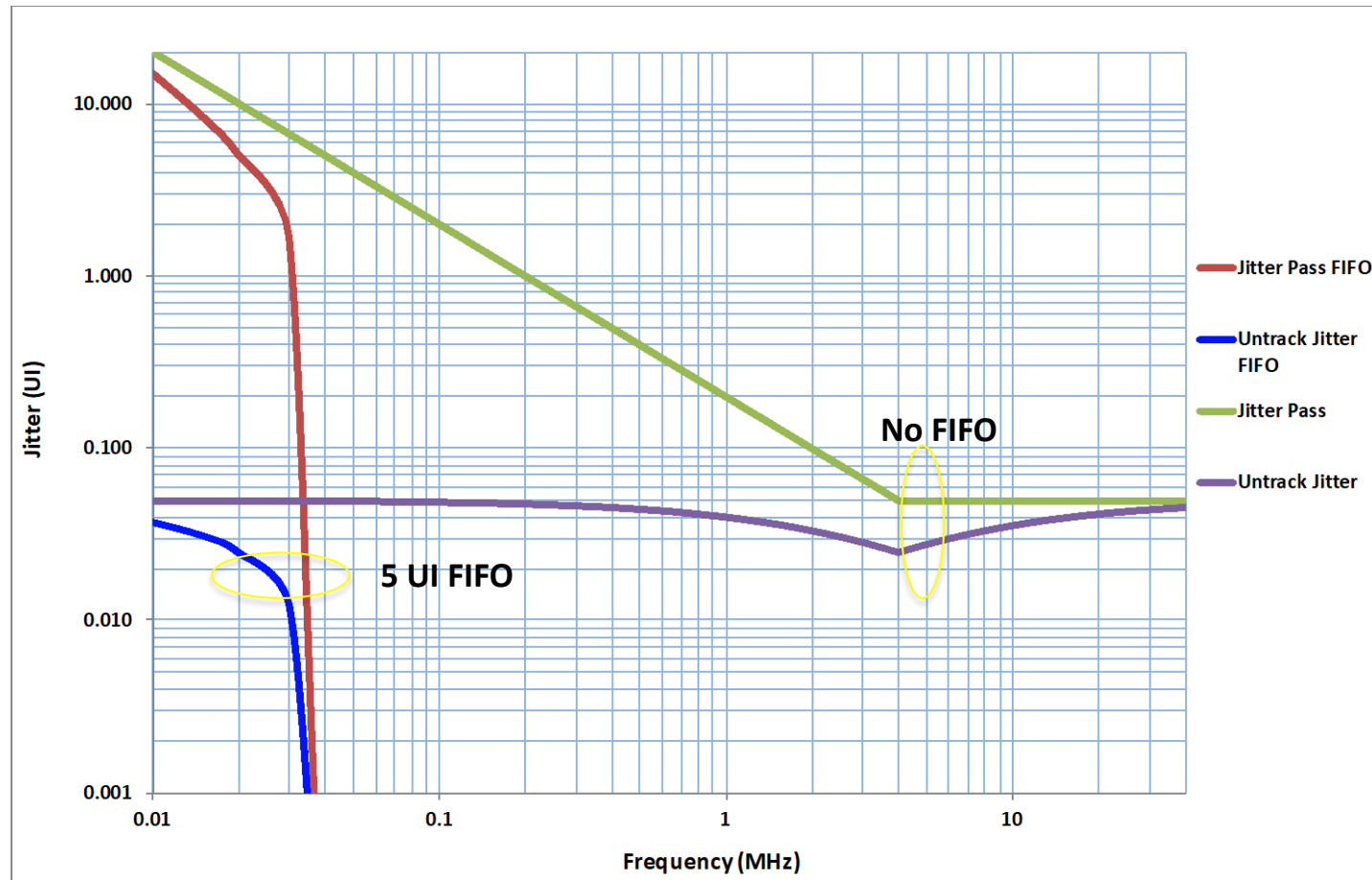
- What is the implication of 4 MHz JTOL on transfer jitter from from 100G to 200G PAM4 with 2:1 mux?
 - Jitter transfer is identical to 802.3bs 50G to 100G PAM4 2:1 mux/CDR
 - A 2:1 Mux chip FIFO needs to absorb 5 UI jitter from 100G inputs instead of 50G inputs
 - Low frequency wander < 40 kHz is also bounded!



Wander from 2:1 Mux is Bounded

❑ Wander in excess of FIFO depth will pass through to TX output

- A 2:1 mux chip with 5 UI (input serial bitrate) FIFO practically speaking has no penalty
- A 2:1 Mux with no FIFO would have 0.05 UI of penalty!



Summary

- ❑ **In 802.3bs wisely the CRU BW was reduced from $f_{\text{baud}}/2504$ to support more complex ADC PAM4 receivers**
 - Otherwise, we would have no digital SerDes implementation given 53.125 GBd PAM4 would require a CDR BW of 21.2 MHz
 - Implementations would have been limited to rudimentary analog SerDes
- ❑ **Jitter/wander penalty through 2:1 mux is bounded and well understood**
 - As current CDR/DSP chips already implement jitter FIFOs
- ❑ **Considering doubling the CRU BW only brings marginal benefit for transmitter but has substantial penalty for ADC receivers the recommendation is to reduce current $f_{\text{Baud}}/13281.25$ by ~half of $f_{\text{Baud}}/26562.5$**
 - Corner frequency in jitter tolerance requirements is equal to the CRU BW above
 - Recommending 4 MHz for all 802.3dj PMD/AUIs operating at KP4 FEC and 4.27 MHz for all 802.3dj PMDs with SFEC per SFEC definition in [patra 3dj 01b 2303](#).

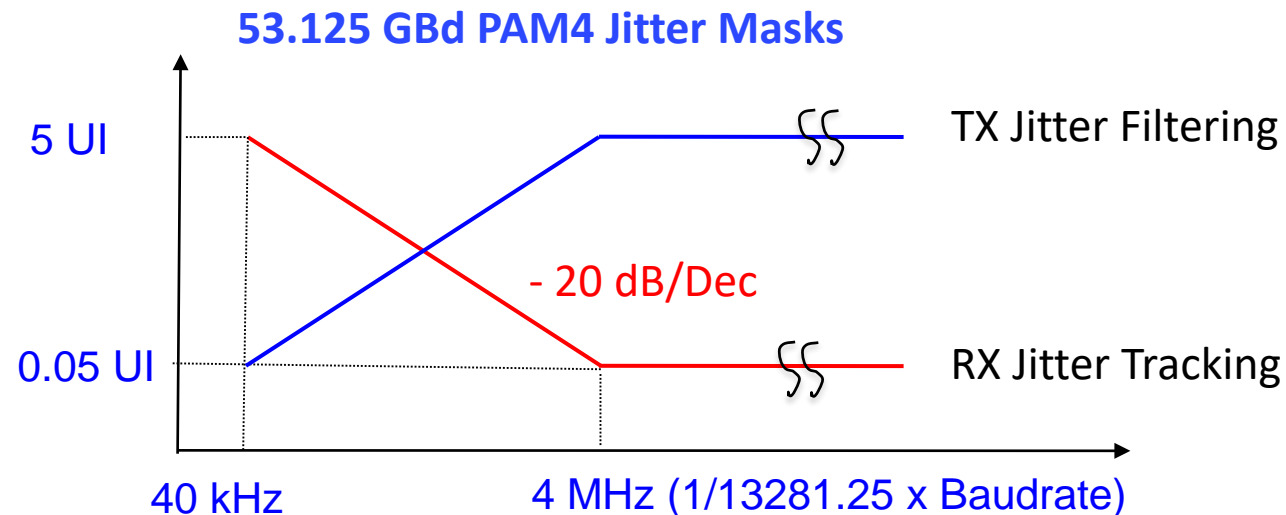
Straw Poll

- I support a CRU bandwidth and jitter tolerance corner frequency of 4 MHz for all 802.3dj PMD/AUIs operating at KP4 FEC and 4.27 MHz for all 802.3dj with SFEC per SFEC definition in https://www.ieee802.org/3/dj/public/23_03/patra_3dj_01b_2303.pdf (The calculation for CRU BW is based on the following $f_{Buad}/26562.5$ equation)
 - Yes
 - No
 - Need more information
 - No opinion/abstain.

Backup Material

Comprehensive Jitter Methodology

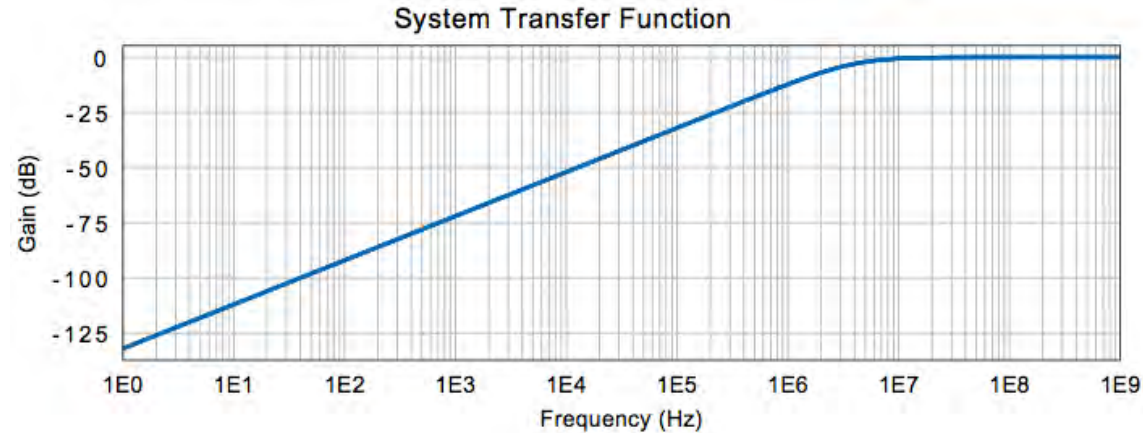
- A comprehensive methodology to test transmitters and receivers for jitter was developed during 1 GFC standardization in the FC-MJS project and later used in the Ethernet projects
- This methodology was based on systems using low-cost oscillators and a reduction in power supply filtering to enable low-cost high-volume applications
 - Transmitter test assumes low frequency jitter should be tracked by a receiver
 - Transmitter specs are relaxed by observing the transmitter using reference PLL with OJTF defined as a high pass single pole filter with -20 dB/dec rolloff and -3dB corner frequency at $1/13281.25 \times \text{Baudrate}$
 - Receiver test should complement transmitter test by verifying low frequency jitter is tolerated, example shown below is for a CRU/CDR response (Clause 124, 140, 151, 162, 163, 167, 120G, etc.)



The Role of Golden CRU in Jitter Tracking and Rejection

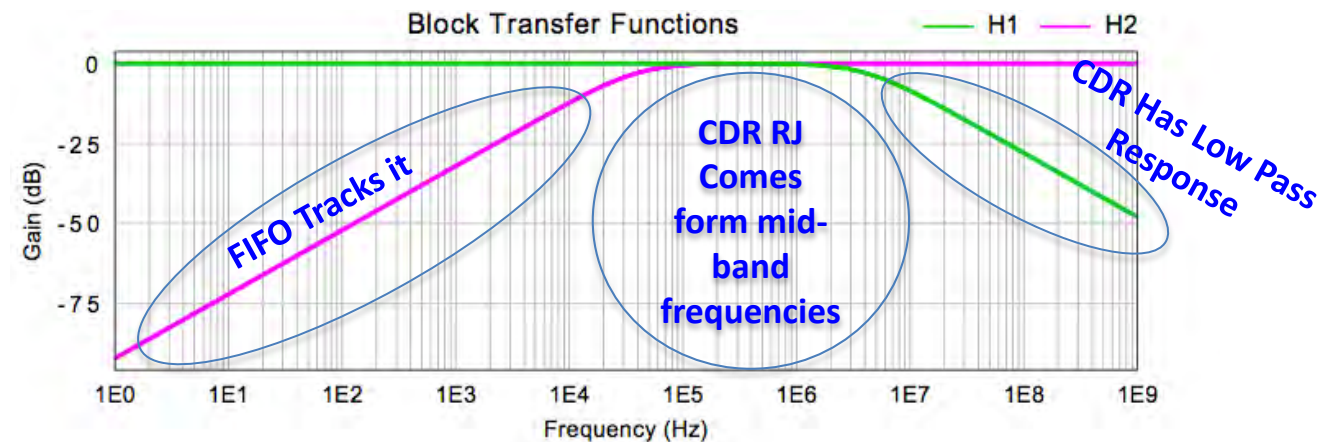
Transmitter jitter calculated with high pass filter “Golden CRU”

- Graph shown is for 4 MHz Golden CRU



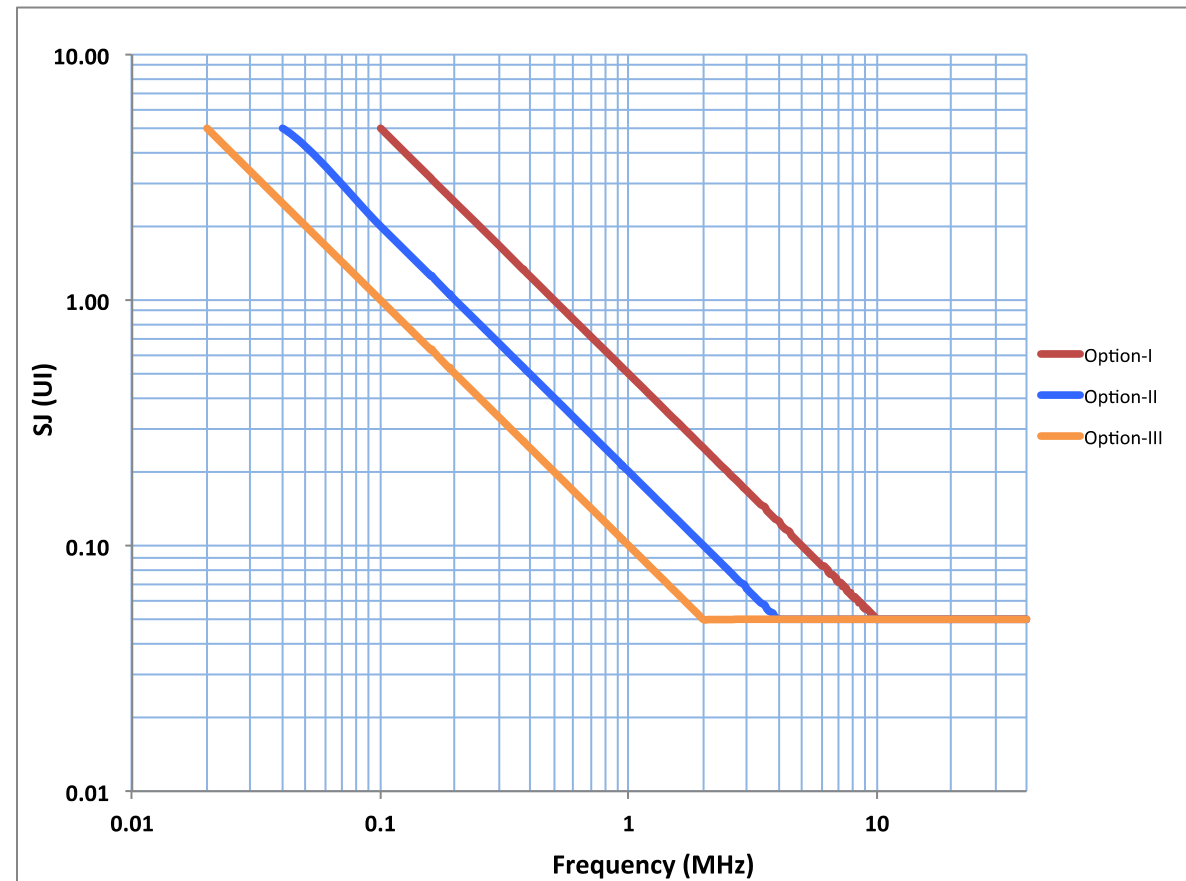
Receiver jitter analyzed by sliding band-pass filter

- Graph shown is for 4 MHz Golden CRU



In 802.3bs we Considered Several CDR Options

- **CL-88 10 MHz CRU BW offered only marginal benefit but increased CDR power and complexity**
 - In 802.3bs considered 2 MHz and 4 MHz, but for 4 MHz was adopted for both 26.55 GBd and 53.125 GBd PAM4
 - The question ahead of us is to either increase CDR with Baudrate or stay with ~ 4 MHz CRU BW?



Consideration for Golden CRU and CDR BW

❑ Consideration for the Golden CRU BW

- Oscillator phase noise
 - Typical oscillator have flat phase noise > 1 MHz
- Crosstalk
 - High frequency effects >> CRU BW
- VCO phase noise
 - No benefit when CRU BW > 4MHz

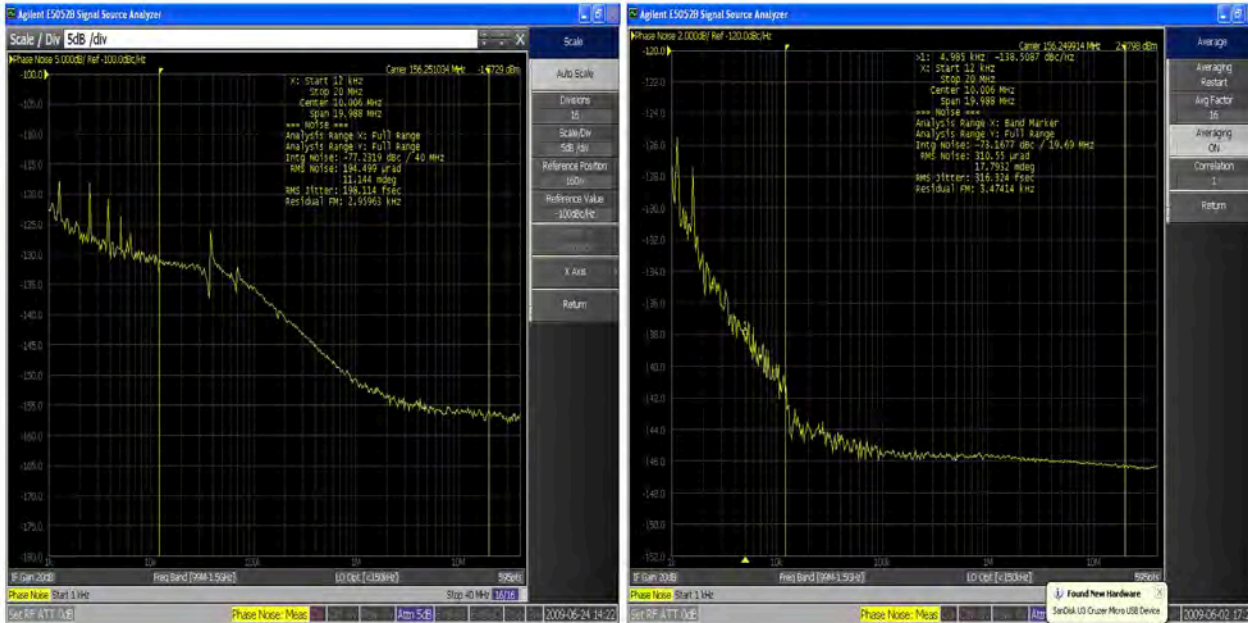
❑ Consideration for CDR BW

- Pattern dependent effect
 - Does not apply to 64B/66B/scrambled data with spectrum in the ~ 100 KHz
- Power
 - Higher loop BW require operating data-path/timing recovery at 2x speed resulting in higher CDR power
- DSP receiver
 - Timing recovery introduces latency making it challenging to meet ~8 MHz CDR loop BW if the CDR loop BW stays at current $F_{\text{baud}}/13281.25$ CDR
- Backward compatibility
 - 800G-AUI8 to 4x200G PMD require similar FIFO currently used in 400G-AUI8 to 4x100G PMDs
 - Not using jitter FIFO, the 2x1 mux operation will result in 0.05 UI of jitter penalty at the transmitter.

Legacy Low-Cost Oscillators

- Contribution from 802.3ba in 2010 where even for 13 years old oscillators there was only marginal benefit having CDR BW > 4 MHz

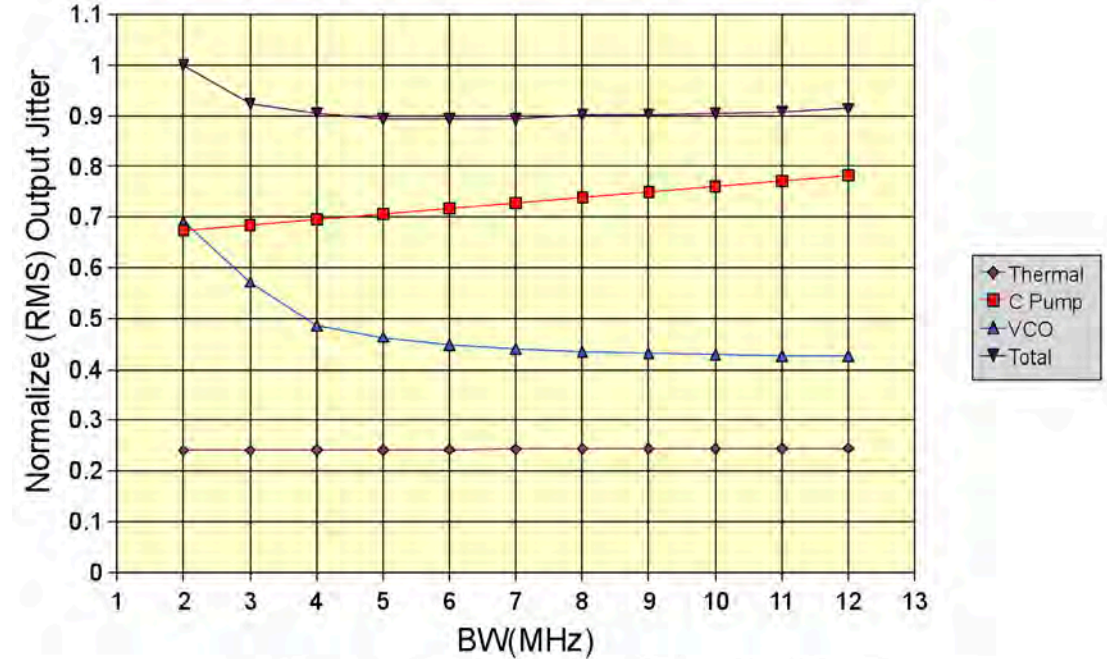
– https://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf



A. Ghiasi

IEEE 802.3ba Task Force Meeting, Jan 2010 New Orleans

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IEEE 802.3ba Task Force Meeting, Jan 2010 New Orleans