Partitioning AUI C2M and C2C BERs

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Background on Med and High Loss AUIs

- **During October session there was strong support to define Med and High Loss AUI considering splintering C2M application with assumption that there will significant power saving**
  - https://www.ieee802.org/3/df/public/22_10/motions_3df_221004.pdf

Straw Poll #1

For the front panel pluggable use case, I am interested in 200 Gbps/lane AUI C2M specifications for:

A. medium loss only (e.g. up to ~22 dB IL die-die per lusted_3df_01_220927)
B. higher loss only (e.g. up to ~36 dB IL die-die per lusted_3df_01_220927)
C. both medium and higher loss
D. need more information

pick one

Results: A: 17, B: 11, C: 49, D: 12

Background on Med and High Loss AUIs, cont.

- **During Nov. 2022 several contribution investigated various implementation of Med/High loss AUIs**
  - Lusted explored higher loss AUI
    - https://www.ieee802.org/3/df/public/22_11/lusted_3df_02_2211.pdf
  - Lusted explored Med loss AUI
    - https://www.ieee802.org/3/df/public/22_11/lusted_3df_03a_2211.pdf
  - Ghiasi and et. al. bottom-up analysis of medium and high Loss AUIs
    - https://www.ieee802.org/3/dj/public/23_01/23_0116/ghiasi_3dj_02a_230116.pdf
  - li_3dj_01a_2303 COM analysis show that ~50% of medium loss AUIs fails with assumed less capable 8 tap DFE equalizer
    - More capable equalizer 24 tap DFE +6x2 banks of FLT with 80 UI operates with margin on channel up to ~35 dB.

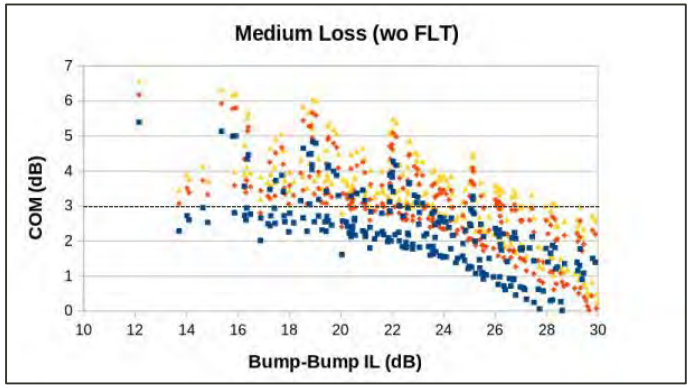
Ghiasi AUI Bottom-Up Analysis

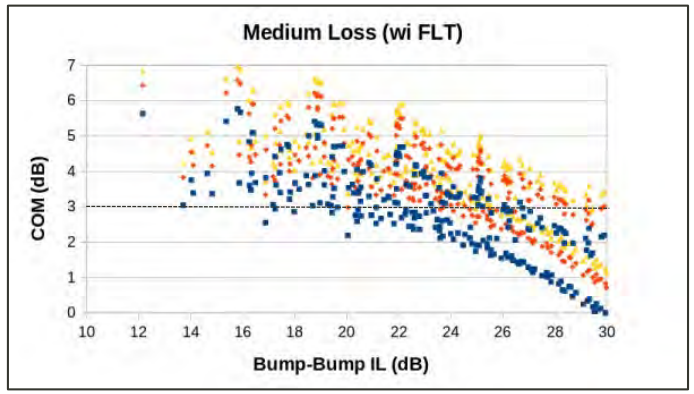
- **Starting point for 200G AUIs/C2Ms:**
  - AUI Type I supporting 11” conventional PCB
    - TP0-TP1a loss increased from 16 dB@100G to ~22 dB
    - Bump-bump loss ~35 dB
  - AUI Type II cabled host
    - TP0-TP1a loss 13.0 dB
    - Bump-bump loss ~26.0 dB
  - AUI conventional NIC supporting 5” PCB
    - TP0-TP1a loss 14 dB
    - Bump-bump loss ~22 dB
  - AUI Type III cabled substrate (CPC)
    - TP0-TP1a loss ~13 dB
    - Bump-bump loss ~26 dB
  - AUI Type V NPO
    - Bump-TP1a loss ~15.5 dB
    - Bump-bump loss ~18 dB.

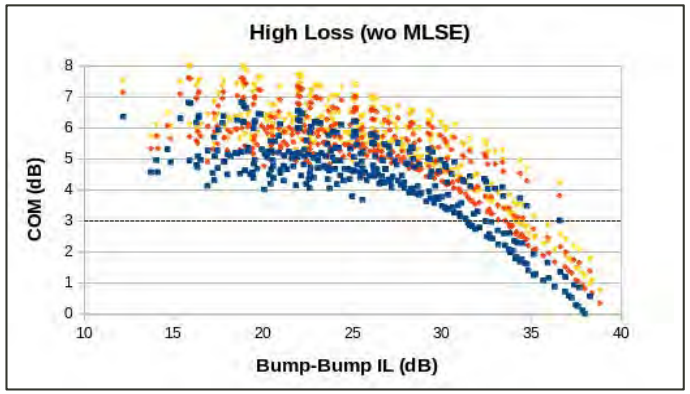
Loss Parameters @ 53 GHz A. Ghiasi - Rev 1.1 1/10/2023	Loss	Length or #	AUI Type I Conventional PCB	AUI Type II Cabled Host	AUI NIC Conventional PCB	AUI Type III Cabled Substrate	XSR+ NPO
Host PCB Loss (dB/in)	1.5	11	16.5	NA	NA	NA	NA
NIC PCB Loss (dB/in)	1.65	5	NA	NA	8.25	NA	NA
Cabled Host PCB Loss (dB/in)	1.5	2	NA	3	NA	NA	NA
Cable Loss (dB/in)	0.3	12	NA	3.6	NA	3.6	NA
Plug Board/PIC/HCB Loss (dB/in)	1.5	1.7	2.55	2.55	2.55	2.55	2.55
AUI Connector Loss (dB)	1.65	1	1.65	1.65	1.65	1.65	NA
Host Via Loss (dB)	0.8	2	1.6	1.6	NA	NA	NA
NIC Via Loss (dB)	0.6	2	NA	NA	1.2	NA	NA
Host Package Loss (dB/mm)	0.21	45					
NIC Package Loss (dB/mm)	0.225	16					
CDR Package Loss (dB/mm)	0.225	10					
Host/NIC PKG Mode Con. Loss (dB)	1	NA	10.45	10.45	4.6	10.45	10.45
CDR PKG Mode Con. Loss (dB)	0.4	NA	2.65	2.65	2.65	2.65	NA
TGA Connector Loss (dB)	0.3	NA	NA	0.3	NA	NA	NA
Socket Loss (dB)	0.2	NA	NA	NA	NA	0.2	0.2
NPO Substrate Loss (dB/mm)	0.095	50					
NPO Substrate Loss (dB)	4.75	NA	NA	NA	NA	4.75	4.75
TP0-TP1a Loss (dB)	NA	NA	22.3	12.7	13.65	12.75	4.95
Bump-TP1a (dB)	NA	NA	32.75	23.15	18.25	23.2	15.4
Bump-Bump Loss (dB)	NA	NA	35.4	25.8	20.9	25.85	17.95

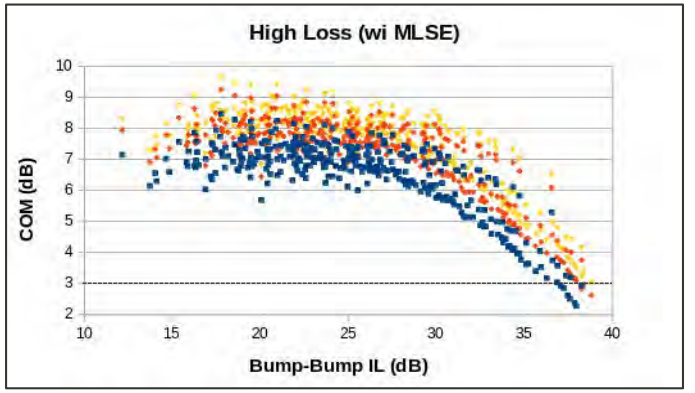
AUI Medium/High Loss COM Analysis

- **li_3dj_01a_2303 COM analysis indicates**
  - Med loss equalizer 8 DFE is inadequate (optional FLT is 3 banks of 3 with 80 UI span is needed even for 22 dB AUIs)
  - High loss equalizer 24 DFE + 6 banks of 3 DFEs with span of 80 UIs
  - Evan at DER of 5E-5 to support channel up to 22 dB require floating taps due to channel reflections
  - High loss AUIs without MLSE pass all channels up to ~34 dB, but MLSE may be need for margin!









How to Partition and Split AUI Application

- **li_3dj_01a_2303 data indicate assumed type I equalizer is under-powered for medium loss AUI**
- **lusted_3dj_elec_01_230504 suggest categorizing AUI equalizer from mild to spicy**
  - Given DSP implementation type II and type III equalizers are not that different given both have 80 UI span
  - The Spicy type IV equalizer is not that different than type II/III given that MLSE can be turned on/off
  - Only type-I (mild) equalizer justifies defining a 2nd AUI C2M application incompatible with high loss AUI!

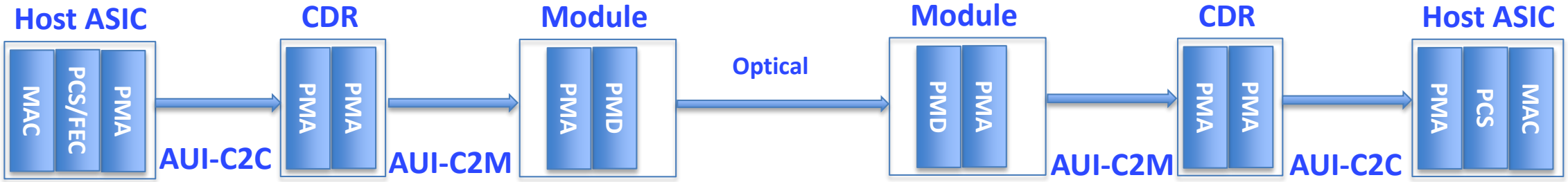
- Class I/II/III/VI

				Exploratory of 802.3dj Medium Loss AUI C2M		Exploratory of 802.3dj High Loss AUI C2M	
Parameter	802.3ck C2M	802.3ck CR	802.3ck KR	802.3ck C2M-like	802.3ck C2M-like + FLT	802.3ck CR-like	802.3ck CR-like + MLSE
DER_0	1E-5	1E-4	1E-4	1E-5/5E-5/1E-4	1E-5/5E-5/1E-4	1E-5/5E-5/1E-4	1E-5/5E-5/1E-4
SNR_TX	32.5	32.5	33	32.5	32.5	33	33
R_LM	0.95	0.95	0.95	0.95	0.95	0.95	0.95
TxFIR Length	4 (2 pre)	5 (3 pre)	5 (3 pre)	5 (3 pre)	5 (3 pre)	6 (4 pre)	6 (4 pre)
eta_0	4.10E-08	9E-09	8.2E-09	2.05E-08	2.05E-08	4.1E-09	4.1E-09
N_b	4	12	12	8	8	24	24
N_bg	0	3	3	0	3	6	6
N_bf	-	3	3	3	3	3	3
N_f	-	40	40	80	80	80	80
MLSE	0	0	0	0	0	0	1
Ref TX/RX Class				I	II	III	VI

(Mild) (Spicy!)

802.3bs FEC Architecture

- **802.3bs analysis by Anslow stole 0.1 dBo to support 4 AUIs 2x(C2C+C2M) sub-links operating 1E-5 BER with end-end RS(544,514) FEC**
  - There is also strong support to support 4 AUI sublinks also in the 802.3dj
  - C2C links not having pluggable connector expect to operate with better BER than C2M AUIs
  - We adopted optical PMDs/FEC based on 0.1 dBo allocation for AUIs in the 802.3bs and we didn't define 100G IO till 802.3ck!

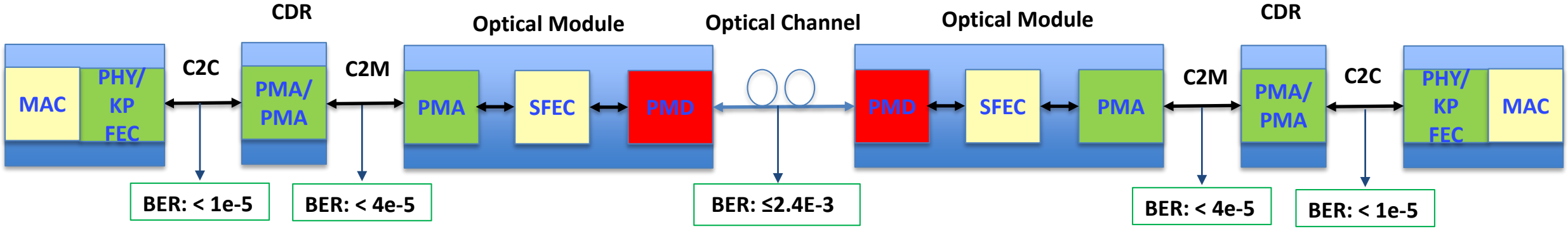


	RS(544,514) FLR = 6.2E-11			
	Electrical		Optical	
1:2 Same FEC, a = 0.75 worst skew	Burst	1.4E-6*	Random	2.4E-4
1:2 Same FEC, a = 0.75 worst skew	Burst	2.9E-6*	Random	2E-4
a = 0.75 misaligned	Burst	5.2E-6*	Random	2.4E-4
Random errors	Random	8.2E-5	Random	2.4E-4

Note – these values are the BER **including** the additional errors due to the bursts. To account for burst errors, the values marked with "*" have been multiplied by 4 when a = 0.75.

Concatenated FEC Scheme Supporting 4 AUI Sublinks

- **Patra_3dj_01a_2305 updated analysis including burst with several interleavers for 5E-5 AUI PHY BER calculates 200G/400G and 800G/1.6TbE PMD BERs**
  - To support AUI PHY BER of 5E-5 with 6-way interleaver the PMD BER is 2.4E-3
  - With 5E-5 allocated to AUI PHY, figure below show a possible BER split between C2C and C2M.



Implementation *	AUI PHY BER	200G/400G PMD BER	800G/1.6TbE BER
SFEC no Inter- leaver	5E-5	1.4E-3	1.4E-3
SFEC+6-way Conv.	**5E-5**	**2.4E-3**	**2.4E-3**
SFEC+12-Way Con	5E-5	3.3E-3	3.3E-3

* For additional FEC implementation options see Patra_3dj_01a_2305

Summary

- **The electrical adhoc has significant work ahead of them**
  - Identify and validate the acceptable C2M channels
  - Continue investigation of C2M medium and high loss AUI even our initial assumption that medium (mild) equalizer will not work on of the channels
  - There is strong support in the task force to support C2C+C2M per host PHY with the end-end FEC
  - Even if we have medium and high loss AUIs there is no reason to have different pre-FEC BER
  - If there isn't substantial power saving between medium and high loss AUIs then we should not create two categories of incompatible C2M interface
  - Perhaps the difference between Med/higher power AUI ports is the MLSE which can be turned on/off based per channel as needed
- **Proposed SFEC (128,120) recommend to allocate 5E-5 per host PHY and let the optical PMDs complete their baseline**
  - The electrical adhoc can take the 5E-5 decide how to divide between C2C and C2M
  - Starting point could be by allocating pre-FEC BER of 4E-5 for C2M and 1E-5 to C2C.