

Demonstration of a 224Gbps-PAM4-LR SERDES in Supporting a 1 Meter Passive DAC Long Reach Channel

Mike Li (Intel)
Nathan Tracy (TE)

May 15, 2023

Contributors

Intel:

Ariel Cohen
Cyril Gaillard
Karthik Ghantasala
Cindy Goh
Itai Gur
Ahmad Hajeer
Jeff Hockert
Amir Laufer
Itamar Levin
Yawen Luo
Velkovich Moshe
Ilia Radashkevich

TE:

Tony Daughtry
Justin Pickel
Dustin Rowe
Megha Shanbhag
Rahul Sharma
Kyle Klinger

Background and Introduction

- Intel and TE collaborately demonstrated a 224 Gbps-PAM4-LR end-to-end (E2E) link with Intel SERDES test chip and TE 1 m DAC copper cable at OFC 2023.
- This presentation highlights the demo characteristics and results, and discusses the implications to the 802.3dj 200G/lane C2M, C2C, CR, KR specifications under development.

A 224Gbps-PAM4-LR Demonstration Link System

Intel 224Gbps-PAM4 Long Reach
SERDES TC and boards [1], [2], [3]

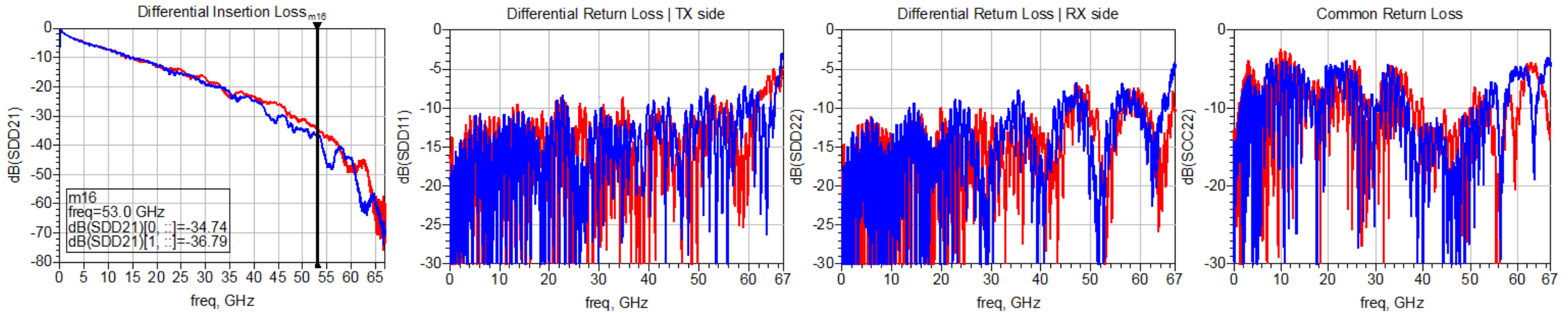
TE OSFP
Connector



TE OSFP
Connector

TE 1 Meter Passive
DAC

A 224Gbps-PAM4-LR E2E Channel Characteristics



— Measured — Simulated

IL: ~36 dB at 53 GHz

RL: ~< 10 dB at 53 GHz

Demonstration at 2023 OFC: Intel Booth, Mar 7-9, San Diego Convention Center, USA



Pre-FEC BER: $3-4e-4$

Summary

- Intel and TE collaborately demonstrated a 224 Gbps-PAM4-LR end-to-end link with Intel SERDES test chip and TE 1 m DAC copper cable at OFC, Mar 2023, and have achieved pre-FEC BER of $3-4e-4$
- It is anticipated that SERDES technology will continue improving in performance and power, and 1 m DAC copper cable will continue improving in performance.
- The demonstrated 224 Gbps-PAM4-LR SERDES technology and 1 m DAC, as well as end-to-end channel, provide solid and helpful momentum in developing 802.3dj 200G/lane C2M, C2C, CR, KR with PAM4 signaling specifications.

References

- [1] Y. Segal, A. Laufer, A. Khairi, Y. Krupnik, M. Cusmai, I. Levin, A. Gordon, Y. Sabag, V. Rahinski, G. Ori, N. Familia, S. Litski, T. Warshavsky, U. Virobnik, Y. Horwitz, A. Balankutty, S. Kiran, S. Palermo, M. Li, A. Cohen, “A 1.41pJ/b 224Gb/s PAM-4 SerDes Receiver with 31dB Loss Compensation”, ISSCC, 2022.
- [2] Khairi A., Krupnik Y., Laufer A., Cusmai M., Segal Y., Levin I., Gordon A., Sabag Y., Rahinski V., Ori G., Familia N., Litski S., Warshavsky T., Virobnik U., Horwitz Y., Lazar D., Balankutty A., Kiran S., Palermo S., Peng M. Li., Cohen A., A 1.41-pJ/b 224-Gb/s PAM4 6-bit ADC-Based SerDes Receiver With Hybrid AFE Capable of Supporting Long Reach Channels. JSSC, 2023.
- [3] J. Kim, S. Kundu, A. Balankutty, M. Beach, B. Kim, S. Kim, Y. Liu, S. Murthy, P. Wali, K. Yu, H. Kim, C. Liu, D. Shin, A. Cohen, Y. Segal, Y. Fan, M. Li, F. O’Mahony, “A 224 Gb/s DAC-Based PAM-4 Quarter-Rate Transmitter with 8-Tap FFE in 10-nm FinFET”, JSSC, 2021.