A 224 Gbps-PAM4 Chip-to-Module Channel for “Universal Port” and Its Characteristics: Design A

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May 15, 2023
Background and Introduction (I)

- An important and common Chip-to-Module (C2M) Channel is the so-called “Universal Port” C2M, as shown in the following diagram.

- The loss of the C2M channel (TP0-TP1A) budget is determined/bounded by the bump-to-bump, ref PKG, and DAC loss budget, which are trending ≤40 dB, ~6 dB, ~16 dB, for 224 Gbps-PAM4 signaling.
Background and Introduction (II)

• We leveraged our established/validated C2M channel design tool-flow-methodology (TFM) (e.g., oif2022.355.00, oif2022.498.00, oif2023.032.00) to create this C2M channel design A to support 224Gbps-PAM4 “Universal Port”.
C2M Channel Design A for “Universal Port”

Component | Insertion Loss TP0-TP1a (dB) @ 56GHz |
---|---|
Host PCB via | 0.85 dB |
Host PCB Trace | 4.5 inch (1.3 dB/inch) |
Connector | 1.62 dB |
HCB | 3.55 dB |
Total | 11.6 dB |
C2M Channel Design A Characteristics (I)

- IL: 11.56dB @ 56GHz
- RL <~11.6dB (<56GHz)
- FEXT < 37.3dB (<56GHz)
- NEXT < 47.5dB (<56GHz)
C2M Channel Design A Characteristics (II)

- ILD < ±1 dB (<56GHz)
- ICR > 25 dB (<56GHz)
C2M Channel Design A Characteristics (III)

[S] parameter BW DC-120GHz

[Graphs showing TDR From Host PCB and TDR From HCB]
Summary

• We have created a C2M channel Design A supporting “Universal Port”
• This C2M channel includes PCB-Via, PCB, connector, and HCB
• This C2M channel has:
  – An IL (TP0-TP1A) of ~11.6 dB at 56 GHz
  – RL <~ 11.6dB at <= 56 GHz
  – FEXT < 37.3dB, NEXT < 47.5dB, at <= 56 GHz
  – PCB IL of 6.58 dB/reach of 4.5 inch (with 1.3 dB/inch) at 56 GHz