A 224 Gbps-PAM4 Chip-to-Module Channel for “Universal Port” and Its Characteristics: Design B

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Background and Introduction (I)

- An important and common Chip-to-Module (C2M) Channel is the so-called “Universal Port” C2M, as shown in the following diagram.

- The loss of the C2M channel (TP0-TP1A) budget is determined/bounded by the bump-to-bump, ref PKG, and DAC loss budget, which are trending \(<=40\, \text{dB}, \sim6\, \text{dB},\) and \(\sim16\, \text{dB}\) for 224 Gbps-PAM4 signaling.
Background and Introduction (II)

• We leveraged our established/validated C2M channel design tool-flow-methodology (TFM) (e.g., oif2022.355.00, oif2022.498.00, oif2023.032.00) to create this C2M channel design B to support 224Gbps-PAM4 “Universal Port”.

C2M Channel Design B for “Universal Port”

<table>
<thead>
<tr>
<th>Component</th>
<th>Insertion Loss TP0-TP1a (dB) @ 56GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Host PCB via</td>
<td>0.85 dB</td>
</tr>
<tr>
<td>Host PCB Trace</td>
<td>3.75 inch (1.3 dB/inch)</td>
</tr>
<tr>
<td>Connector</td>
<td>2.31 dB</td>
</tr>
<tr>
<td>HCB</td>
<td>3.55 dB</td>
</tr>
<tr>
<td>Total</td>
<td>11.6 dB</td>
</tr>
</tbody>
</table>
C2M Channel Design B Characteristics (I)

- IL: 11.63dB @ 56GHz
- RL < ~10.4dB (<56GHz)
- FEXT < 41.7dB (<56GHz)
- NEXT < 41.3dB (<56GHz)
• ILD < +- 1 dB (<56GHz)
• ICR > 27.13 dB (<56GHz)
C2M Channel Design B Characteristics (III)

[S] parameter BW DC-80GHz
Summary

• We have created a C2M channel Design B supporting “Universal Port”
• This C2M channel includes PCB-Via, PCB, connector, and HCB
• This C2M channel has:
  – An IL (TP0-TP1A) of ~11.6 dB at 56 GHz
  – RL <~ 10.4dB at <= 56 GHz
  – FEXT < 41.7dB, NEXT < 41.3dB, at <= 56 GHz
  – PCB IL of 4.9 dB/reach of 3.75 inch (with 1.3 dB/inch) at 56 GHz