224 Gbps-PAM4 Chip-to-Module Link Simulation and Analysis with a “Universal Port” Channel: Design B

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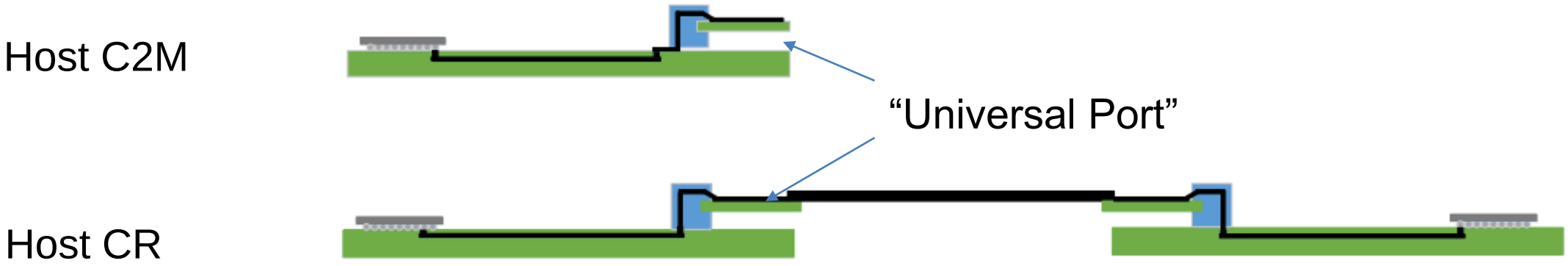
Background and Introduction (I)

- An important and common Chip-to-Module (C2M) Channel is the so-called “Universal Port” C2M, as shown in the following diagram:



- We have created a C2M channel to support “Universal Port” (oif2023.171.00).

Background and Introduction (II)

- We leveraged our established/validated C2M simulation/modeling tool-flow-methodology (TFM) (e.g., oif2022.355.00, oif2022.498.00, oif2023.033.00), and updated reference package (oif2023.172.00, li_3dj_02_2305), to provide link simulation and analysis with this newly created C2M channel Design B.

Preliminary 224Gbps PAM4 COM Analysis

for C2M Channel TP1a Test

- Based on 802.3ck chip-to-module COM with the following changes
  - TP1a COM Test Configuration:
    - Proposed CEI-224G-VSR-PAM4 reference TX
      - RLM = 0.95, SNR_{TX}=33dB, BUJ = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
      - 20%-80% Rise/Fall Time (*T_r*): 4.0ps
      - TX FIR: 4-pre, 1-post
      - TX Die: No change (see oif2022.065.02, mli_3df_01a_220316.pdf)
      - Termination impedance (R_d): 46.25 ohms
      - TX Package:
        - » Z_p = 33mm, Z_{p2} = 1.8mm
        - » γ_0, a_2, *and* C_p *are updated* (see oif2023.172.00, li_3dj_02_2305)
    - TP1a Reference Receiver (Scope)
      - Based on scaled 802.3ck CR/C2M reference RX with DFE (8 fixed, 6 groups of 3 consecutive floating taps up to 60 UI), and Input Referred Noise = $5x10^{-9}$ V^2/GHz
      - Termination impedance (R_d): 46.25 ohms
    - Measurement Window: +/-50mUI
    - DER: 10^{-6}, 10^{-5},and 10^{-4}

Preliminary 224Gbps PAM4 COM Analysis *(cont.)*

for C2M Channel TP1a Test

- Preliminary COM analysis results

DER =10^{-6}

Channel	EH	VEC	COM
CH17	4.49 mV	17.01 dB	1.31 dB

DER

Channel	EH	VEC	COM
CH17	7.53 mV	12.57 dB	2.33 dB

DER

Channel	EH	VEC	COM
CH17	9.27 mV	11.01 dB	3.66 dB

Proposed COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	112	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0 0 0]	nF	[TX RX]
L_s	[.13 .15 .14; 0 0 0]	nH	[TX RX]
C_b	[0.3e-4, 0e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[15 33; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[0 0 ; 0 0]	mm	[test cases]
z_p (FEXT)	[15 33; 1.8 1.8]	mm	[test cases]
z_p (RX)	[0 0 ; 0 0]	mm	[test cases]
C_p	[0.4e-4 0e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=.694
A_fe	0.413	V	vp/vf=.694
A_ne	0.489	V	
L	4		
M	32	Samp/UI	
samples_for_C2M	100	Samp/UI	
T_O	50	mUI	
AC_CM_RMS	0	V	[test cases]
filter and Eq			
f_r	0.5	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.16]		[min:step:max]
c(-3)	[-0.1:0.02: 0]		[min:step:max]
c(-4)	[0:0.02:0.1]		
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	8	UI	
b_max(1)	0.5		**As/dffe1**
b_max(2..N_b)	[0.3 0.2*ones(1,6)]		**As/dfe2..N_b**
b_min(1)	0		**As/dffe1**
b_min(2..N_b)	[-0.3 -0.2*ones(1,6)]		**As/dfe2..N_b**
g_DC	[-20:1:-0]	dB	[min:step:max]
f_z	39.1334731	GHz	
f_p1	59.4511386	GHz	
f_p2	112	GHz	
g_DC_HP	[-6:1:-0]		[min:step:max]
f_HP_PZ	1.4	GHz	
G_Qual	[]	dB	ranges
G2_Qual	[]	dB	ranges
GDC_Min	0	dB	0 disables check. maybe different for each interface.

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_C2M_host_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_eval_	
COM_CONTRIBUTION	0	logical
Local Search	2	
Operational		
VEC Pass threshold	12	db
EH_min	8	mV
ERL Pass threshold	7.3	dB
Min_VEO_Test	0	mV
DER_0	1.00E-06	
T_r	0.004	ns
FORCE_TR	1	5
PMD_type	C2M	
BREAD_CRUMBS	0	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	logical
TDR and ERL options		
TDR	1	logical
ERL	0	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	800	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0.2e-9]	[port1 port2]
TDR_W_TXPKG	1	
N_bx	20	UI
Tukey_Window	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	5.00E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0.0005 0.00089 0.0002]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
ICN & FOM_ILD parameters		
f_v	0.528	*Fb
f_f	0.528	GHz f_r specified in first column
f_n	0.528	GHz
f_2	40	GHz
A_ft	0.600	V
A_nt	0.600	V

Histogram_Window_Weight	Gaussian	gaussian. triangle, rectangle
sigma_r	0.02	sigma in UI fo or gaus.. Wind

Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	407	mm
z_bp (NEXT)	407	mm
z_bp (FEXT)	407	mm
z_bp (RX)	407	mm
C_0	0	nF
C_1	0	nF
Include PCB	0	logical

different for each test fixture

upodated for D3.1

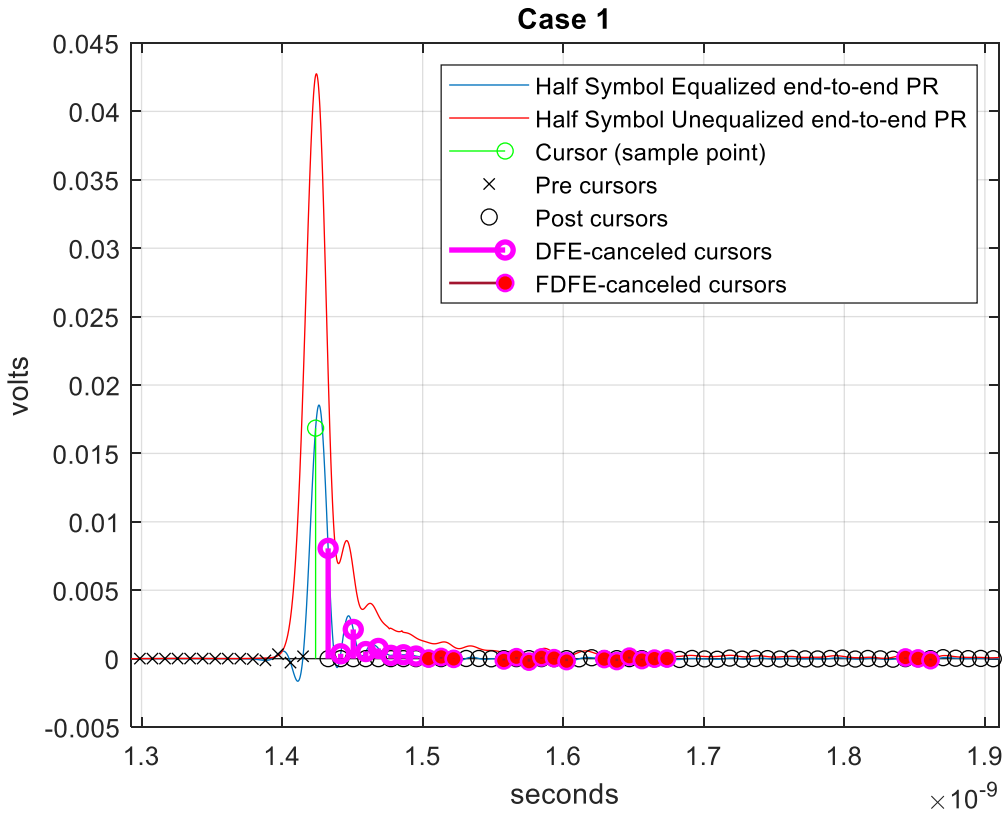
Floating Tap Control		
N_bg	6	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps

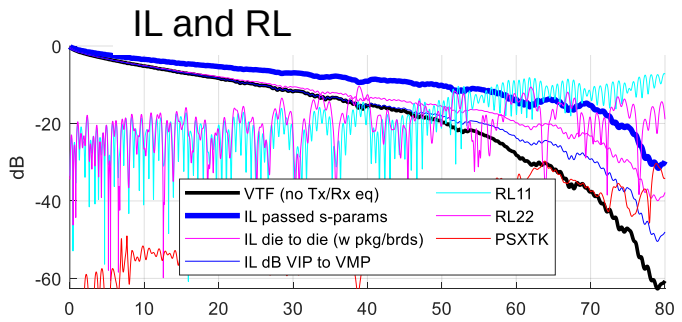
Notes:

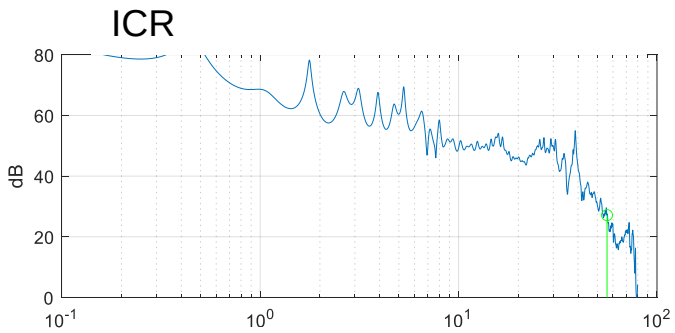
- ***Changes are marked in yellow.***
- ***COM v4.0 was used in this study.***

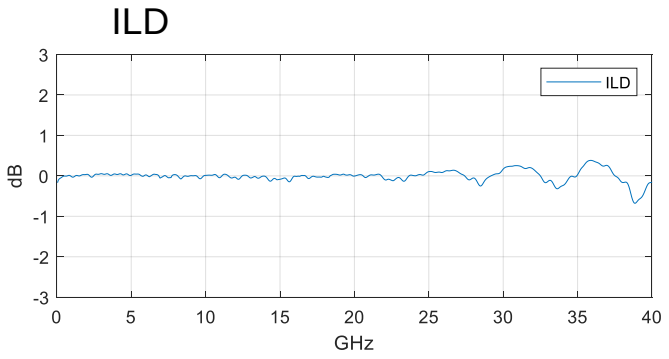
Preliminary 224Gbps PAM4 COM Analysis (CH17)

TP1a

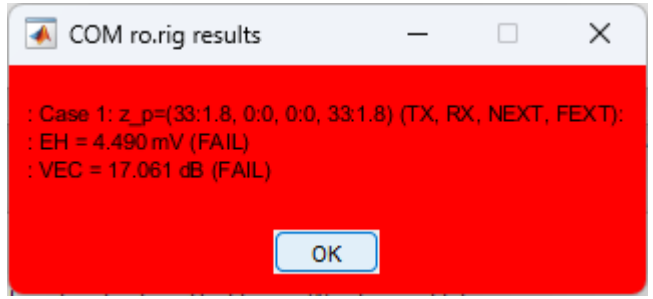




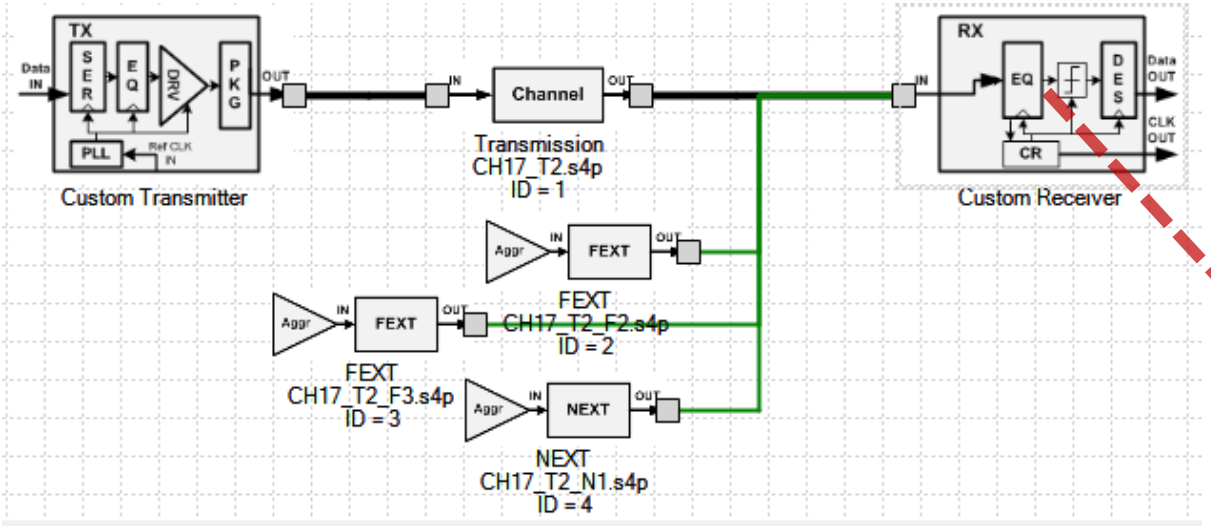


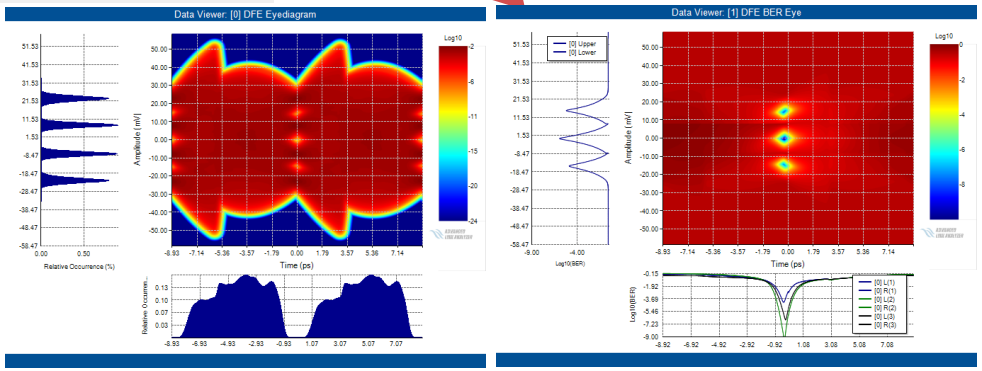


- DFE Taps = 8 + 6x3
- EH = 4.49 mV
- VEC = 17.06dB
- DER = 1e-6
- COM = 1.31dB



224Gbps PAM4 C2M TP1a Time-Domain Simulation (CH17)





TP1a RX output
EH = 1.16mV, EW = 0.03UI VEC = 16.28dB
@ DER=1e-6

Simulation Configuration

- Test Pattern: QPRBS13-CEI
- Transmitter: Proposed CEI-224G-VSR-PAM4 reference TX, die, and package
  - RLM = 0.95, SNR_{TX}=33dB, BUJ = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
  - 20%-80% Rise/Fall Time (*T_r*): 4ps
  - Termination impedance (R_d): 46.25 ohms
  - TX Package:
    - Zp = 33mm, Zp2 = 1.8mm
    - Γ0 a2, and Cp also updated (see COM table)
- TP1a Reference Receiver (Scope)
  - Based on scaled 802.3ck CR/C2M reference RX with DFE (8 fixed and 6 groups of 3 consecutive floating taps up to 60 UI), and Input Referred Noise = 5x10^{-9} V^2/GHz*
  - Termination impedance (R_d): 46.25 ohms
- Channel: C2M channel with 2 FEXTs and 1 NEXT
- DER = 10^{-6}

*Notes: *: RX optimizes signal-to-noise-and-distortion ratio for CDR and EQ.*

COM Analysis and Link Simulation Results Summary & Observations

DER	Channel	COM EH	COM VEC	Simulation Eye Opening Height	Simulation VEC
10^{-6}	CH17	4.49 mV	17.01 dB	1.16 mV	16.28 dB
10^{-5}	CH17	7.53 mV	12.57 dB	2.55 mV	12.63 dB
10^{-4}	CH17	9.27 mV	11.01 dB	4.41 mV	9.45 dB

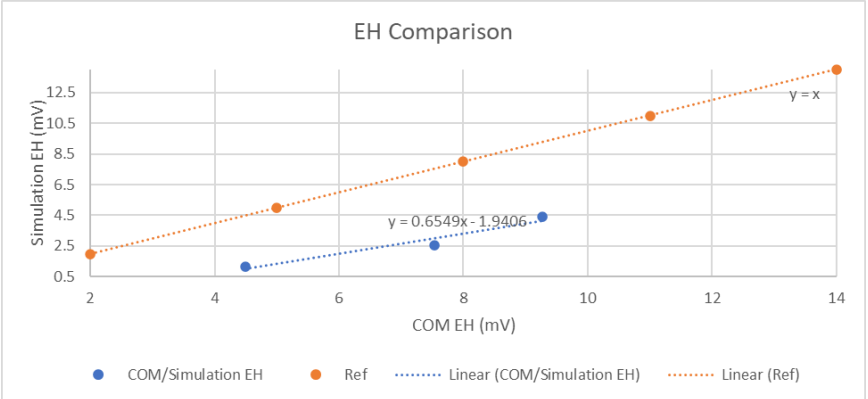
Correlations between COM and Link Simulations (CH17)

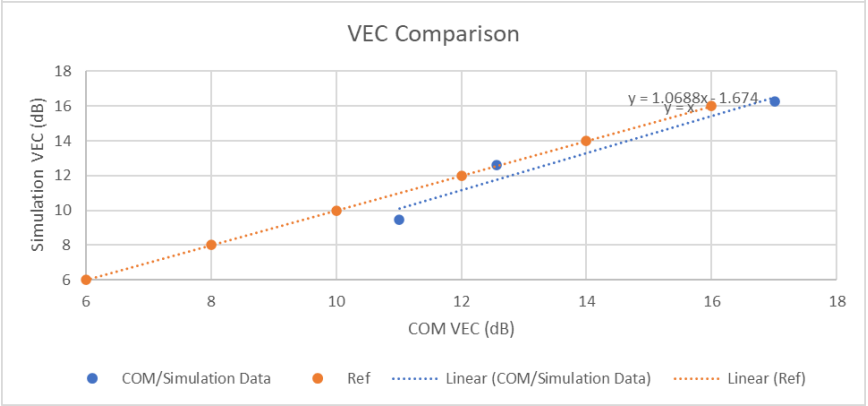
- Link simulations and COM analysis shown to choose different EQ settings, which led to EH and VEC results differences, due to:
  - Optimization method
  - COM is SBR-based and mostly LTI while link simulations include nonlinear effects such as level mismatch, jitter amplifications, burst errors, … etc.
  - COM assumes constant noise SNR across the link while noises are shaped by channel/device in link simulations.

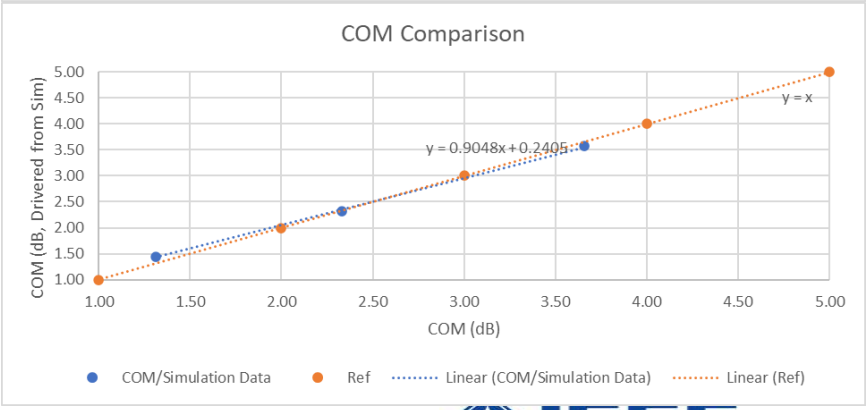
- However, when comparing the COM values from COM analysis and link simulation results*, good correlations were observed.

*Note: *: COM value can be derived from link simulation's VEC values through OIF CEI Eq. 23-20:*

$$VEC = -20\ log_{10}\left(1 - 10^{\frac{-COM}{20}}\right)$$







Summary and Next Steps

- Reasonable solution can be found for this C2M “Universal Port” Tp0-TP1A channel (Design B) for DER < 1e-5.
- Future works including TP4 short and long channel design, simulation and analysis, for C2M specification development.