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# 200Gbps/Lane AUI C2C Considerations

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IEEE P802.3dj Task Force

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# Supporter

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- **Richard Mellitz – Samtec**
- **Rick Rabinovich – Keysight Technologies**

# Outline

- ❑ **AUI BER Status Recap**
- ❑ **C2C Technical Considerations**
- ❑ **Example of COM Parameters**
- ❑ **Proposed Straw Poll**

# Introduction

- **Current focus of AUI BER targets**
  - Trade-off between AUI BER limit and PMD BER limit
  - Relationships among C2M BER realistic, C2M channel characteristics, and the C2M TX/RX complexity
- **Requirement of compatible host BER budgets for both optic and DAC to support “universal switch port”**
- **This presentation will discuss the work and decisions needed to progress C2C interface type towards a baseline proposal**

## Straw Poll #1 and 2 -- directional

At this time, I prefer the 200 Gbps/lane AUI BER target option per brown\_3dj\_elec\_01\_230420 slide 18:

- Option A: C2M and C2C AUI BER 1E-5
- Option B: C2M and C2C AUI BER 2E-5
- Option C: C2M and C2C AUI BER 5E-5
- Option D: C2M and C2C AUI BER 1E-4
- Option E: C2M AUI BER 8E-5 and C2C AUI BER 2E-5

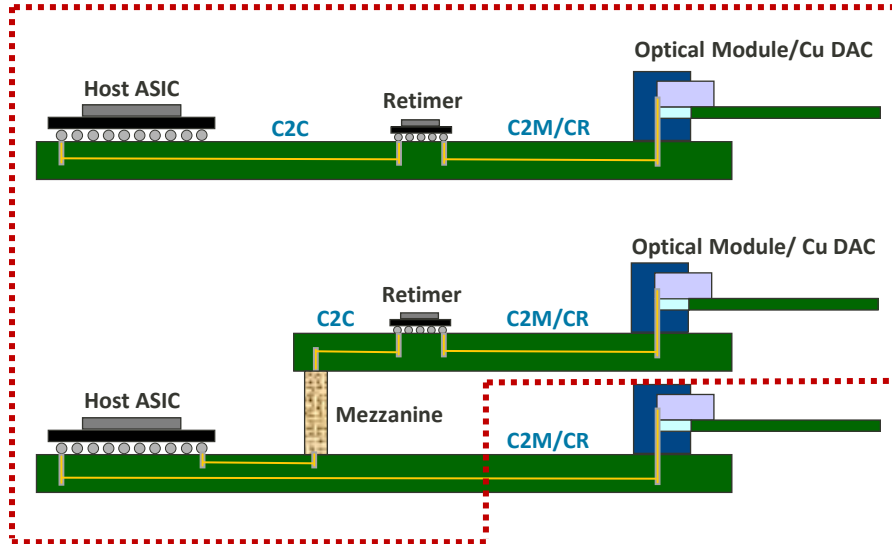
SP#1 Results (Chicago rules): A: 29 B: 19 C: 25 D: 8 E: 24

SP#2 Results (Choose one): A: 12 B: 4 C: 17 D: 0 E: 12 NMI: 11

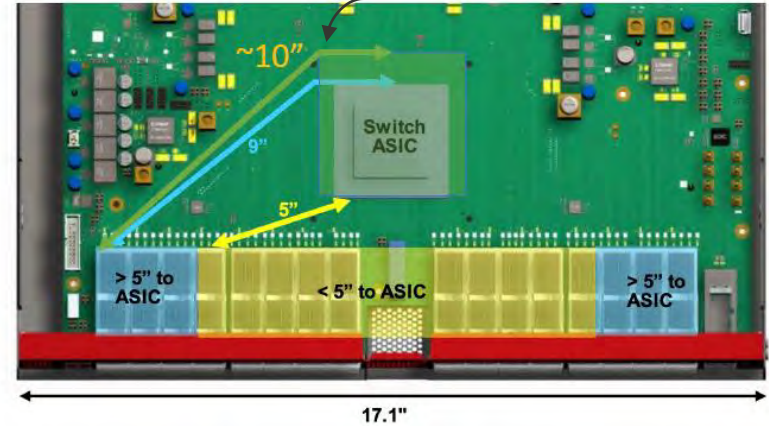
[https://www.ieee802.org/3/dj/public/adhoc/electrical/23\\_0420/straw\\_polls\\_3df\\_elec\\_adhoc\\_230420.pdf](https://www.ieee802.org/3/dj/public/adhoc/electrical/23_0420/straw_polls_3df_elec_adhoc_230420.pdf)

# Common C2C Applications

- Extend pluggable module range
  - Requirement of up to 10" electrical trace for 51.2T switch with ~90x90 package per recommendation [ghiasi\\_3df\\_01\\_2211](#)
- Support mezzanine card



Require either intermediate retimers or intra-box cabling

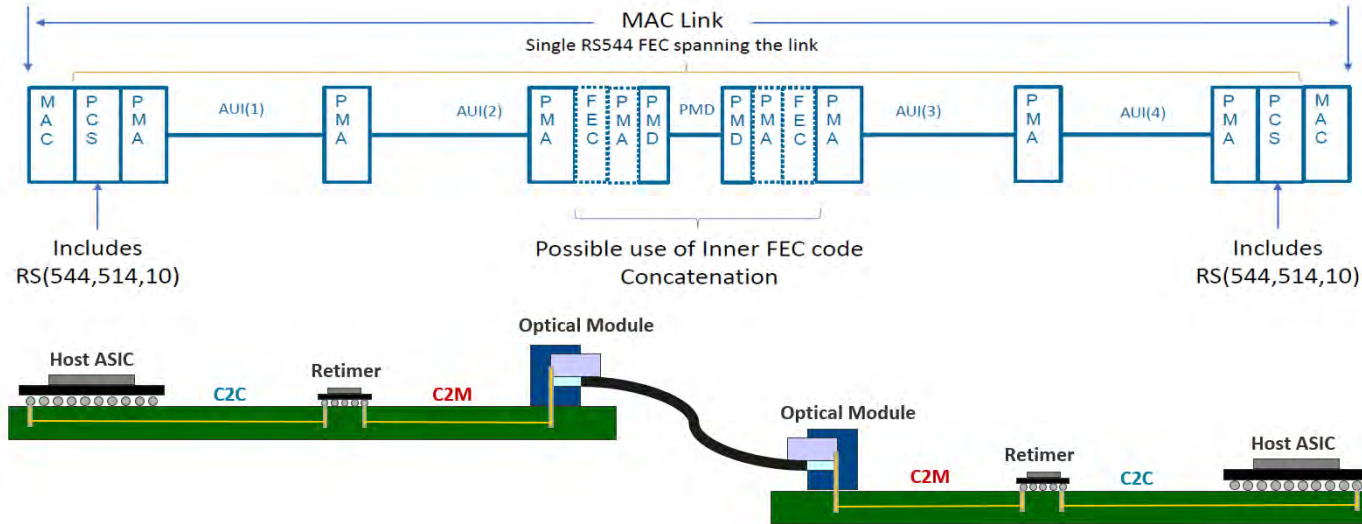


Retimer in the path for

- Optical ports: At least two AUIs (C2C+C2M) required
- Copper ports: At least one AUI C2C required

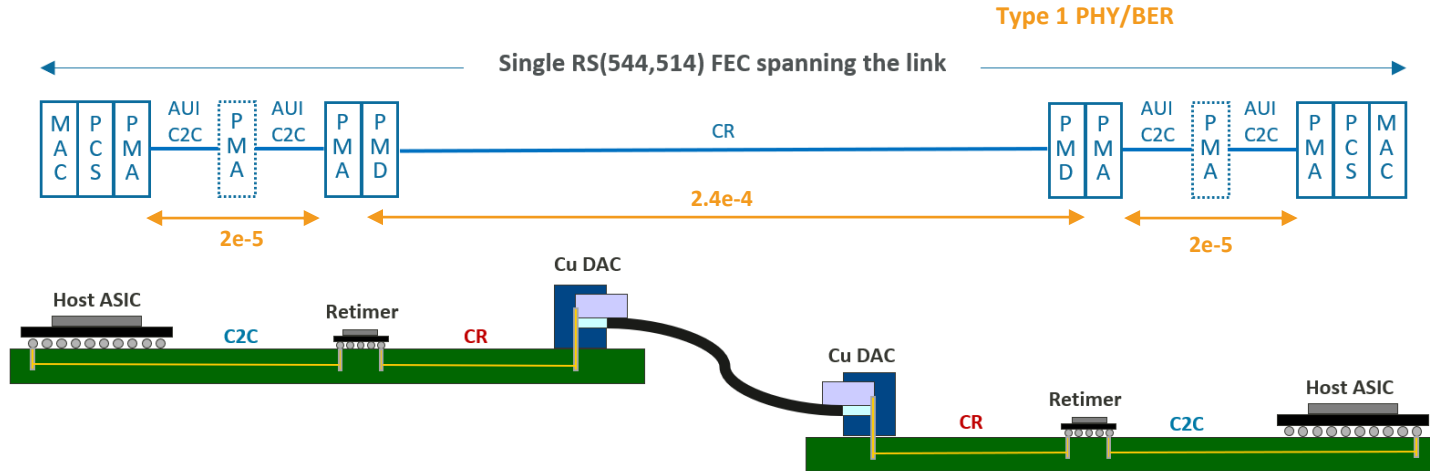
# C2C BER Consideration: ASIC-CDR Interconnection

Source: [gustlin\\_3dj\\_01\\_2303](#)



- Trade-off between AUI BER limit and PMD BER limit have been illustrated in [he\\_3df\\_01\\_2211](#) and [ran\\_3dj\\_elec\\_01\\_230420](#)
- MAC link latency in according to the choice of FEC architecture have been compared in [brown\\_3dj\\_optx\\_01b\\_230413](#)
- **C2C AUI BER > 1E-5 should be supported by Type 2 or Type 3 PHY**
  - AUI BER target (per segment) <= 2E-5 can only allow up to 1 AUI per Type 1 PHY → Retimerless!!

# C2C BER Consideration: ASIC-ASIC Interconnection

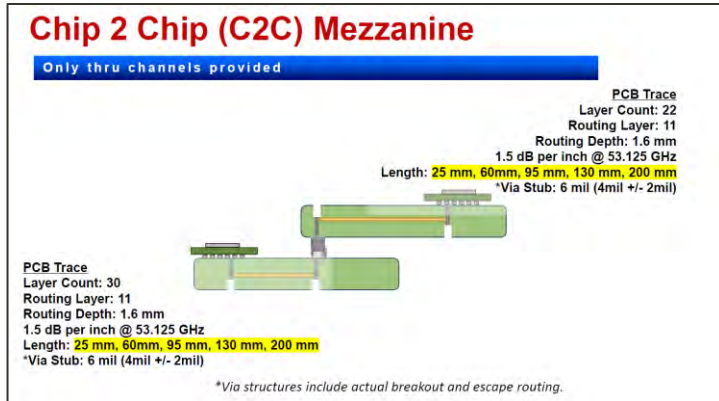
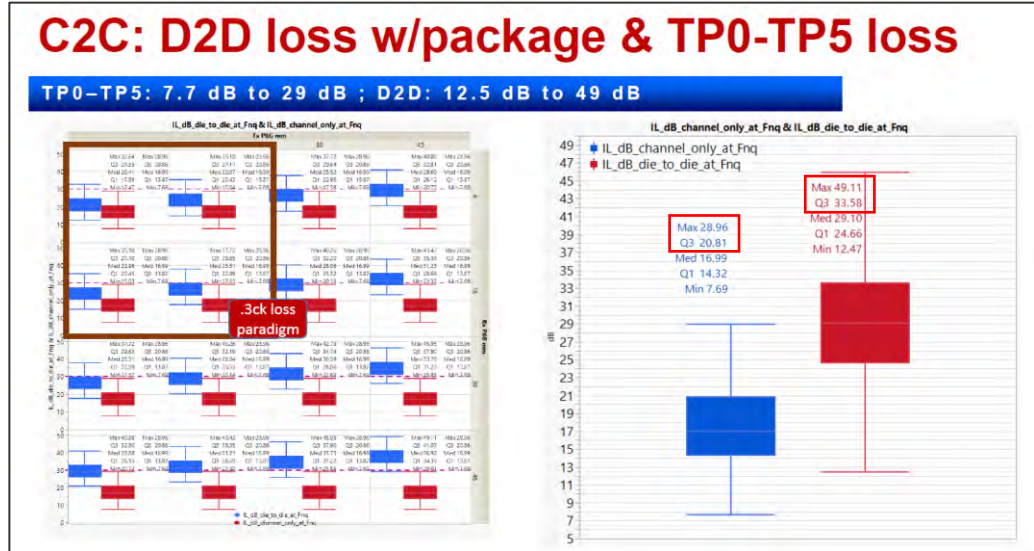


- **C2C AUI BER  $\leq 2E-5$  can be supported by Type 1 FEC**
  - BER target  $\leq 1E-5$ : Up to 2 AUI C2C per Type 1
  - BER target  $\leq 2E-5$ : Up to 1 AUI C2C per Type 1
- **Implement inner FEC at retimer may not be helpful**
  - Increasing coding gain will accelerate data-rate requirement, especially for electrical interfaces

**C2C AUI BER  $\leq 1E-5$  is recommended to support "universal port", otherwise FEC termination required**

# C2C Mezzanine Channel Topology

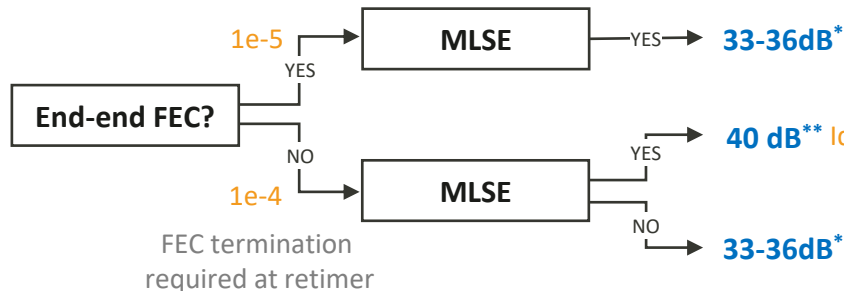
- C2C construction based on PCB and one Mezzanine connector taken from [mellitz\\_3dj\\_04\\_2303](#) and [mellitz\\_3dj\\_elec\\_01\\_230504](#)
  - Electrical interconnect up to 400mm
  - TP0-TP5 loss ~20.x dB with a total length of 260mm
- 802.3ck: TP0-TP5 loss 20 dB with a total length of 250mm





# C2C Loss Consideration

- TP0-TP5 IL range from 7.7 to 29 dB with 50-400mm reach shown in [mellitz\\_3dj\\_elec\\_01\\_230504](#)
- Package loss assumptions for 200G high radix applications
  - [benartsi\\_3df\\_01a\\_2211](#) uses best ABF conventional construction to lower package loss to 8+ dB
  - [ghiasi\\_3df\\_01\\_220927](#) suggests using wider traces to give us the path to 6 dB package loss
  - [li\\_3dj\\_02\\_2305](#) extracts a reference package model from the test package with ~6 dB loss
- C2C interface complexity will be somewhere between C2M and KR/CR
- C2C die-die loss and equalization complexity would probably like...



\* Bump-Bump IL estimated based on [li\\_3dj\\_01a\\_2303](#)

\*\* Bump-Bump IL estimated based on [mellitz\\_3dj\\_elec\\_04a\\_230504](#)

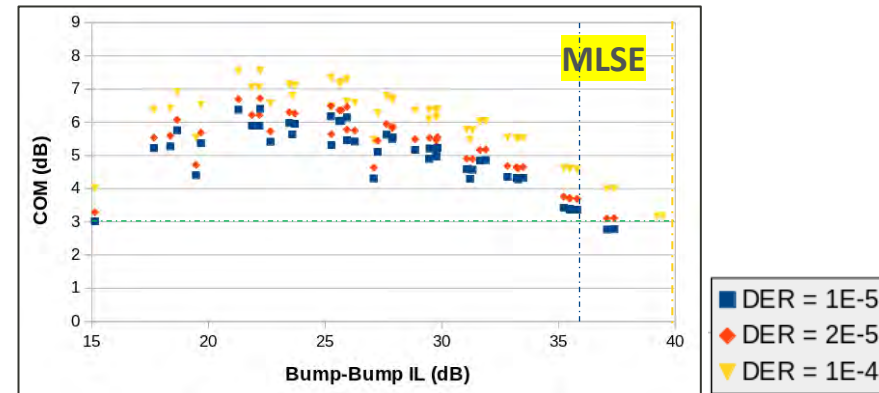
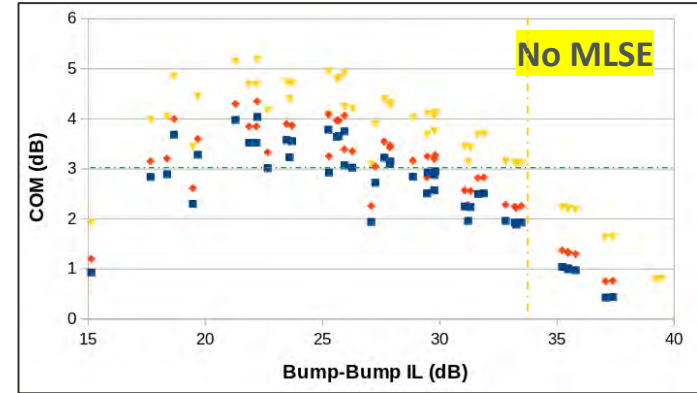
# COM Simulation

- Test channels (25x): [mellitz\\_3dj\\_elec\\_01\\_230504](#)
- COM 4.0 used, COM spreadsheet in [appendix](#)

Parameter	802.3ck C2C	802.3ck KR	Exploratory of 802.3dj C2C
DER_0	1E-5	1E-4	1E-5/2E-5/1E-4
SNR_TX	33	33	33
R_LM	0.95	0.95	0.95
TxFIR Length	5 (3 pre)	5 (3 pre)	6 (4 pre)
eta_0	2E-08	8.2E-09	8.2E-09
N_b	6	12	24
N_bg	0	3	6
N_bf	-	3	3
N_f	-	40	80
MLSE	0	0	0, 1

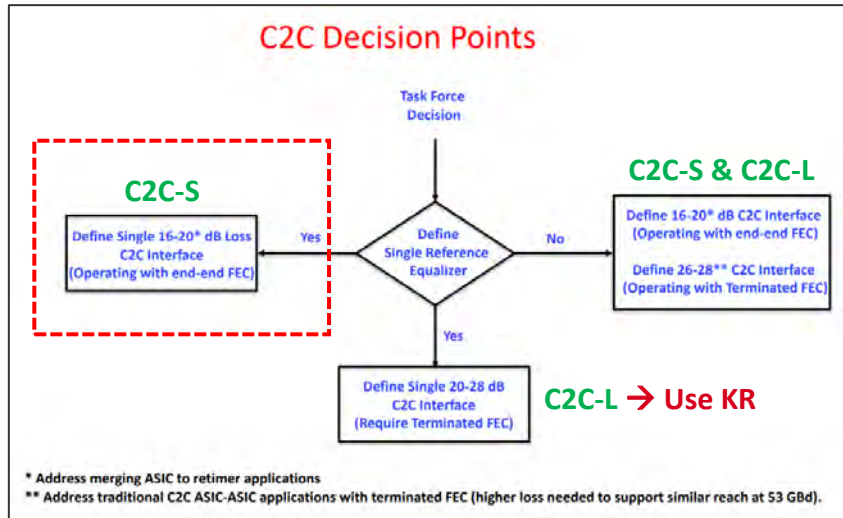
\* Changes from 802.3ck C2C are marked in green

- This is NOT parameters proposal
  - Example parameters give > 3dB COM for direction finding



# How to Proceed

- 802.3ck C2C direction recap
  - [ghiasi\\_3ck\\_01\\_0719](#) addressed C2C applications with 2 classes of BER, Loss, and equalizer complexity
  - Straw Poll #5 secured direction on the proposed C2C baseline without exceeding “end-end FEC” capability, see [lusted\\_3ck\\_02\\_0719](#)



## Straw Poll #5:

I would support the proposed C2C “no FEC termination” parameters in [lusted\\_3ck\\_02\\_0719](#), slide 10 as an initial target for investigation

Y: 43 , N: 0 , A: 5

## Straw Poll #6:

I would support continuing to explore another C2C case (appx 26-28 dB IL and segmented FEC) in addition to the C2C “no FEC termination” from Straw Poll #5

Y: 6 , N: 22 , A: 12

[https://www.ieee802.org/3/ck/public/19\\_07/minutes\\_3ck\\_0719.pdf](https://www.ieee802.org/3/ck/public/19_07/minutes_3ck_0719.pdf)

# Proposed Straw Poll

- I would support a C2C baseline operating without FEC termination, as illustrated in lit\_3dj\_01a\_2305, slide 7 as the initial target for investigation
- Y/N/A

# Appendix

# Example COM Configuration for 200G/L C2C

Table 93A-1 parameters				I/O control				Table 93A-3 parameters			
Parameter	Setting	Units	Information	DIAGNOSTICS				Parameter	Setting	Units	
f_b	106.25	GHz		0		logical		package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]		
f_min	0.05	GHz		DISPLAY_WINDOW	0	logical		package_tl_tau	0.00644805	ns/mm	
Delta_f	0.01	GHz		CSV_REPORT	0	logical		package_z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
C_d	[0.4e-4 0.9e-4 1.1e-4; 0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]	RESULT_DIR	.\results\CARR_[date]\	logical					
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]	SAVE_FIGURES	0	logical					
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	Port Order	[ 1 3 2 4 ]						
z_p_select	[1, 2]		[test cases to run]	RUNTAG	CARR_RCoS_eval						
z_p (TX)	[13 31; 1 1 : 1 1 ; 0.5 0.5]	mm	[test cases]	COM_CONTRIBUTION	0	logical		board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G	
z_p (NEXT)	[11 29; 1 1 : 1 1 ; 0.5 0.5]	mm	[test cases]	Operational				board_tl_tau	5.790E-03	ns/mm	
z_p (FEXT)	[13 31; 1 1 : 1 1 ; 0.5 0.5]	mm	[test cases]	ERL Pass threshold	9.7	dB		board_z_c	100	Ohm	
z_p (RX)	[11 29; 1 1 : 1 1 ; 0.5 0.5]	mm	[test cases]	COM Pass threshold	3	db		z_bp (TX)	125	mm	
PKG_Tx_FFE_preset	0			DER_0	1.00E-05			z_bp (NEXT)	0	mm	
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]	T_r	3.75E-03	ns		z_bp (FEXT)	125	mm	
R_0	50	Ohm		FORCE_TR	1	logical		z_bp (RX)	0	mm	
R_d	[50 50]	Ohm	[TX RX]	PMD_type	C2C			C_0	[0.2e-4 0]	nF	
A_v	0.413	V	sp/xf=	EW	1			C_1	[0.2e-4 0]	nF	
A_fj	0.413	V	sp/xf=	TDR and ERL options		logical		Include PCB	0	logical	
A_ng	0.45	V	sp/xf=	TDR	1	logical					
L	4			ERL	1	logical		Selections (rectangle, gaussian, dual, gy, high, triangle)			
M	32			ERL_ONLY	0	ns		Histogram_Window_Weight	g2u8Jan	selection	
Filter and Eq				TR_TDR	0.01			Qr	0.02	UI	
f_r	0.75	*fb		N	2000	logical					
c(0)	0.54	min		TDR_Butterworth	1						
c(-1)	[-0.34; 0.02; 0]	[minstep; max]		beta_x	0			ICH parameters			
c(-2)	[0.02; 0.12]	[minstep; max]		rho_x	0.618			f_v	0.594	Fb	
c(-3)	[-0.06; 0.02; 0]	[minstep; max]		TDR_W_TXPKG	0	UI		f_f	0.594	Fb	
c(-4)	0	[minstep; max]		N_bx	12			f_n	0.594	Fb	
c(1)	[-0.12; 0.02; 0.1]	[minstep; max]		fixture delay time	[ 0 0 ]			f_2	79.688	GHz	
N_b	24	UI		Tukey_Window	1			A_ft	0.450	V	
b_max(1)	0.85	As/die1		Noise_jitter		UI		A_nt	0.450	V	
b_max(2..N_b)	[0.5 0.3 0.3 0.2 *ones(1,20)]	As/die2..N_b		sigma_RJ	0.01	UI		Floating Tap Control			
b_min(1)	0.3	As/die1		A_DD	0.02	V <sup>2</sup> /GHz		N_bg	6	0 1 2 or 3 groups	
b_min(2..N_b)	[0.2 0.05 0.05 -0.05 *ones(1,20)]	As/die2..N_b		eta_0	8.20E-09	db		N_bf	3	taps per group	
g_DC	[-20; 1; 0]	dB	[minstep; max]	SNR_TX	0			N_f	80	UI span for floating taps	
f_z	42.5	GHz		R_LM	0.95			bmaxg	0.2	max DFE value for floating taps	
f_p1	42.5	GHz		Enforce Causality	1						
f_p2	106.25	GHz		S-parameter magnitude extrapolation policy	trend to DC			MUSE	1	logical	
g_DC_HP	[-6; 1; 0]		[minstep; max]					Receiver testing			
f_HP_PZ	1.328125	GHz		Filter: Rx/FFE				RX_CALIBRATION	0	logical	
Butterworth	1	logical	include in fr	frc_pre_tap_len	0	UI		Sigma BBN step	5.00E-03	V	
Raised Cosine	0	logical	include in fr	frc_post_tap_len	0	UI					
RC_Start	6.70E+10	Hz	start freq for RCoS	frc_tap_step_size	0						
RC_end	7.97E+10	Hz	end freq for RCoS	frc_main_cursor_min	0.7						
				frc_pre_tap1_max	0.7						
				frc_post_tap1_max	0.7						
				frc_tapn_max	0.7						
				frc_backoff	0						

**Thank you**

**Questions and Discussions**