200 Gb/s per lane KR Backplane Objective Proposal

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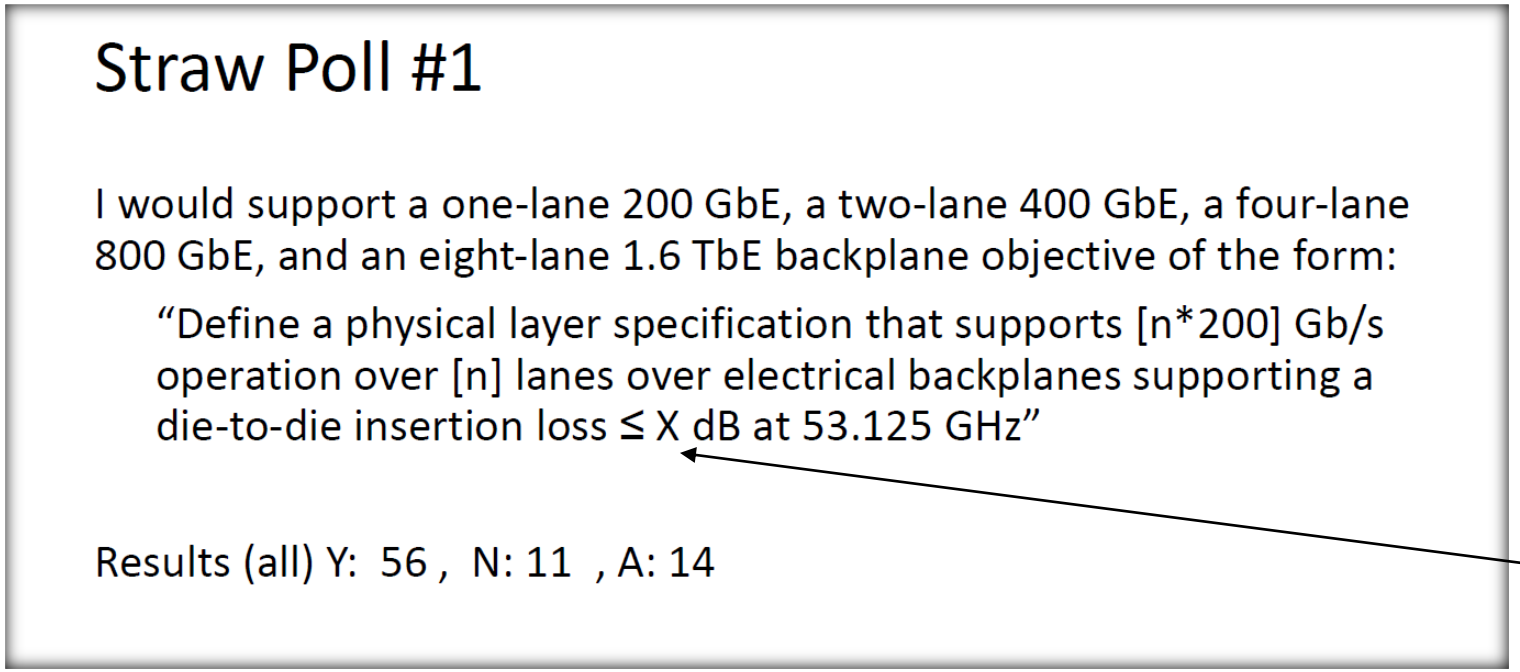
Presentation Goal

MOTIONS_3DFDJ_2303

- Propose a value for "X" in straw poll #1 (motions_3dfdj_2303)

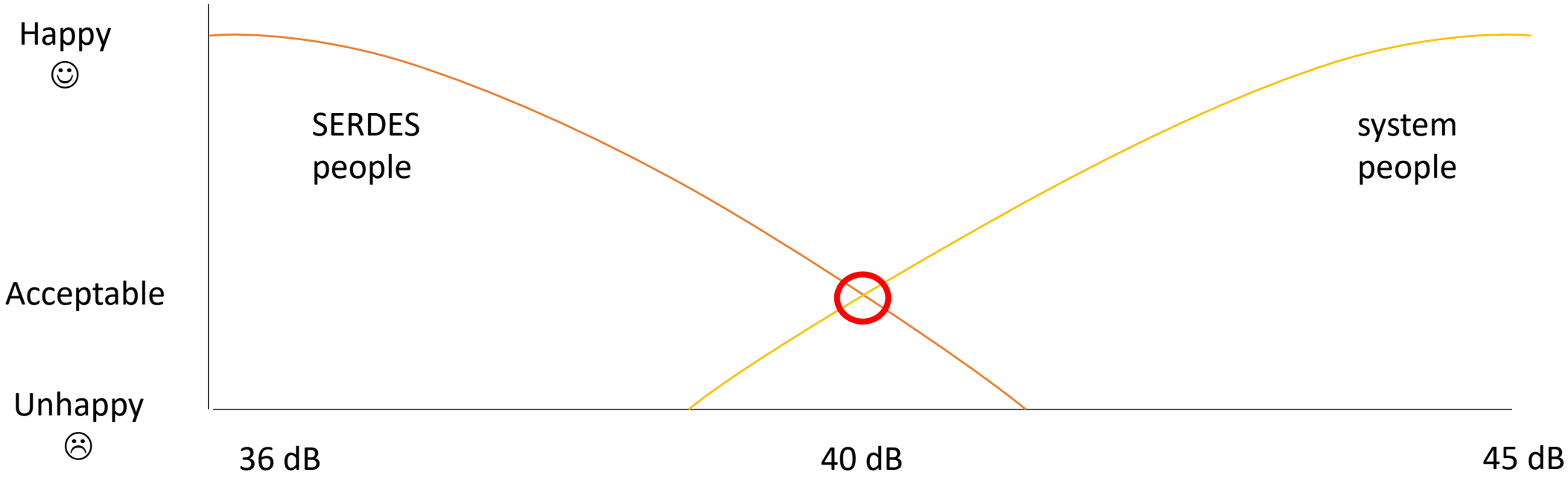


X = 40

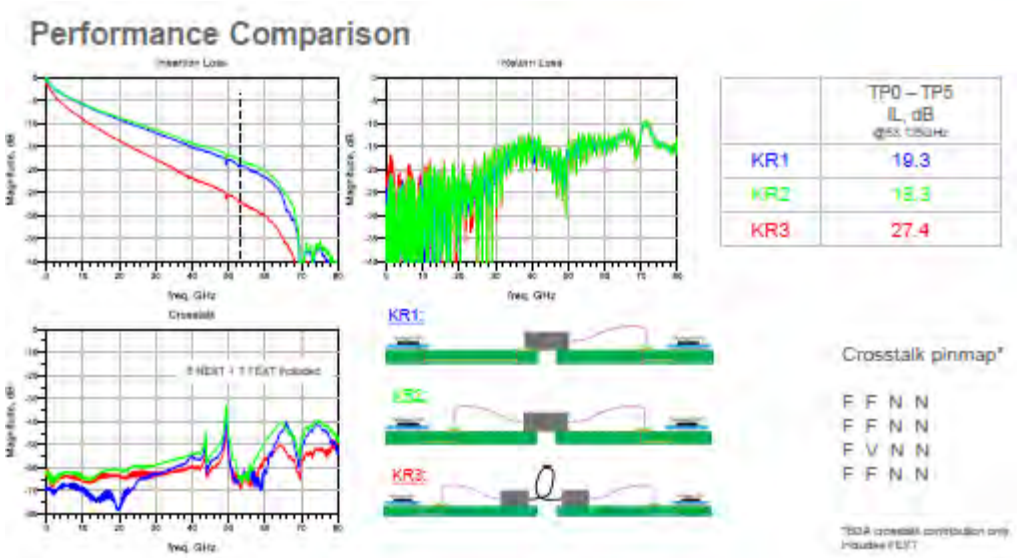
Why 40 dB?

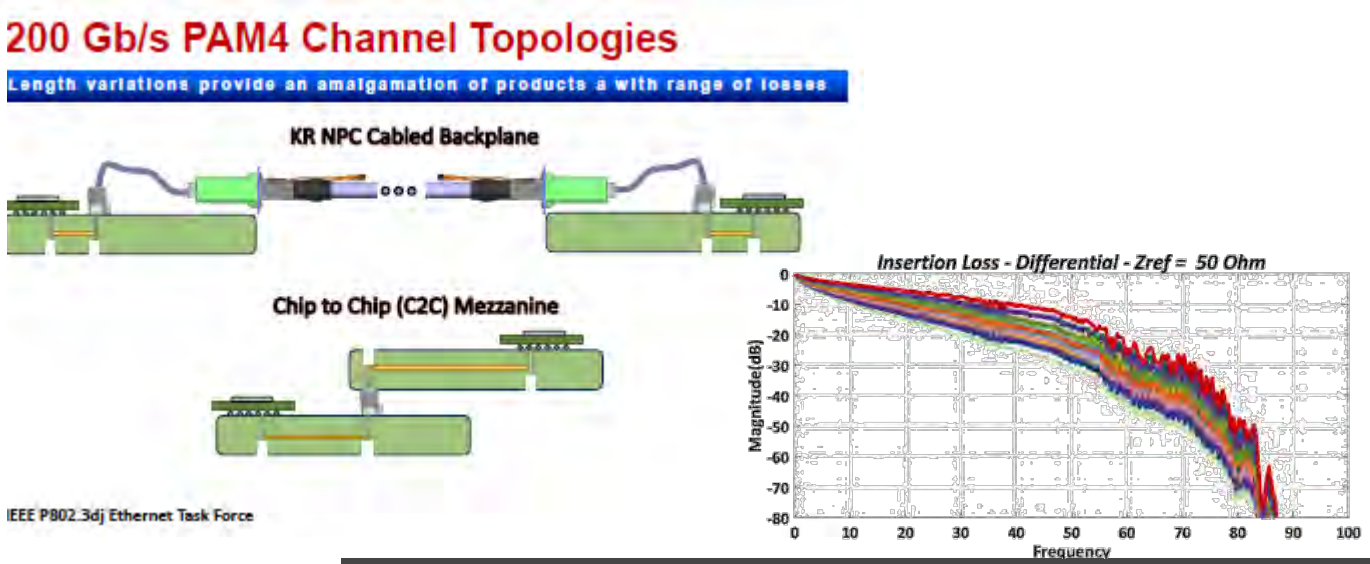
COMPROMISE!!!!

- Feedback from people building SERDES: 36-37dB IL target
- Feedback from people building systems: 42-45 dB IL target

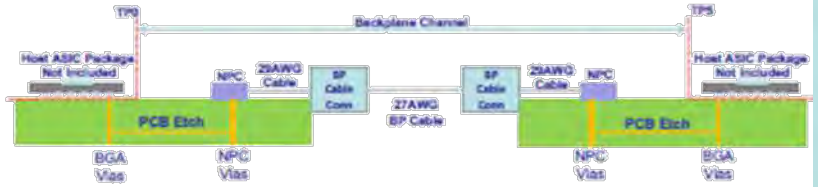


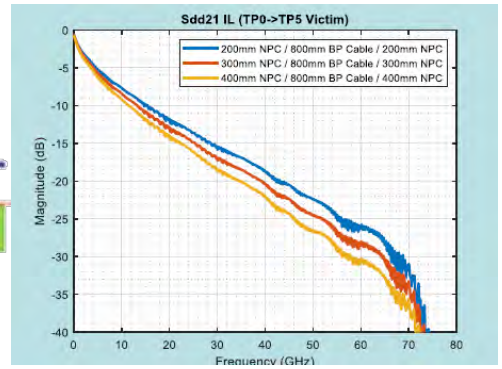
Feasibility based on P802.3dj contributions illustrate a variety of 200 G KR configurations





- Simulation of a typical KR cabled backplane architecture over various cable lengths
- Contributions:
  - BGA / PCB trace / NPC via escapes simulated with HFSS
  - NPC + BP cable assemblies: provided by Michael Rowlands, affiliated with Amphenol
- Ball-to-Ball topology: does not include package effects
- This presentation does NOT propose the following:
  - Specific aggregate or cable losses
  - Specific host architecture implementations





Summary of KR reaches are up to

- ❑ 1 meter for a cabled backplane
- ❑ 300 mm of cable on a host plus a few inches for break out
  - Or between 5 to 7 inches of host PCB trace
- ❑ Subset of KR may include
  - orthogonal box designs
  - chip to chip

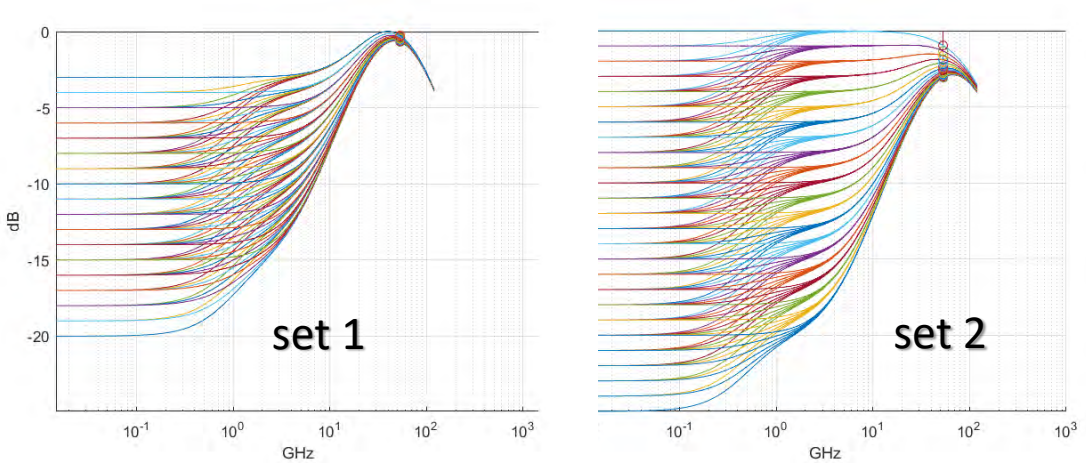
Details in References on slide 11

Example parameters sets which suggest > 3 dB COM feasibility for "X" = 40 dB

THIS IS NOT A PARAMETER PROPOSAL

parameter	Used for this work set 1	Used for this work set 2
η_0 [V²/GHz]	4e-9	5e-9
SNR_Tx	33	33
t_r [ps]	4	4
f_r	0.58	0.5
b_{max}	0.75	0.85
DFE equivalent [Taps]	1	1
Tx FFE Pre/Post	4/1	4/1
Rx FFE pre/post cursor	6/60	6/24
FFE floating groups/ floating taps per group*	NA	4/5
DER_0	1e-4	1e-4
MLSE used	yes	yes

* RX FFE floating taps estimated in COM 4.0 with RX DFE floating taps in the presentation



parameter	Used for this work set 1	Used for this work Set 2
fz	fb/4.223	fb/2.5
fp1	fb/2.6562	fb/2.5
fp2	Fb/1.8973	Fb
fLF	Fb/80	Fb/160
Gdc	-15 to 0-3 (step 1)	-20 to 0 (step 1)
Gdc2	-5 to 0 (step 1)	-6 to 0 (step 1)

Example 200 Gb/s KR COM configuration set 1

Packages were adjusted to achieve around 40 dB die to die loss

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.386	V	vp/vf=
A_fe	0.386	V	vp/vf=
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.58	*fb	
c(0)	0.55		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	0.15		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15	S	As/dfe2..N_b
g_DC	[-15:1:-3]	dB	[min:step:max]
f_z	25.16	GHz	
f_p1	40.00	GHz	
f_p2	56.00	GHz	
g_DC_HP	[-5:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CACR_set1_{date}\	
SAVE_FIGURES	0	logical
Port Order	**[1 3 2 4]**	
RUNTAG	KR_se1_eval_	
COM_CONTRIBUTION	1	logical
Operational		
ERL Pass threshold	10	dB
COM Pass threshold	3	db
DER_0	1.00E-04	
T_r	0.00400	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
MLSE	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	1000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	20	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	4.00E-09	dB
SNR_TX	33	
R_LM	0.95	

Table 93A–3 parameters			
Parameter	**Setting**	**Units**	Information
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]		
package_tl_tau	0.00644805	ns/mm	
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
z_p select	[1:10]		[test cases to run]
z_p (TX)	[6 31 ; 1 1; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[8 29 ; 1 1; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[6 31 ; 1 1; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 29 ; 1 1; 1 1 ; 0.5 0.5]	mm	[test cases]
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
Floating Tap Control			
N_bg	**0**	0 1 2 or 3 groups	
N_bf	3	taps per group	
N_f	80	UI span for floating taps	
bmaxg	0.2	max DFE value for floating taps	
B_float_RSS_MAX	0.1	rss tail tap limit	
N_tail_start	25	(UI) start of tail taps limit	
Filter: Rx FFE			
ffe_pre_tap_len	**6**	UI	
ffe_post_tap_len	60	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	1		
ffe_pre_tap1_max	1		
ffe_post_tap1_max	1		
ffe_tapn_max	1		
ffe_backoff	0		

Example 200 Gb/s KR COM configuration set 2

Packages were adjusted to achieve around 40 dB die to die loss

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.5	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.16]		[min:step:max]
c(-3)	[-0.1:0.02:0]		[min:step:max]
c(-4)	[0:.02:0.1]		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.3 -0.2*ones(1,22)]	S	As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.50	GHz	
f_p1	42.50	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_set2_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_set2_eval_	
COM_CONTRIBUTION	1	logical
Operational		
ERL Pass threshold	10	dB
COM Pass threshold	3	db
DER_0	1.00E-04	
T_r	0.004	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
MLSE	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	3500	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	21	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	5.00E-09	dB
SNR_TX	33	
R_LM	0.95	

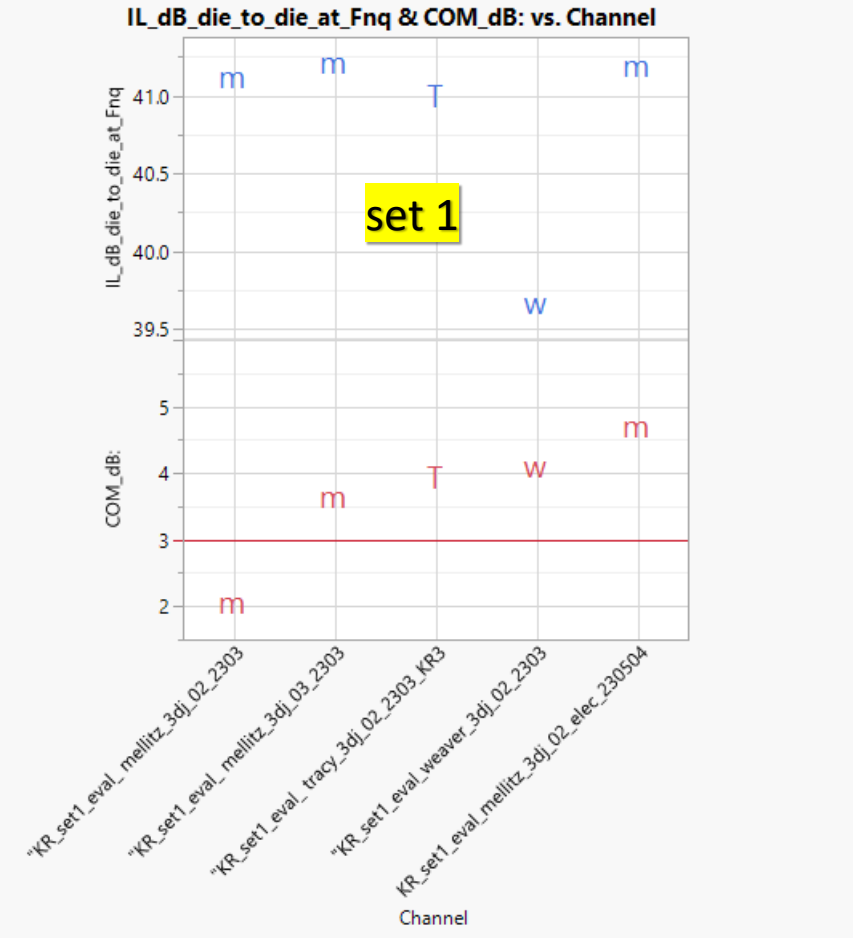
Table 93A–3 parameters			
Parameter	**Setting**	**Units**	**Information**
package_tl_gamma0_a1_a2	[0.0005 0.00089 0.0002]		
package_tl_tau	0.006141	ns/mm	
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm	
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 42; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 40; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 42; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 40; 1.8 1.8]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
Floating Tap Control			
N_bg	4		0 1 2 or 3 groups
N_bf	5		taps per group
N_f	60		UI span for floating taps
bmaxg	0.05		max DFE value for floating taps
B_float_RSS_MAX	0.02		rss tail tap limit
N_tail_start	50		(UI) start of tail taps limit
Filter: Rx FFE			
ffe_pre_tap_len	6	UI	
ffe_post_tap_len	24	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		

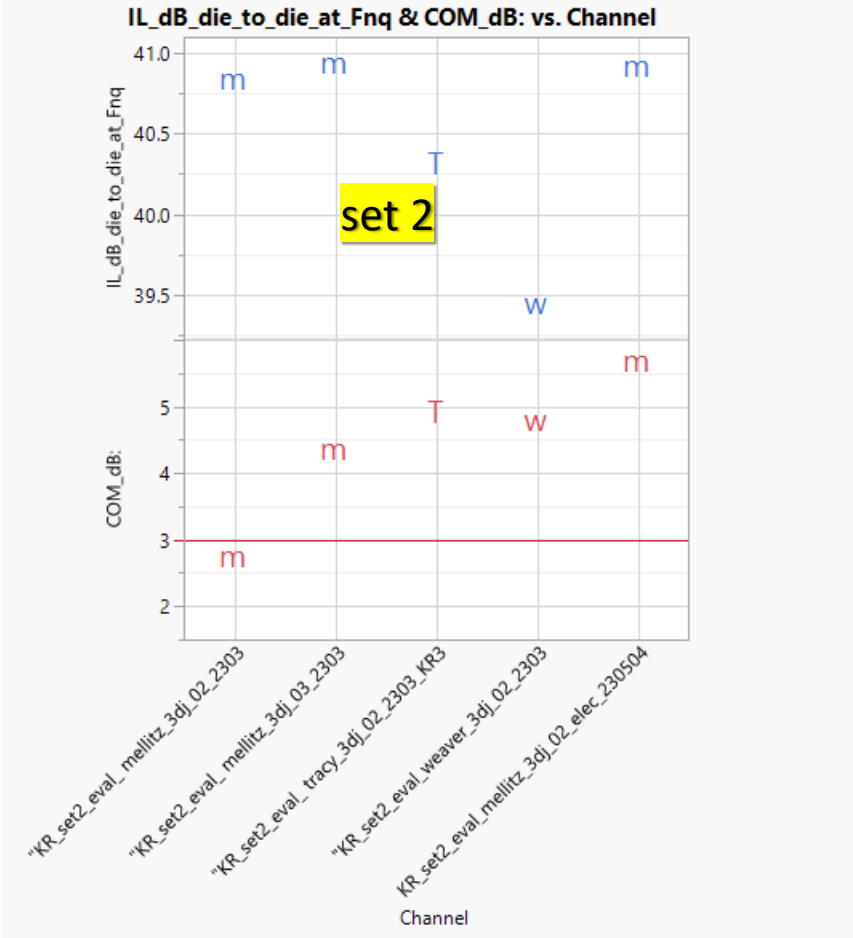
Channels which reached X of 40 dB with 7 dB loss packages

- Channels in this presentation (with key)
  - tracy_3dj_02_2303 (T)
    - TE_KR3_2p7dBPCB_10in30AWG_Conn_1m26AWG_Conn_10in30AWG_2p7dBPCB_THRU
  - weaver_3dj_02_2303 (w)
    - KR_ch_3in_PCB_NPC_300mm_29AWG_BP_800mm_27AWG_thru
  - mellitz_3dj_02_2303 (m)
    - KRCA_wXTALK_25_PCB-25-25_mm_FO-300-300_mm_CA-1000_mm_thru
  - mellitz_3dj_03_2303 (m)
    - KRCA_wXTALK_LD_25_PCB-25-25_mm_FO-300-300_mm_CA-1000_mm_thru
  - mellitz_3dj_02_elec_230504 (m)
    - KRCA_wXTALK_MX_4_PCB-25-25_mm_FO-200-200_mm_CA-200_mm_thru

Landing zone channels for X=40 dB

Both sets of COM parameter can achieve 3 dB of COM





Proposed IEEE P802.3dj Objectives

- Define a physical layer specification that supports 200 Gb/s operation over 1 lane over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz
- Define a physical layer specification that supports 400 Gb/s operation over 2 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz
- Define a physical layer specification that supports 800 Gb/s operation over 4 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz
- Define a physical layer specification that supports 1.6 Tb/s operation over 8 lanes over electrical backplanes supporting a die-to-die insertion loss <= 40 dB at 53.125 GHz

Summary

- 3 dB COM demonstrated for channels with 40 dB die to die loss
- Replace X with 40 dB in straw poll #1 of motions_3dfdj_2303
  - Technical feasibility illustrated with 3 KR channels from different sources and different COM parameters,
- Propose: Add 200GBASE-KR1, 400GBASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8 objectives to IEEE P802.3dj as on slide 13

Straw Poll

I would support the backplane objectives for 200GBASE-KR1, 400BASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8 in mellitz_3dj_01_2305 slide 13

Y: N: A:

Thank You!