25G FECL & 100G FECL Based FEC Sublayer Architecture for Inner Code (128,120)

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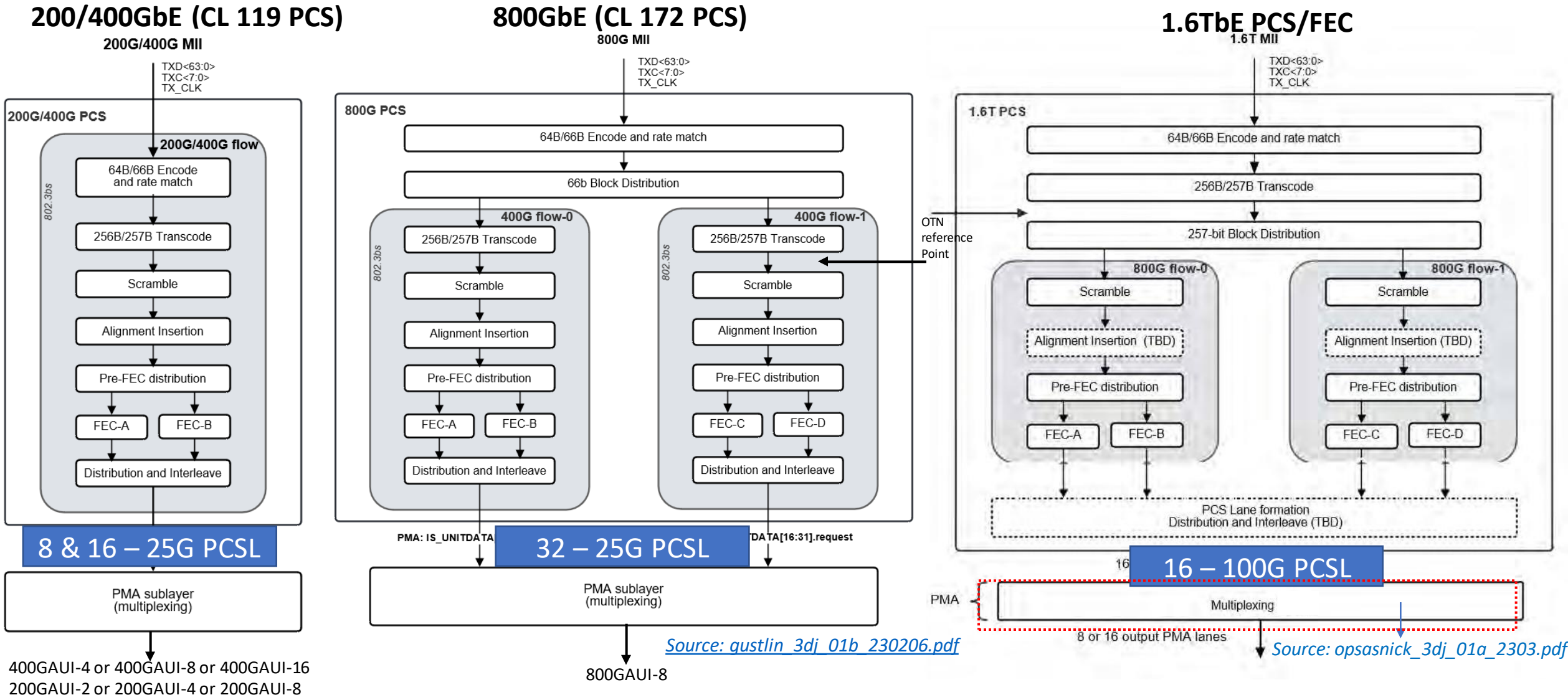
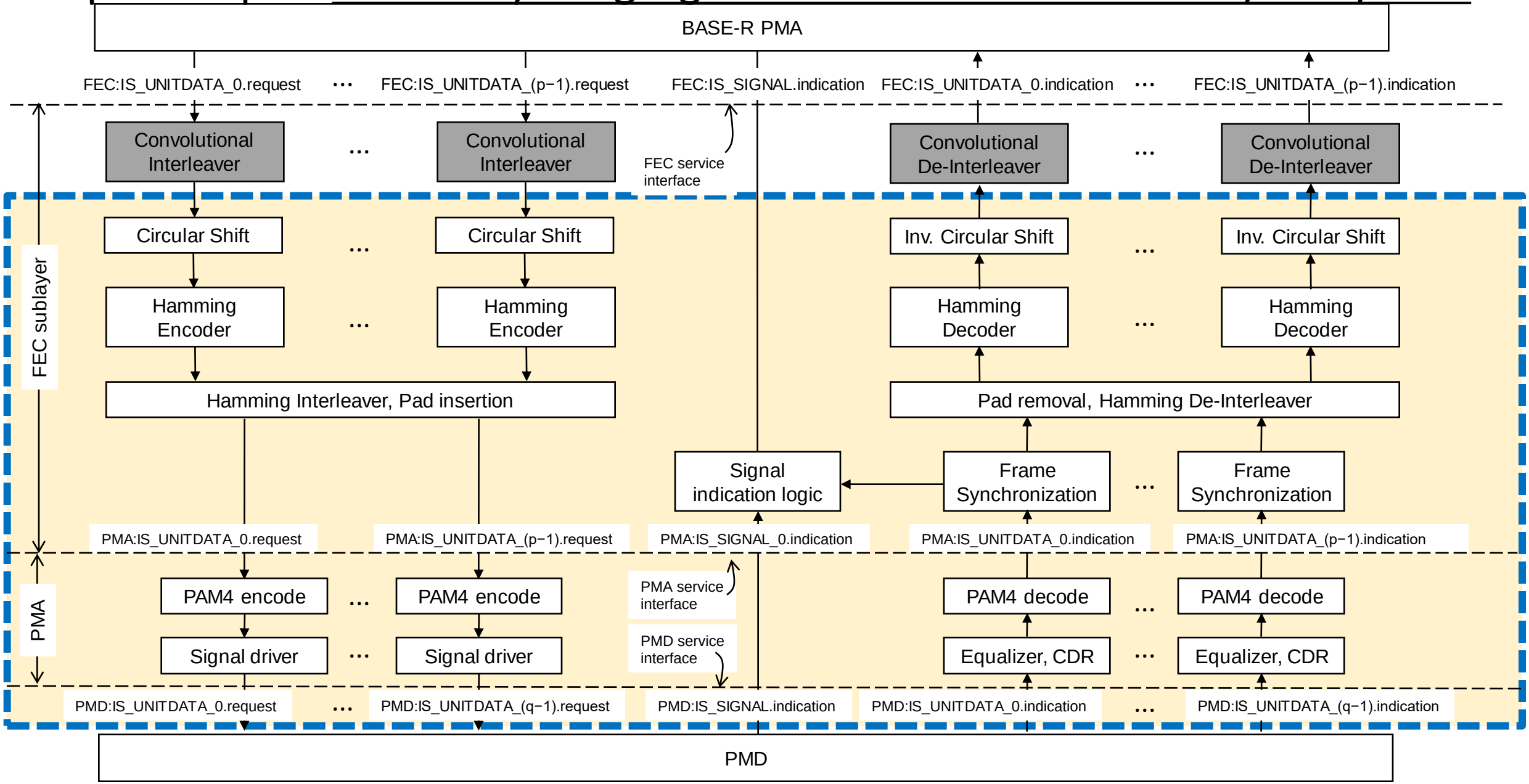
Goal of this Presentation

This presentation describes the detailed overview of 25G FECL & 100G FECL based FEC sublayers Architecture for Inner Code (128,120).

Recap of Type of PCSL already adopted for 200G/400G/800G/1.6TbE in IEEE

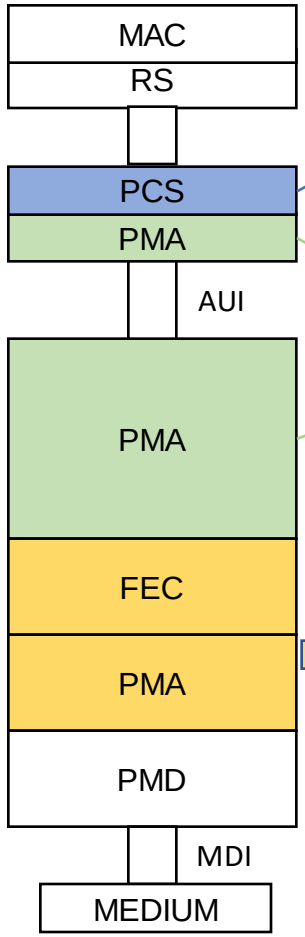


Recap of Adopted FEC Sublayer Highlighted in Dotted Lines for 200G/400G/800G



Source: patra_3dj_01b_2303.pdf & parthasarathy_3dj_02a_2303.pdf

Status of Inner FEC Architecture & Work in Progress



Type 2 scheme

200G, 400G, 800G, 1.6T PCS is adopted as per CL-119, CL-172 PCS

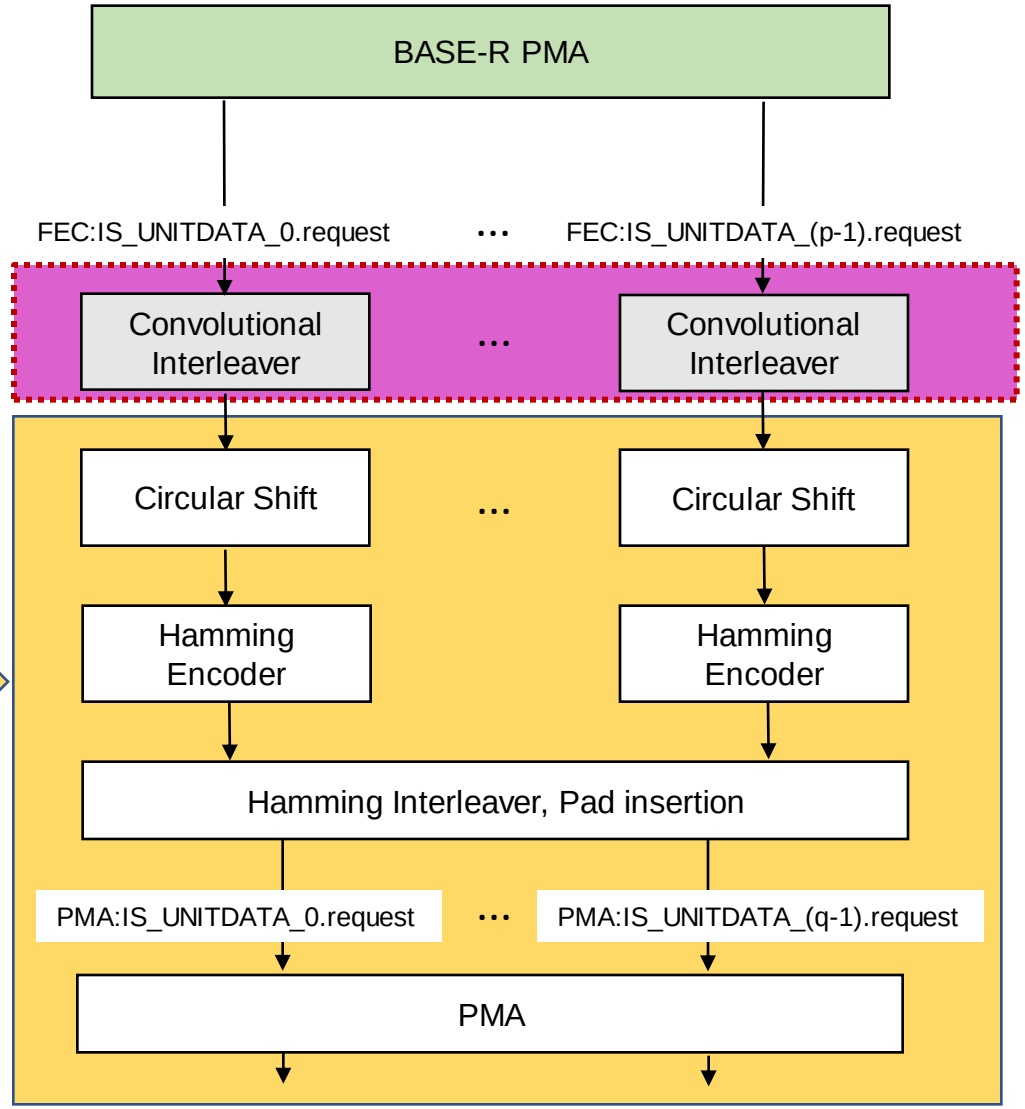
- Up to 800G – This is **25G PCSL** based
- For 1.6T - This is **100G PCSL** based

200G Symbol Muxing PMA Lane is adopted: ran_3dj_01a_2303.pdf

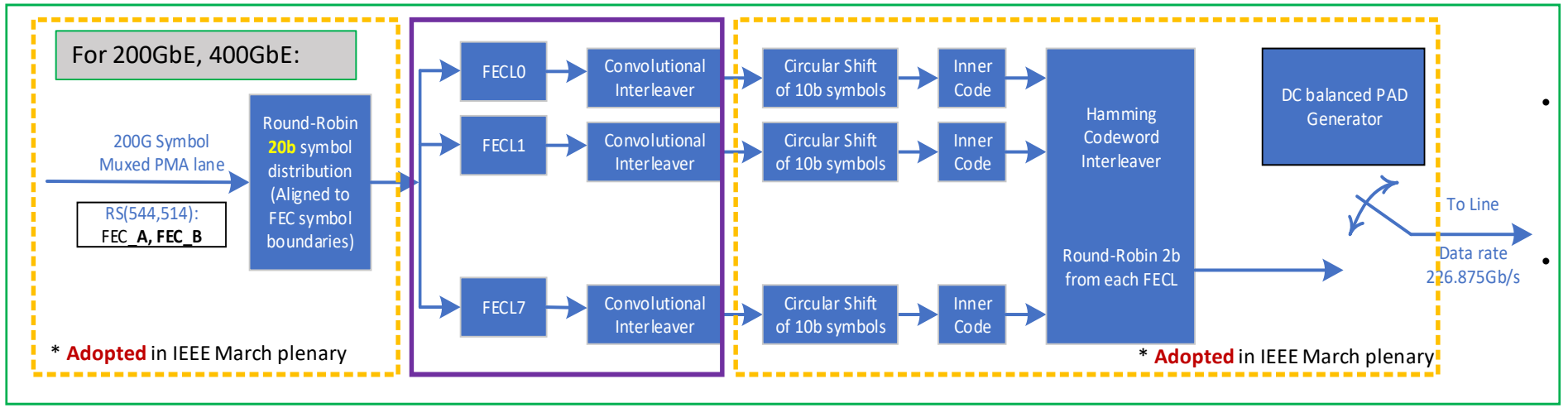
* Most of the Inner Code FEC sublayer is adopted except few blocks

Work in Progress:

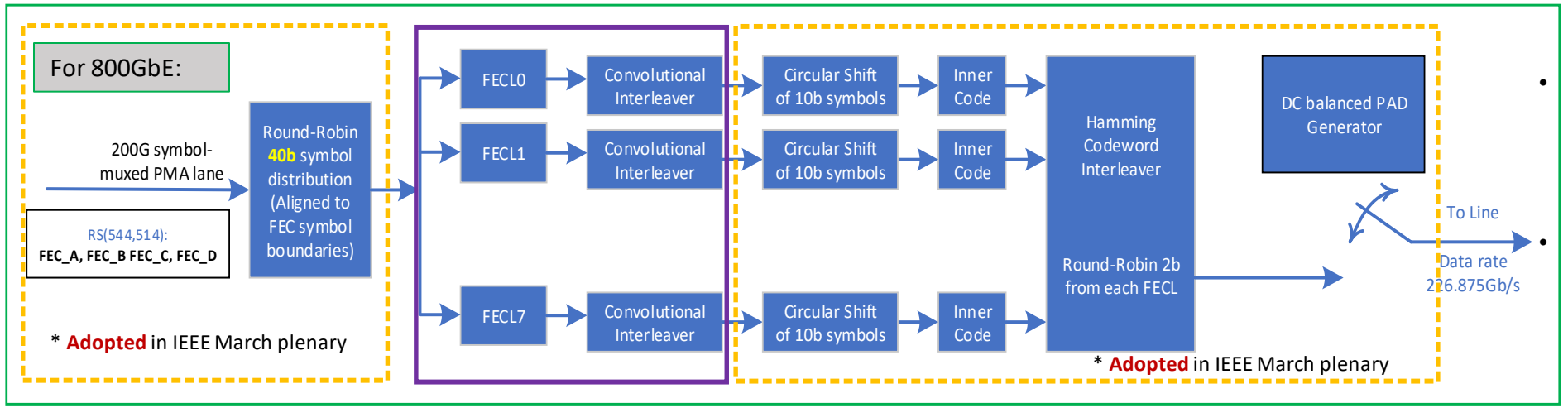
- Rate of Convolutional Interleaver for 200G/400G/800GbE
- Inner FEC sublayer for 1.6TbE



Representation of 25G FECL Processing of TX Path with Inner Code (128,120) Based on 200G PMD

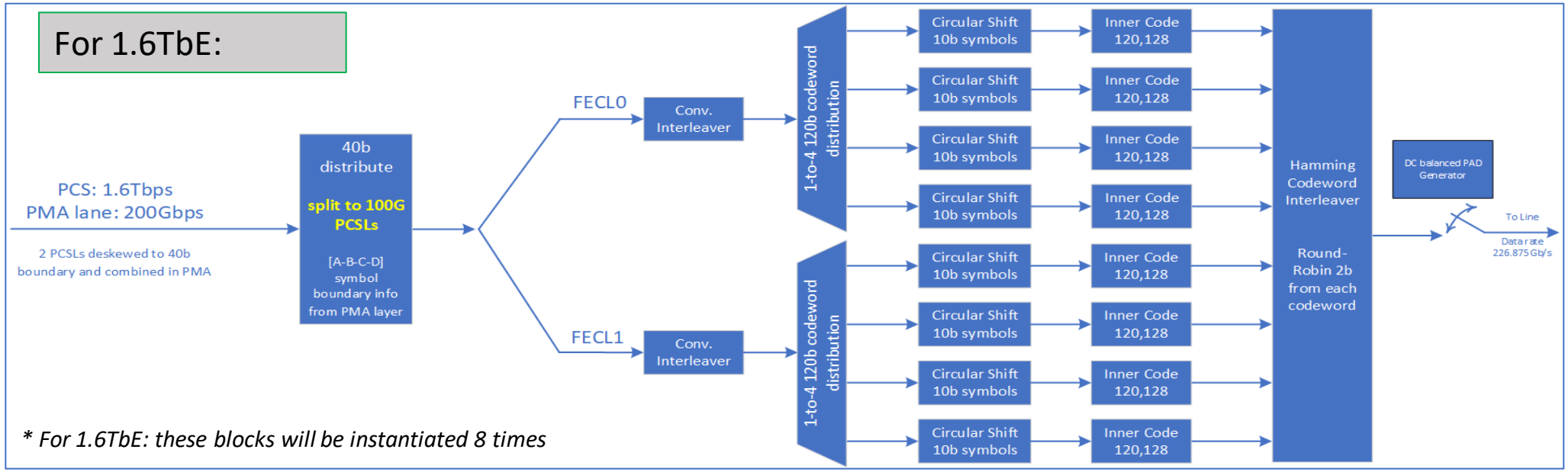


- 200G/400G – Building the **CI** (Convolutional Interleaver) based on 25G FECL fits perfectly to the PCSL already defined for 200G/400GbE in IEEE
- 25G FECL based CI also fits well to the already adopted 8-way Hamming Interleaver for better System Performance with Inner Code



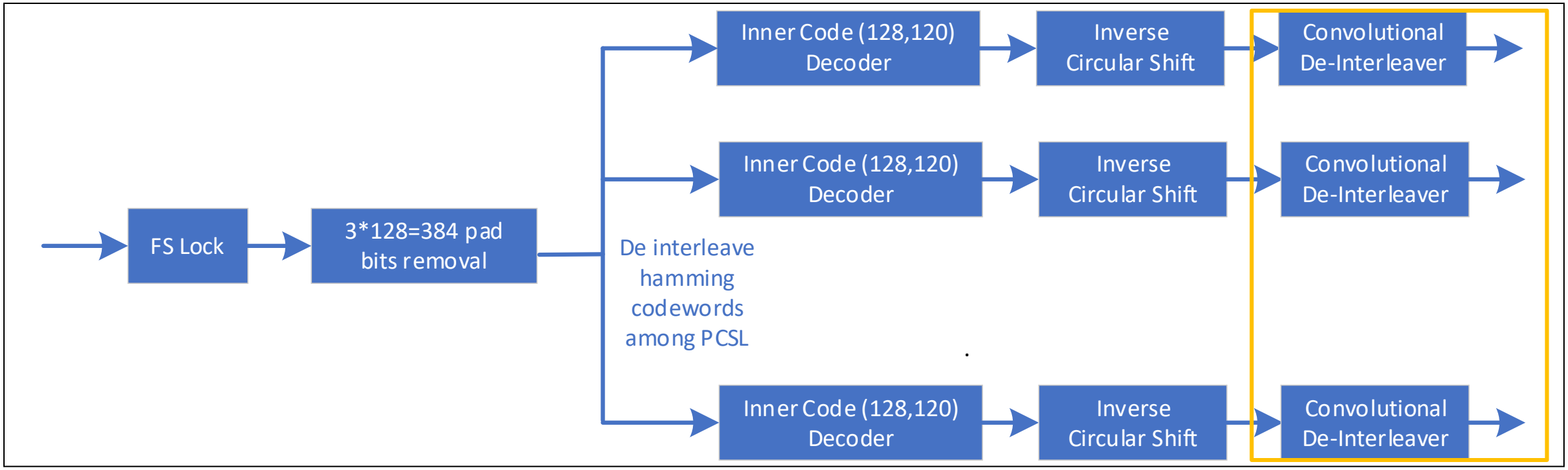
- 800G – Building the **CI** (Convolutional Interleaver) based on 25G FECL also chimes well with 32 PCSL already defined for 800GbE
- Just like 200G/400G - 25G FECL based CI also fits well to the already adopted 8-way Hamming Interleaver for better System Performance with Inner Code for 800GbE

Representation of 100G FECL Processing TX Path with Inner Code (128,120) Based on 200G PMD



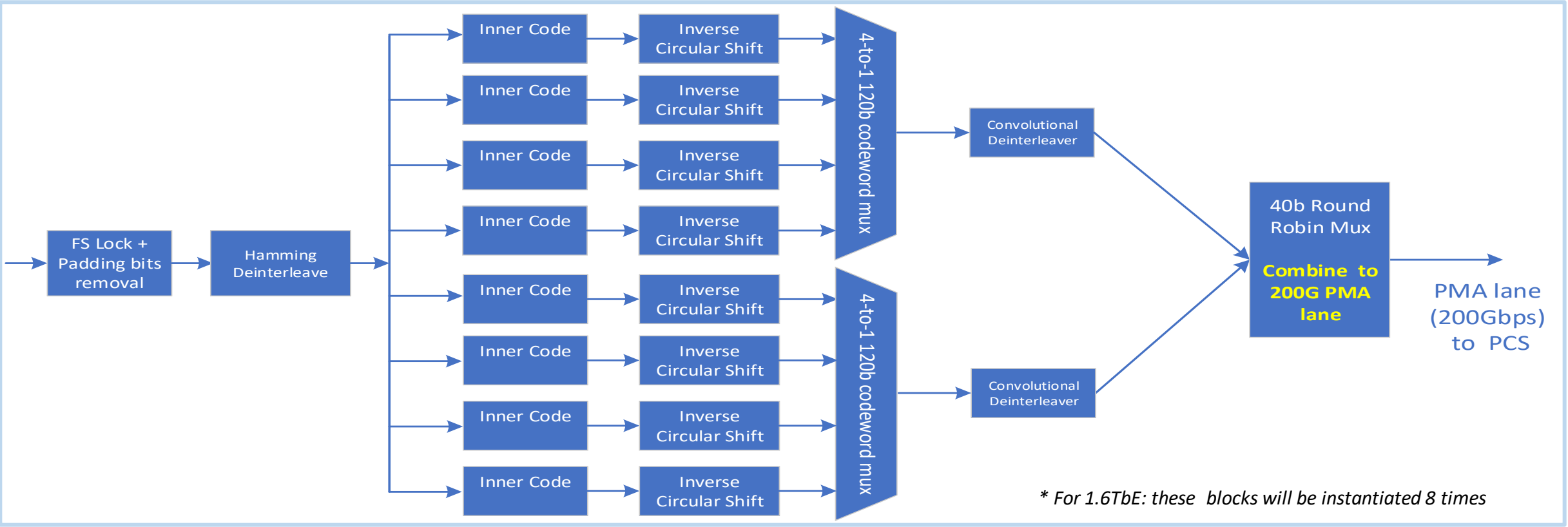
- 1.6Tbps PCS is based on 16 X 100G PCSL. A 200G PMA lane for such a scheme will consists of 2 X 100G PCS Lane.
- As adopted in IEEE - 200Gbps PMA Lane is already formed by de-skewing 2x 100G PCS lanes to 40b boundary, followed by multiplexing any 2 PCS lanes (among 16) into FEC A/B/C/D boundary aligned to 40 boundary.
- 100G PCSL based 200G PMA can simply leverage the properties of 8-way Hamming Interleaver; which is already adopted for 200G/400G/800G.
- Following blocks are needed to process it with 8 -way Hamming Interleaver
  a. Convert 200G PMA lane to 100G FEC Lanes by distributing 40b blocks among 2 streams. The correct boundary of 40b blocks is already available from the PMA layer.
  b. Convolutional Interleaver operates at 100G FECL rate, followed by 1:4-120bit codeword distribution Demux to Circular shift and 8 way Hamming inter-leaver block.
  c. Hamming Interleaver and Padding processing is identical to 200G/400G/800GbE – as previously shown in slide # 6.

Detailed Representation of 25G FECL Processing of RX Path with Inner Code (128,120)



- FS Lock, Padding Removal Scheme, Hamming de-interleaver, Inverse circular shift has been adopted in IEEE March plenary
- Convolutional De-interleaver scheme is going to follow Convolutional Interleaver scheme as shown in 25G FECL TX path.

Detailed Representation of 100G FECL Processing of RX Path with Inner Code (128,120)



- FS Lock, Padding Removal, Hamming De-Interleaver , Inverse circular shift processing are identical to 200G/400G/800G processing scheme.
- 4:1 Mux 120bit codeword distribution is analogous to the 1:4 DeMux for 120-bit codeword distribution in the TX path.
- Convolutional De-Interleaver is going to follow the Convolutional Interleaver scheme in TX path; as shown in TX path slide to form 100G FECL for 1.6T.

Summary

- We presented a 25G & 100G FECL processing proposal, which suits well to the PCS Lanes already adopted for 200G/400G/800G/1.6T MAC configurations.

- The presented proposal also works well with adopted Inner code FEC Sub-layers and 200G Symbol Muxing PMA sublayers.

Proposed Straw poll:

I am supportive of the direction of patra_3dj_02_2305 as the baseline Convolutional Interleaver proposal for Inner Code FEC (128,120) for 200GbE/400GbE/800GbE/1.6TbE PCS.

A: Yes
B: No
C: Need more information

Thanks !