Simplified Pad Insertion for Inner FEC

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Background

- The inner-FEC in patra_3dj_01b_2303.pdf with FEC lane rate, convolutional interleaver details, and 1.6T support as TBD has been adopted by motion #5 in the P802.3dj March 2023 Plenary meeting
- Slide 14 “Insertion of padding bits to make the line rate a multiple of 156.25MHz reference clock frequency” was adopted.
- The padding block size is 384 bits (3x Inner FEC CWs).

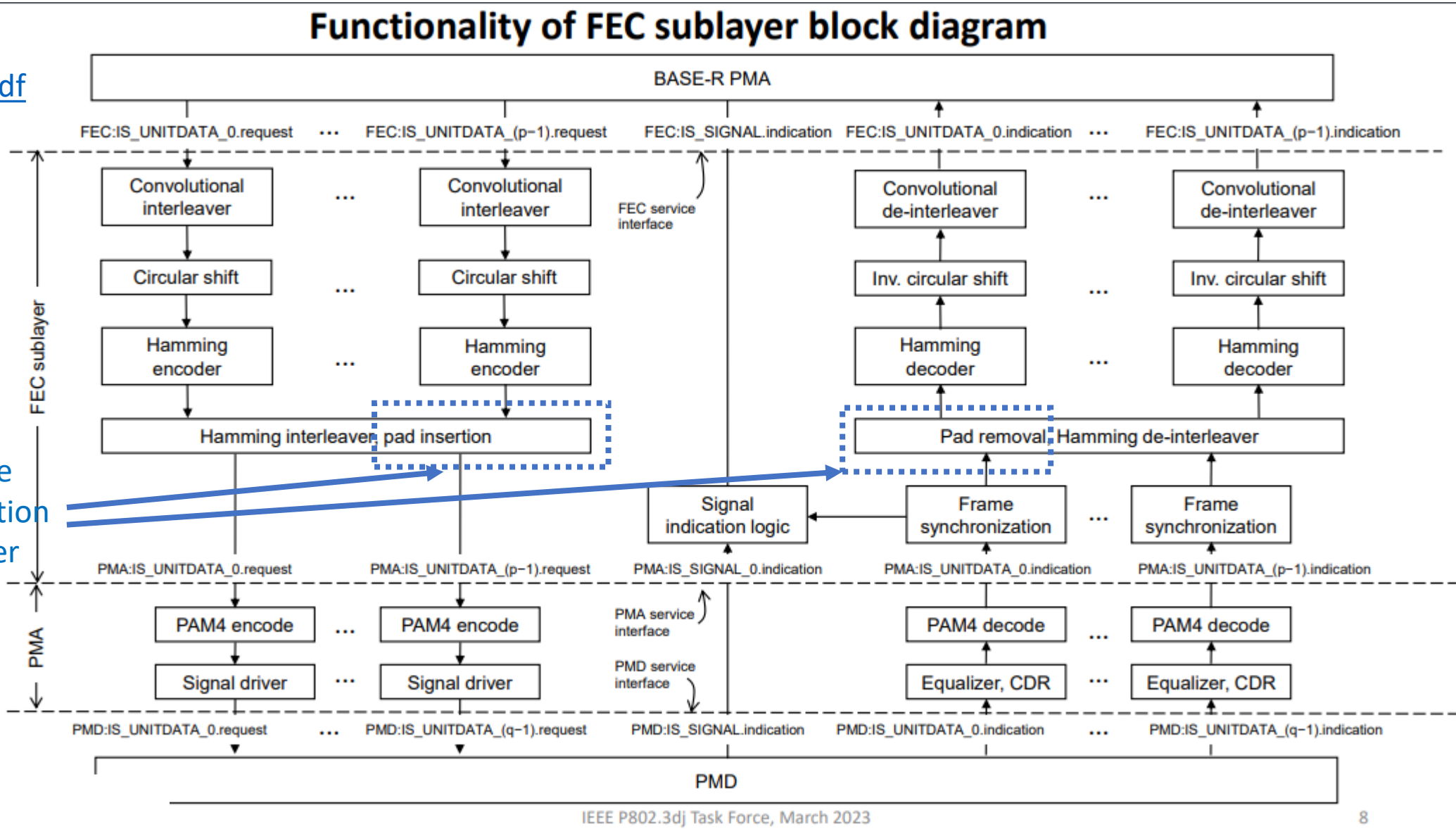
This presentation

- Proposal to improve the pad block and insertion time, in addition to Hamming interleaver protection.
  - **It delivers the same adopted 113.4375GBd (726*156.25)**
  - Appropriate for all relevant 200G/L rates (i.e., 1.6TE, 800GE, 400GE, 200GE) and breakout applications
- Considerations:
  - Protection scheme on pad bits (e.g., Hamming Interleaver) for possible reliable backchannel definitions.
  - Optimize area and power
  - Allow simple receiver synchronization scheme (e.g., Frame Sequence lock)
  - Padding bits insertion time and latency.

Adopted inner-FEC Architecture for Reference

*Figure:
patra_3dj_01b_2303.pdf
Slide 8

This proposal covers the definition for pad insertion and removal in the Inner FEC sublayer

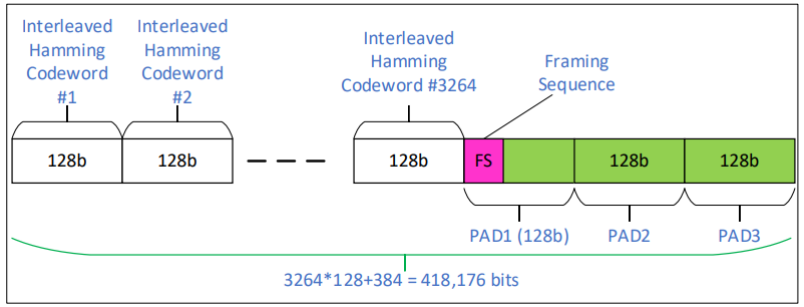


Pad insertion – 384 bits/3 CWs (patra_3dj_01b_2303.pdf)

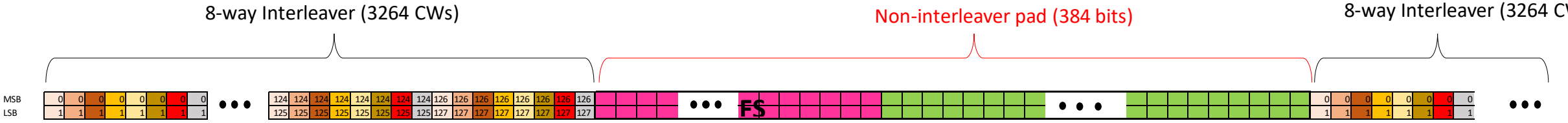
- Inserted every 3264 inner FEC CWs $(106.25Gbd * \frac{128}{120} * \frac{3264+3}{3264} = 113.4375Gbd)$
- Enable receiver to lock on Framing Sequence
- **Lack of 8-way Hamming interleaver "protection", thus pad bits are more sensitive to error propagation.**
- Less suitable for Search & Test synchronization method (like Clause 74), since pad bits differ from Datapath traffic
  - S&T – Search for 128-Hamming boundaries as alterative method to FS lock
    - Also referred in barakatain_3dj_01a_230206.pdf slide 6 "Enhanced SFEC Synchronization Process"
- Mandates to have extra logic (Inner-FEC encoders/decoders) for pad bits.
- Padding bits latency is ~1.7nsec
- Time between padding bits ~1.84usec

Pad insertion (as adopted) - Lack of interleaver on padding bits

- Slide 14 in patra_3dj_01b_2303.pdf doesn't show the Hamming interleaver:



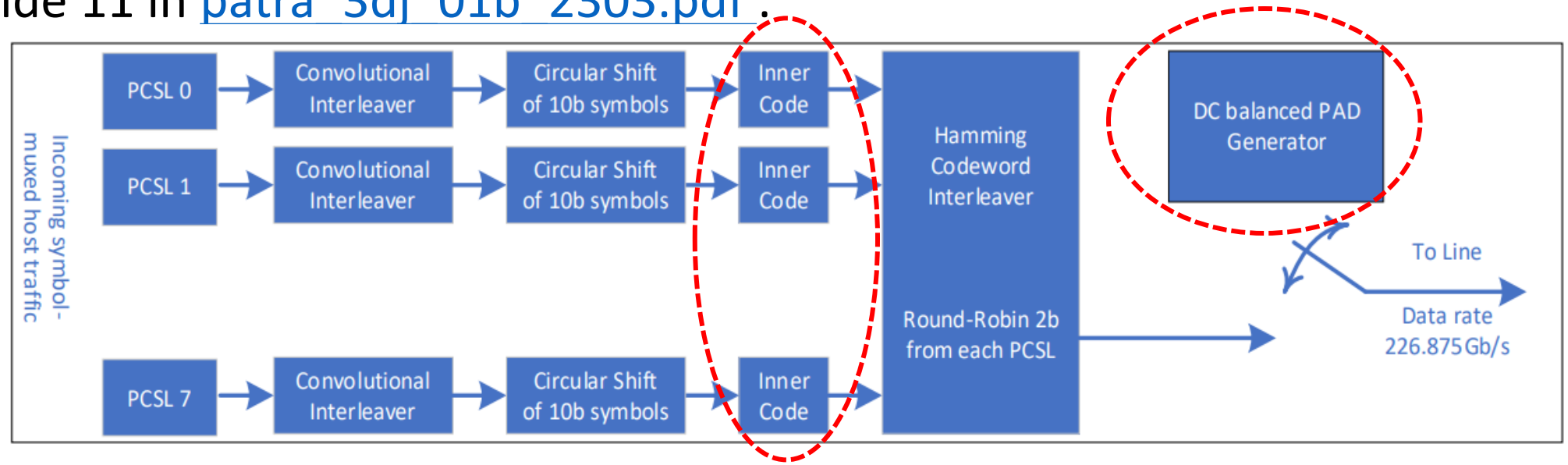
- More detailed representation:



- Two forms of data: 8-way interleaved and non-interleaved pad bits
  - No simple single data-path stream out of PMDs, as in other 802.3 BASE-R specifications.
- **No leveraging of existing Hamming interleaver for the padding bits**

Pad insertion (as adopted) inner-FEC encoders/decoders

- Slide 11 in patra_3dj_01b_2303.pdf :

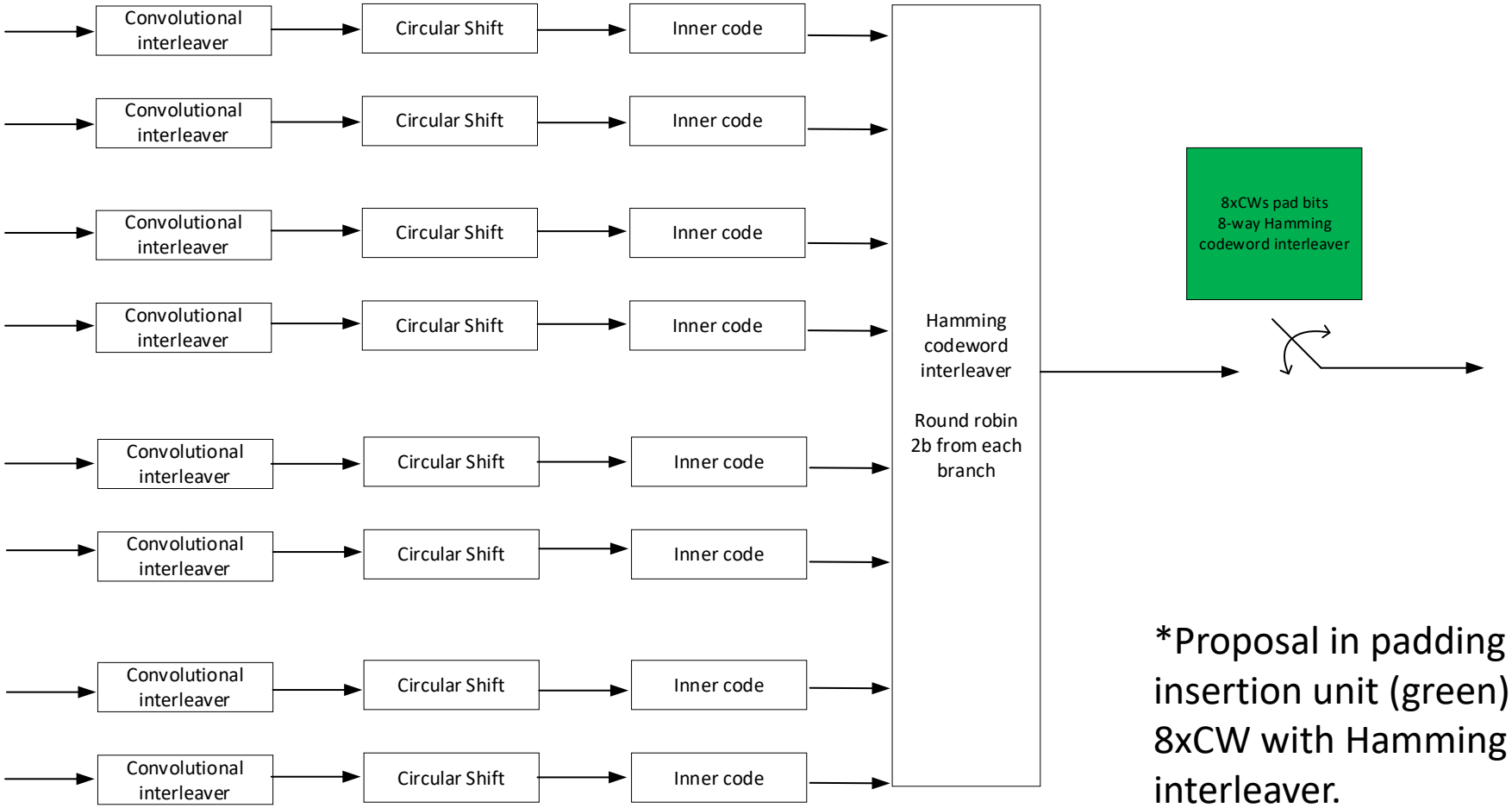


- This diagram includes 8-inner encoders/decoders for the data-path and **additional encoders/decoders for the padding bit.**
  - No reuse of the datapath encoder/decoders

Pad insertion proposal - 1024 bits/8 CWs with Hamming interleaver

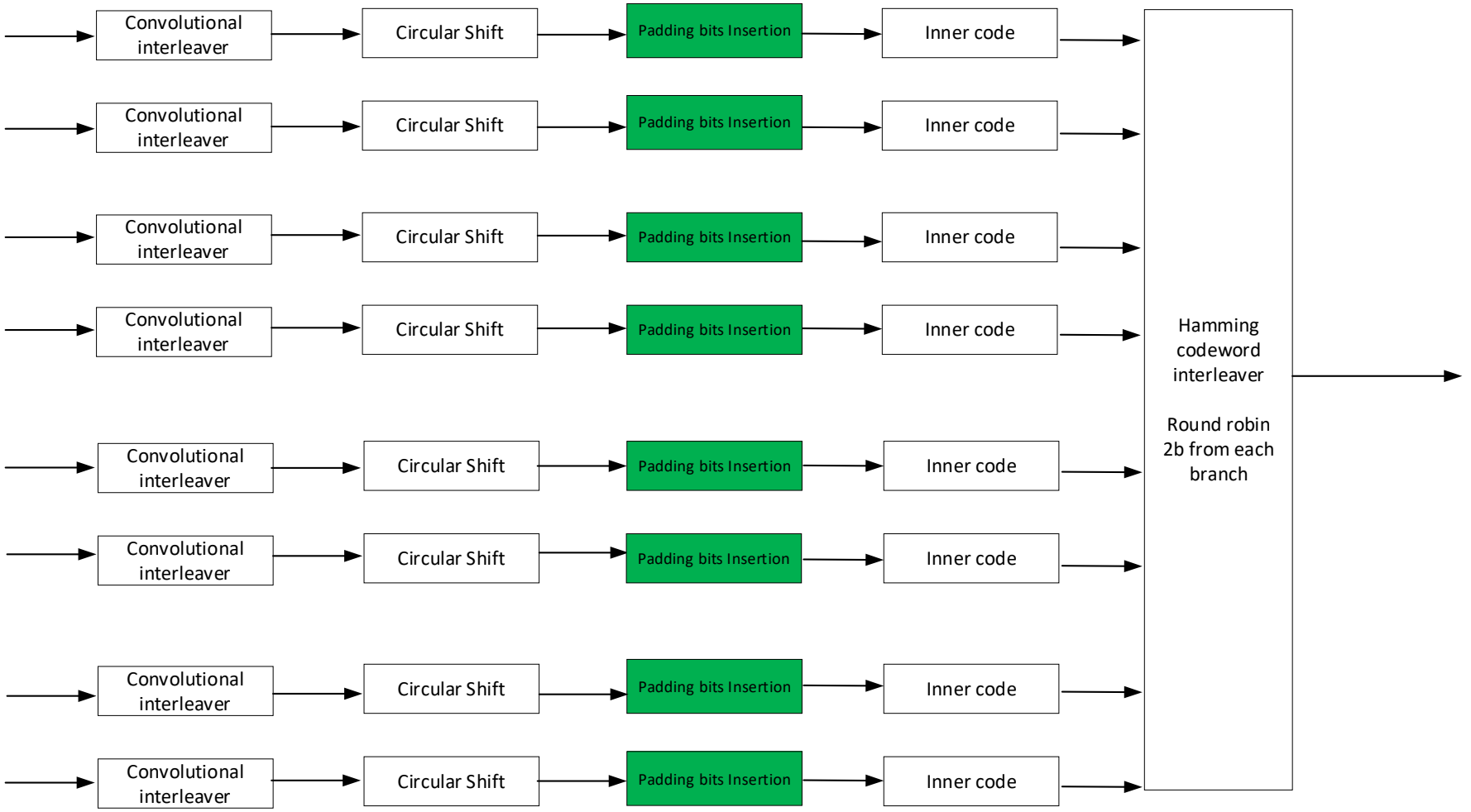
- Inserted every 8704 inner FEC CWs $(106.25Gbd * \frac{128}{120} * \frac{8704+8}{8704} = 113.4375Gbd)$
- 8-way Hamming interleaver “protection” on padding bits
- Enable receiver to lock on Framing Sequence
- Allow possible implementation of Search & Test synchronization method (similar to clause 74).
- Allow optional implementation with minimal number of inner-FEC encoders/decoders.
- Single Datapath stream of Hamming Interleaved bits on the PMD lane.
- Padding latency (~4.5 nsec)
    - pad latency can be handled by “TX/RX_NUM_BIT_CHANGE” signals (802.3cx), the same is true for the 384 bits pad size.
    - For comparison Clause 172 (800G PCS) AM size is 4,112 bits at total.
- Time between padding bits ~4.91usec

8xCWs (1024 bit) and Hamming interleaver assuming 8 FEC lanes as shown in patra_3dj_01b_2303.pdf



*Proposal in padding insertion unit (green) 8xCW with Hamming interleaver.

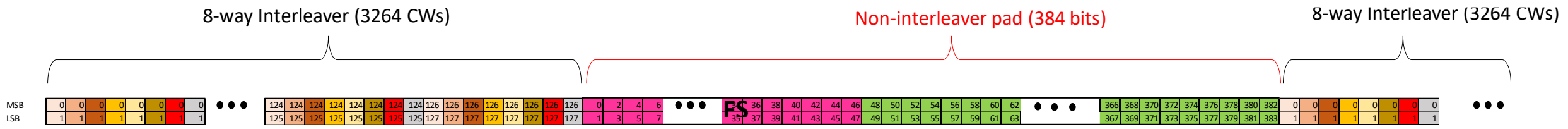
Equivalent representation of the proposed change assuming 8 lanes as shown in patra_3dj_01b_2303.pdf



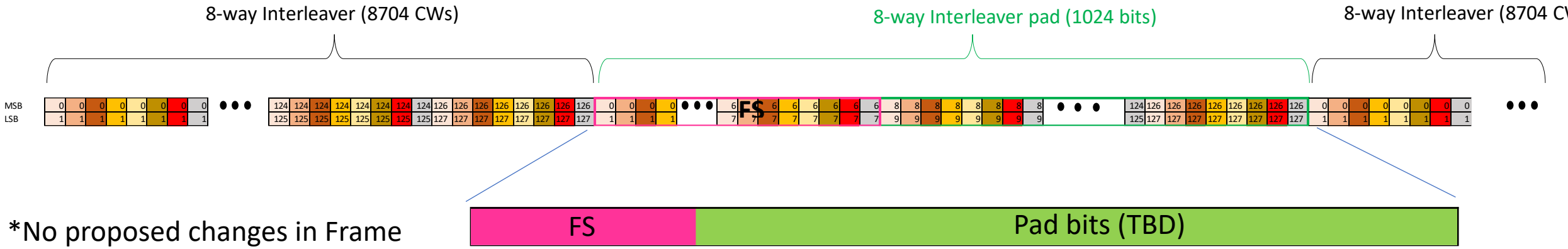
* 120 padding bits per FEC_i lane

Simple data stream on PMD

- From <u>two types</u> of streams:



- To <u>single type</u> of stream:



*No proposed changes in Frame Sequence size (48 bit) and content

Comparison table

	384 bits (patra_3dj_01b_2303.pdf)	1024 bits (proposed)
Baud rate	113.4375 GBd	113.4375 GBd
Hamming Interleaver “protection”	No	Yes
Similar to existing 802.3 BASE-R AMs/CWMs insertion process	No	Yes
Time/CWs between pad bits	1.8 usec/3264 CWs	4.91 usec/8704 CWs
Pad latency	1.7ns	4.5ns
FS lock	Yes	Yes
Possible S&T synchronization method	No	Yes
Number of encoder/decoder Power/Area	Additional inner-FEC encoders/decoders required for the pad bits	Can be optimal (reuse of inner-FEC and interleaver)

Summary

- Proposal: change the pad block to 1024 bits (8 Inner FEC CWs) and insertion period to 8704 CWs, in addition to Hamming interleaver protection.
- Content of the bits for backchannel (message field) remains TBD

Appendix A: Padding bits

Padding Specification

- 1024 bits = 8 CW using the same inner-FEC code (128,120)
  - Payload bits = 960 (=120B), Parity = 64 bits

- 120B data bytes composed as follows:*
  - 6-byte frame sync field
  - Remaining 912 bits are scrambled with PRBS13
    - 112 Byte Message field
    - CRC8 or stronger
  - The message field (details to be specified) can be used to convey link and signal-related information, such as receiver state, channel pulse response, FEC stats, etc.

*Same as patra_3dj_01b_2303.pdf Appendix A, with 114 Bytes instead of 39 Bytes for “Byte Message Field and CRC protection”