Towards an 800G-LR4 IMDD Specification Consensus - May 2023 update

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Introduction

- This presentation is an update to the 800GBASE-LR4 specs proposed in rodes_3df_01_2303

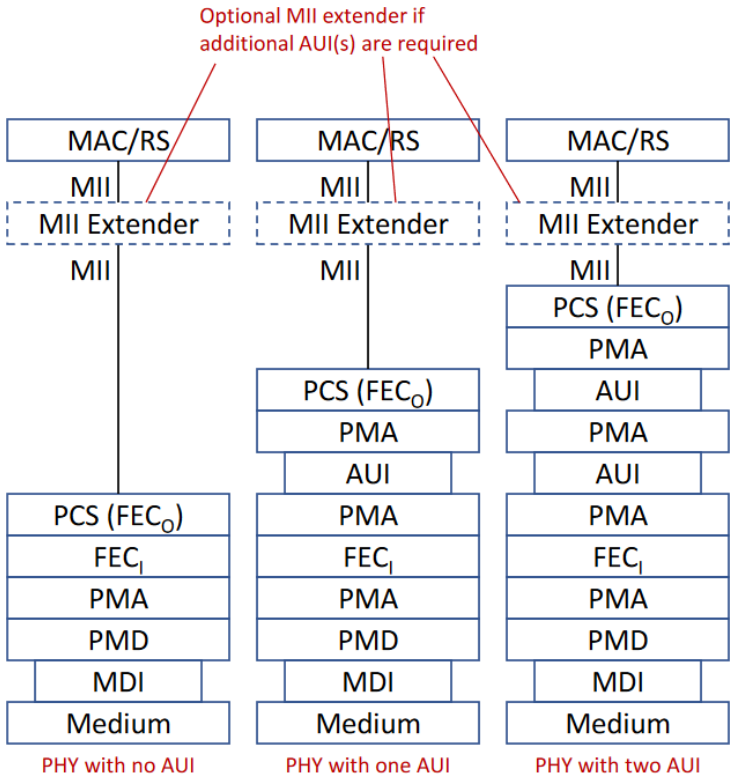
- Updated on this presentation:
  - Propose using same inner FEC adopted for other 200G/lane IMDD PMDs
  - Propose to adopt fiber channel model in cole_3dj_01_2305
  - Proposing TDECQ equalization to be left ‘TBD’ for future discussion
  - Updated FWM penalty allocation based on latest analysis

- We propose this specification as a baseline for 800GBASE-LR4 with further refinements based on contributions from the Task Force

FEC proposal

- 800G-LR4 small volume will not justify a dedicated IC design
- 800G-LR4 will necessarily reuse the same Type2 inner FEC as in Motion#5 in March 2023 Plenary
- Experimental and simulation data indicates FEC in patra_3dj_01b_2303 is enough to accommodate:
  - CD up to -28ps/nm (assuming worst case dispersion window from ITU ZDW of 1300-1324nm). kuschnerov_3df_02_221012
  - LR power budget. kuschnerov_3df_02_221012
  - FWM. liu_3dj_01_2303
  - PMD. kuschnerov_3df_01b_221012

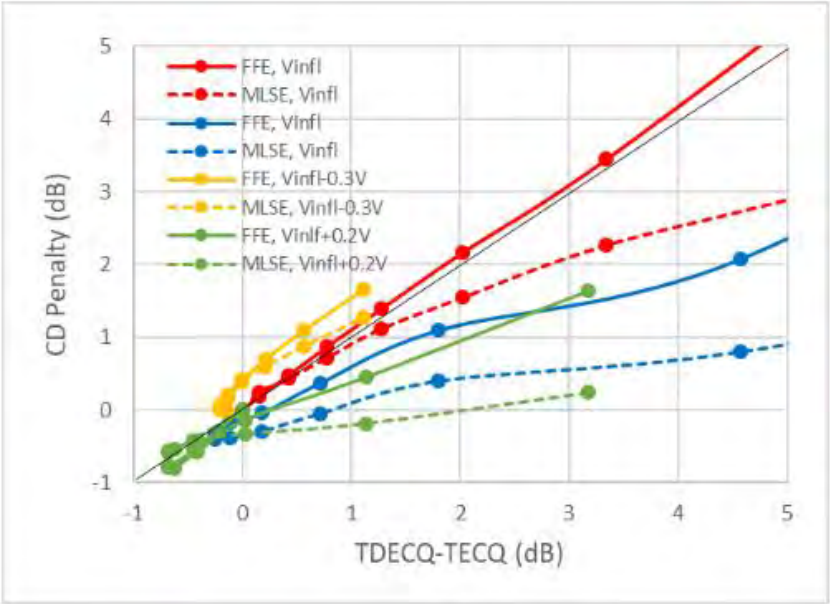
Type 2 PHY/FEC scheme



brown_3dj_optx_adhoc_01a_230222

TDECQ reference equalizer considerations

- 200G/lane requires stronger equalization compared to 100G/lane:
  - Higher ISI: components are not quite doubling the BW
  - Higher Noise: higher Xtalk and Rx IRN
  - Smaller CD tolerance: it reduces quadratically with Baudrate
  - Farther away reflections: round trip is two times the number of UIs for the same electrical length
- Real receivers have equalizers that are more powerful including FFE with more taps, DFE and MLSE
- Reference receiver needs to be updated accordantly otherwise:
  - TDECQ will not represent real link power penalty
  - Unnecessary yield hit and added cost in Tx
  - Distrust from users on SECQ to evaluate Rx Sensitivity
- A weaker TDECQ reference equalizer is inefficient to provide margin on Rx because it cannot distinguish Txs with equalizable impairments from Txs with unequalizable impairments
- We propose to leave TDECQ reference equalizer as 'TBD' in the first baseline. It requires careful evaluation with more data, and it is not strictly necessary to build link power budget.



johnson_3df_01a_221011

Updating Fiber Channel model

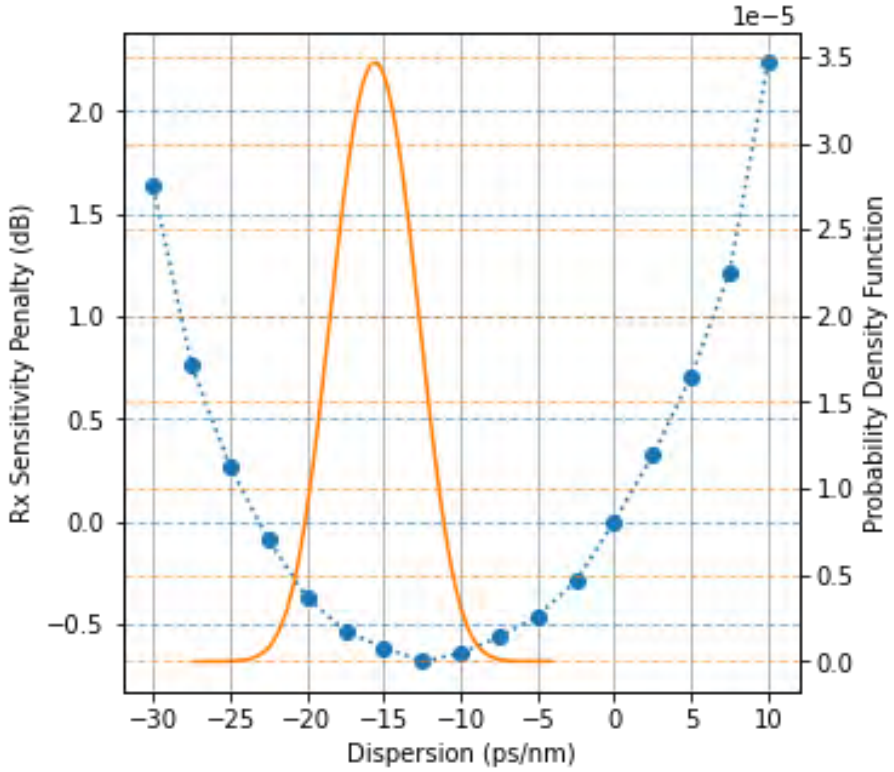
Chromatic dispersion penalty exponentially increases toward dispersion edges on 800G-LR4. At the same time, probability of facing such large dispersion rapidly decreases. Therefore, considering the probability of facing corner dispersion is important.

cole_3dj_optx_01_2305 defines a fiber ZDW model and proposes to use TDECQ testing points form ZDWmin= 1305nm and ZDWmax= 1319nm.

liu_3dj_optx_01_230427 shows how those test points represent a statistically worst-case dispersion scenario with probability <1e-6 for >=4 segments

Therefore, we propose adopting 1305nm and 1319nm ZDW as the worst cases for power budget calculations for 800G-LR4

Penalty for Lane0= 1295.56nm with 0.8 chirp

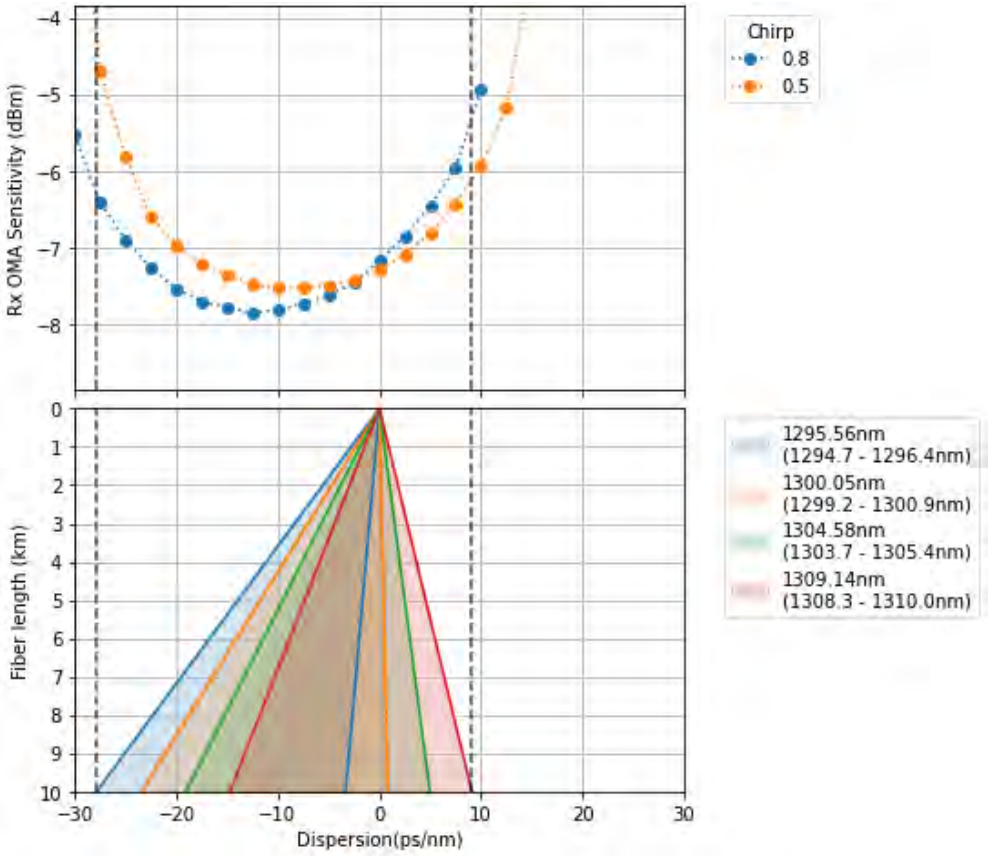


CD penalty with new test points

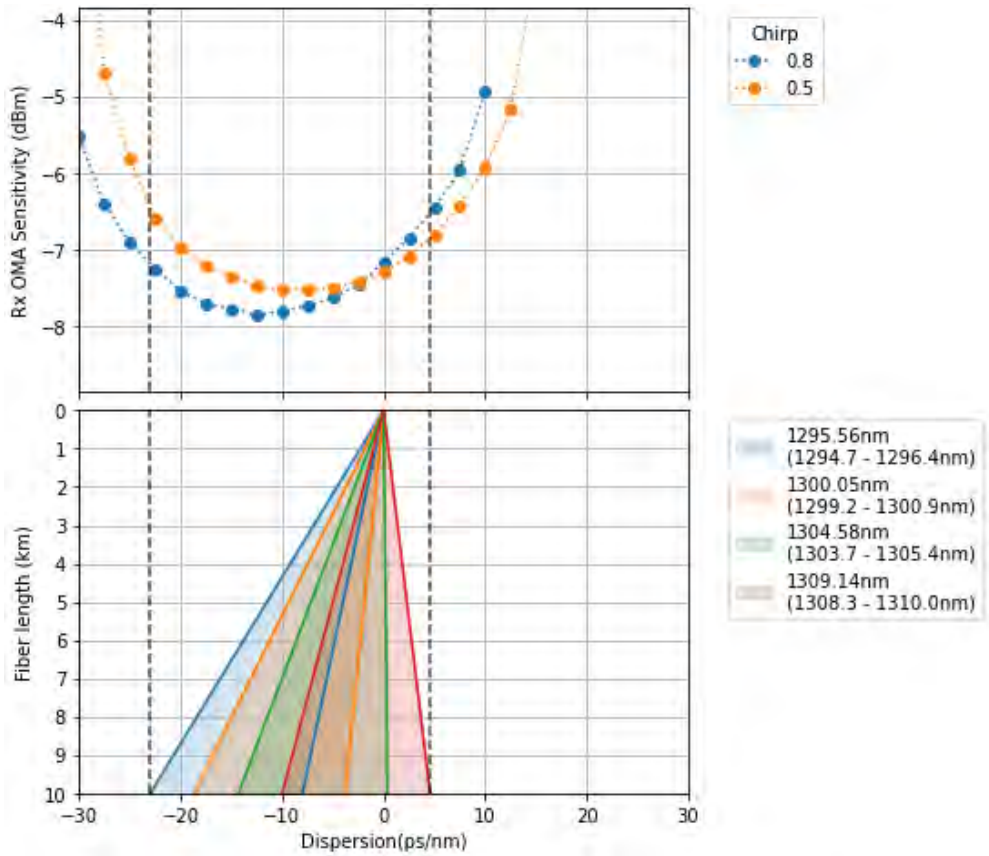
Assumptions:

- 113.4375 GBd
- BER = 4.85e-3
- 21-tap Rx FFE

Traditional ZDW 1300-1324nm



New ZDW 1305-1319nm



New test point would provide lower CD penalty potentially enabling simpler receiver

Tx Spec proposal

Static FWM probability is low enough to not have significant economic consequences, based on liu_3dj_01_2303 and johnson_3dj_01a_230206. Therefore, lower TDECQ spec over the range of lower CD where FWM could possibly occur is not necessary anymore

OMAouter is 5.7dBm to provide sufficient headroom for OMAmin@TDECQmax (1.3dB)

AOP is 5.5dBm, 0.2dB lower than OMAouter max. Same than, for example, 400GBASE-DR4

TDECQ reference receiver:

- BW: 4th order Bessel Thompson filter with -3dB cutoff at Nyquist
- Reference Equalizer: TBD

Description	800G-LR4	Unit
Signaling rate, each lane (range)	113.4375	GBd
Modulation format	PAM4	
Lane wavelengths (range)	1294.6 to 1296.6 1299.1 to 1301.1 1303.6 to 1305.6 1308.1 to 1310.1	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Total average launch power (max)	11.5	dBm
Average launch power, each lane (max)	5.5	dBm
Average launch power, each lane (min)	-0.9	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane (max)	5.7	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane (min) for TDECQ <1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.9 dB	 1.9 0.5+TDECQ	 dBm dBm
Difference in launch power between any two lanes	3	dB
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.9	dB
Transmitter eye closure for PAM4 (TECQ), each lane (max)	3.2	dB
|TDECQ-TECQ| (max)	2.5	dB
Over/under-shoot (max)	22	%
Transmitter power excursion (max)	3.1	
Extinction ratio, each lane (min)	3.5	dB
Transmitter transition time (max)	13	ps
Average launch power of OFF transmitter, each lane (max)	-16	dBm
$RIN_{15.6}OMA$ (max)	-139	dB/Hz
Optical return loss tolerance (max)	15.6	dB
Transmitter reflectance (max)	-26	dB

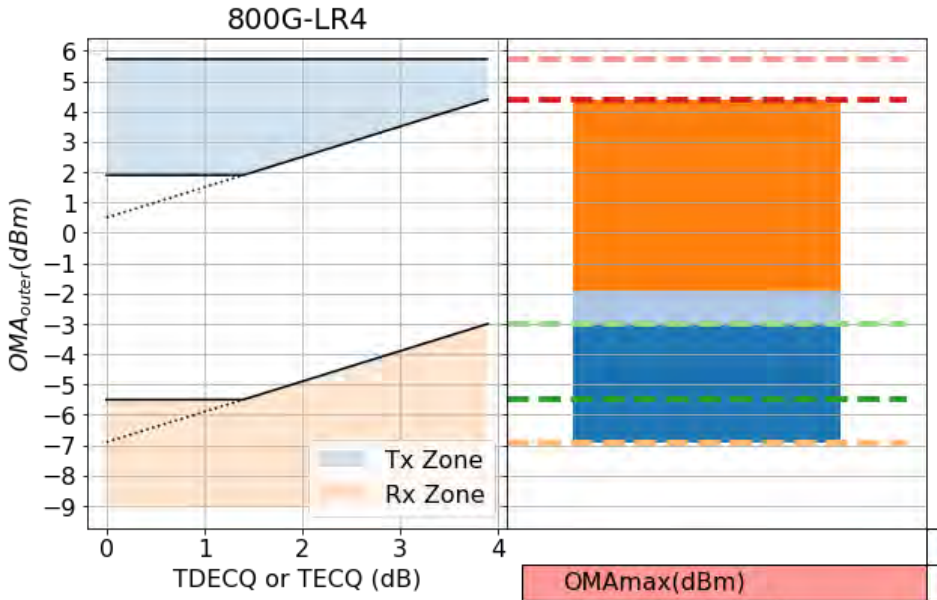
Rx Spec proposal

Rx sensitivity of -5.5dBm @ TDECQ = 1.4dB is achievable based simulation analysis:
rodes_3df_01b_221012
,and experimental data:
kuschnerov_3df_02a_221012

Rx sensitivity measured for BER= 4.85e-3 per patra_3dj_01b_2303. Slight modification might be required based on final AUI BER requirement.

Description	800G-LR4 proposal	Unit
Signaling rate, each lane (range)	113.4375	GBd
Modulation format	PAM4	
Lane wavelengths (range)	1294.6 to 1296.6 1299.1 to 1301.1 1303.6 to 1305.6 1308.1 to 1310.1	nm
Damage threshold, each lane	6.5	dBm
Average receive power, each lane (max)	5.5	dBm
Average receive power, each lane (min)	-8	dBm
Receive power (OMAouter), each lane (max)	5.7	dBm
Difference in receive power between any two lanes (OMAouter) (max)	3.3	dB
Receiver reflectance (max)	-26	dB
Receiver sensitivity (OMAouter), each lane (max) for TECQ <1.4 dB for 1.4 dB ≤ TECQ ≤ 3.9 dB	 -5.5 -6.9 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMAouter), each lane (max)	-3	dBm
Conditions of stressed receiver sensitivity test:		
Stressed eye closure for PAM4 (SECQ), lane under test	3.9	dB
OMAouter of each aggressor lane	1.3	dBm

Link Power Budget



	800G-LR4
OMAmax(dBm)	5.7
OMA-TDECQ(dBm)	0.5
OMAmin@TDECQmax(dBm)	4.4
SRS(dBm)	-3.0
Rx Sens (TECQ <= 1.4dB)	-5.5
RSnominal(dBm)	-6.9
OpticalLossBudget	6.3
AdditionalPenalties	1.1
TDECQmax	3.9
PowerBudget	11.3

Parameter	**800G-LR4 proposal**	**Unit**
Power budget (for maximum TDECQ)	11.3	dB
Operating Distance	10	km
Channel insertion loss	6.3	dB
Maximum discrete reflectance	-35	dB
Allocation for penalties (for maximum TDECQ) *	5	dB

*DGD=0.7dB and MPI= 0.4dB , kuschnerov_3df_01b_221012, kuschnerov_3df_02a_221012

Conclusion

- We have presented an update on the set of specs for 800GBASE-LR4
- We propose to use the same FEC in patra_3dj_01b_2303 that was adopted for all other 200G/lane PMDs as in Motion#5 in March 2023 Plenary
- We propose to adopt TDECQ test points in cole_3dj_optx_01_2305 with ZDWmin=1305nm and ZDWmax=1319nm and use them as the worst cases of statistical link analysis for power budget calculations
- TDECQ reference equalizer is proposed to be left as 'TBD' for future discussion
- Lower TDECQ spec over the range of lower CD where FWM could possibly occur is not necessary and has been removed
- We expect further refinement as the task force progresses and more data comes available