Updated KR Channels In Support of a 200G Backplane Objective

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TE Connectivity
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EVERY CONNECTION COUNTS

Contributors

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Overview

This contribution is an update to and replaces KR channels provided in the March 2023 IEEE 802.3dj meeting.

Goal is to provide an updated set of passive copper backplane channels, based on conventional and unconventional architecture concepts, to help support technical feasibility, enable multi-party analysis and provide guidance to P802.3dj discussions.

Development work is on-going, updates and refinements are anticipated in future contributions.

The intent of this presentation is to provide technical support and directional input for adding a backplane objective and promote consensus among the participants.

Description

- Updated simulated KR channels, for 200G applications, using backplane concept connector and cabled backplane assembly with various host architecture options

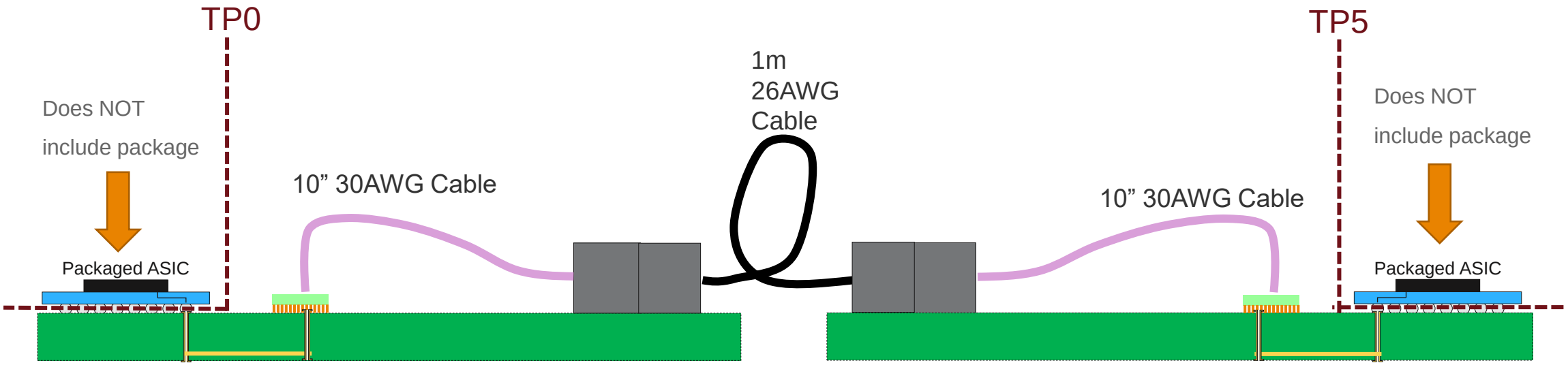
- The updates include –
  - Updated symmetric cabled line card model with improved BGA escape and updated traces
  - A new channel with PCB based line card at each end of cabled backplane, using updates from above

- BGA escape model provided by Regee Petaja and Chi Tu of Broadcom

- Does NOT include silicon package

- What this presentation is NOT:
  - A specific host architecture proposal; comparative performance options are presented, i.e., traces vs. cabled host
  - Asymmetric architecture proposal (managed deployment)

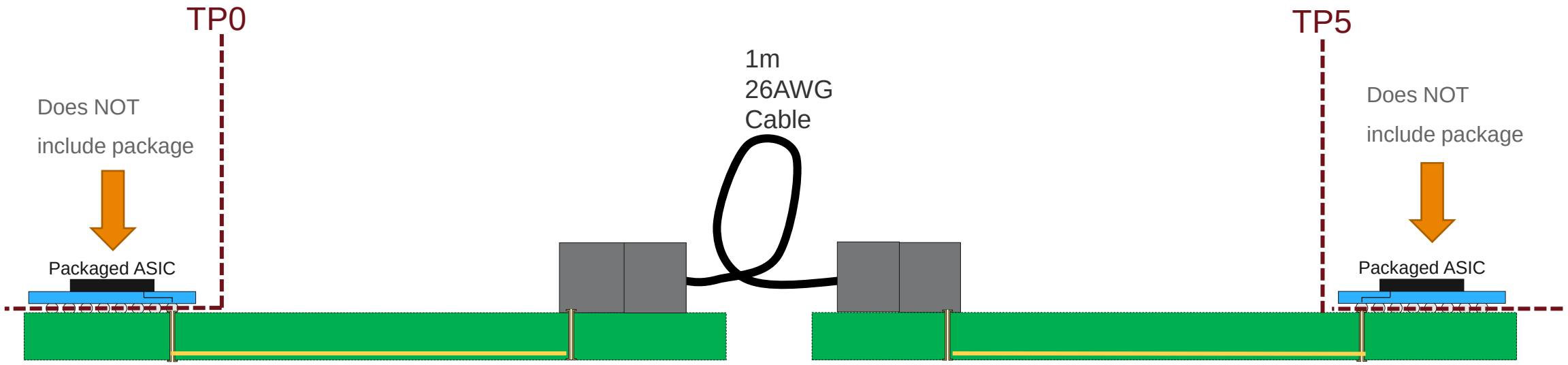
Cabled Backplane, Near Chip Cables



Channel includes at each end of 1m cable,

- Cabled backplane connector to cabled backplane connector
- Cable Termination to cabled backplane connector
- 10”, 30AWG Cable
- Cable termination to near chip connector
- Near chip connector
- Near chip transition via and breakout traces
- Updated BGA footprint + breakout, 0.9-1.0mm pitch
- Updated Host Loss,~7.85dB @ 53.125GHz
  - Host Loss includes BGA escape, traces, near chip connector and internal cable
- All components are at room temperature
- Channels do not include additional skew beyond whatever is part of design.

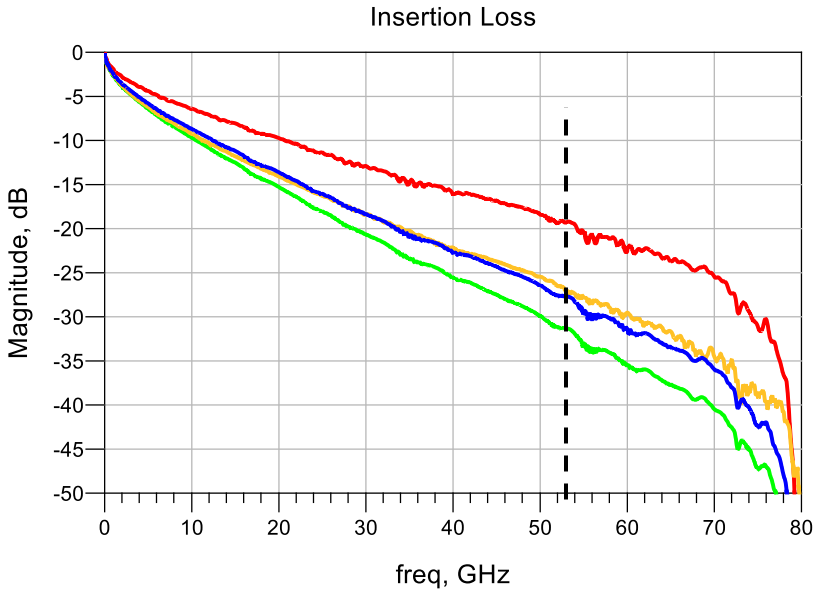
Cabled Backplane, PCB

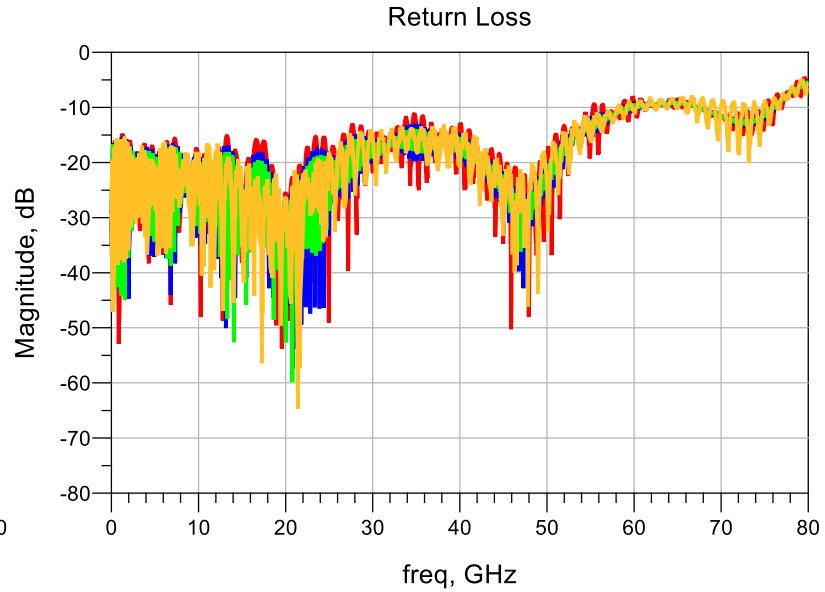


Channel includes at each end of 1m cable,

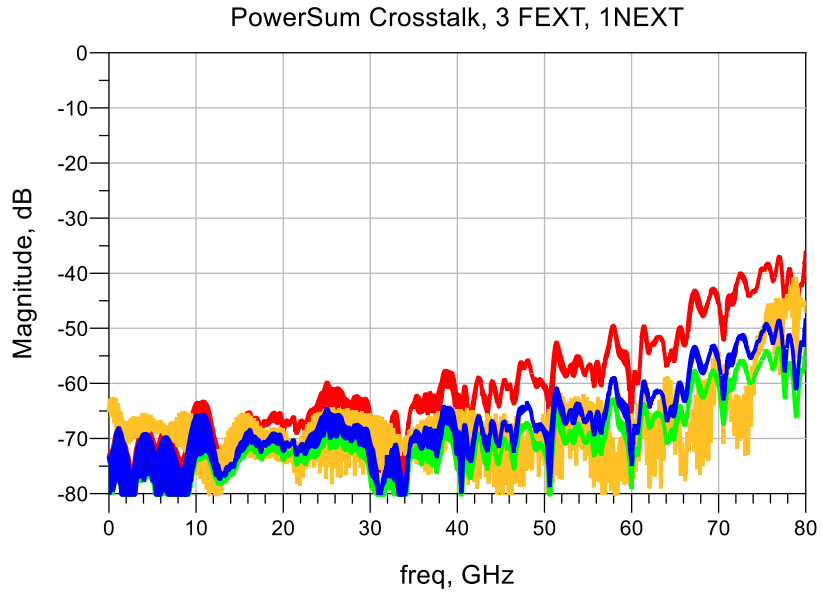
- Cabled backplane connector to cabled backplane connector
- Cable Termination to cabled backplane connector
- Updated BGA footprint + breakout, 0.9-1.0mm pitch
- Host Loss,~3.7dB, ~8dB and ~9.8dB @ 53.125GHz
  - Host Loss includes BGA escape and traces
- All components are at room temperature
- Channels do not include additional skew beyond whatever is part of design.

Performance Comparison

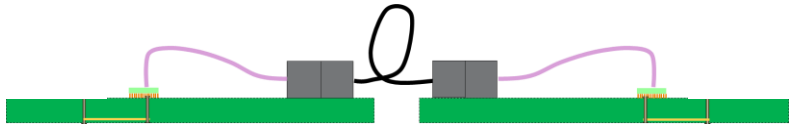




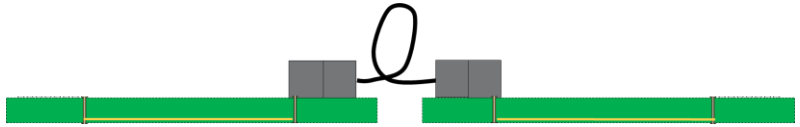
	TP0 – TP5 IL, dB @53.125GHz
Ch1	27.4
Ch2	19.3
Ch3	28.0
Ch4	31.4



Ch1: Cabled Line Card 7.85dB



Ch2: PCB Line Card 3.8dB
Ch3: PCB Line Card 8.0dB
Ch4: PCB Line Card 9.8dB



Crosstalk pinmap*

F
F V N
F

*BGA crosstalk contribution only includes FEXT

Simulated results are provided to 80 Ghz, but channel bandwidth is assumed to be 67 Ghz max.

Summary

- Simulation results have been provided for 200G TP0-TP5 channels with –
  - Various host loss options resulting in TP0-TP5 loss ranging from ~19 to 32dB
  - Includes traditional PCB based as well as cabled host architecture
- Not a final position on component or channel performance, further development is in process
- Intent is to provide meaningful support for addition of an 802.3dj backplane objective
- Touchstone files for data presented will be shared with the IEEE802.3dj community for COM analysis as we refine and finalize the COM parameters.