

Update to IEEE P802.3dj 200Gbps/lane AUI C2M channels

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Intel

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Contributors

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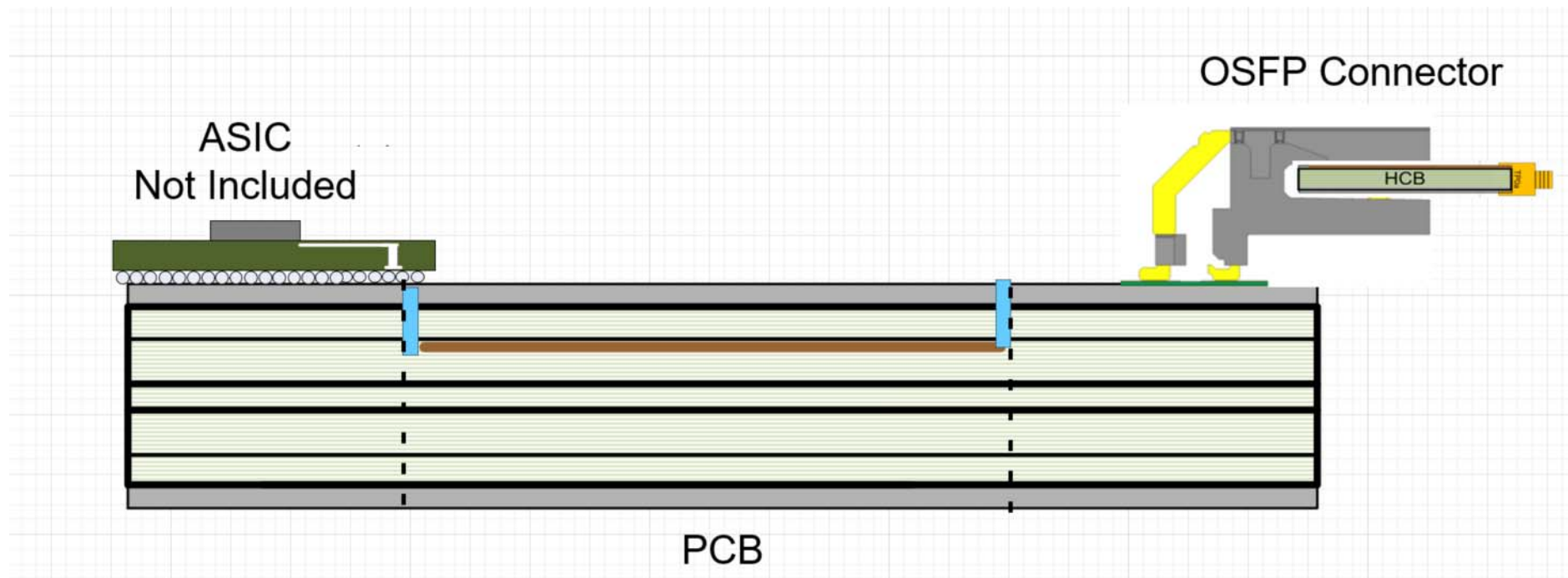
Objective

- Follow up on the presentation [akinwale 3df elec 01 220921.pdf](#)

Description

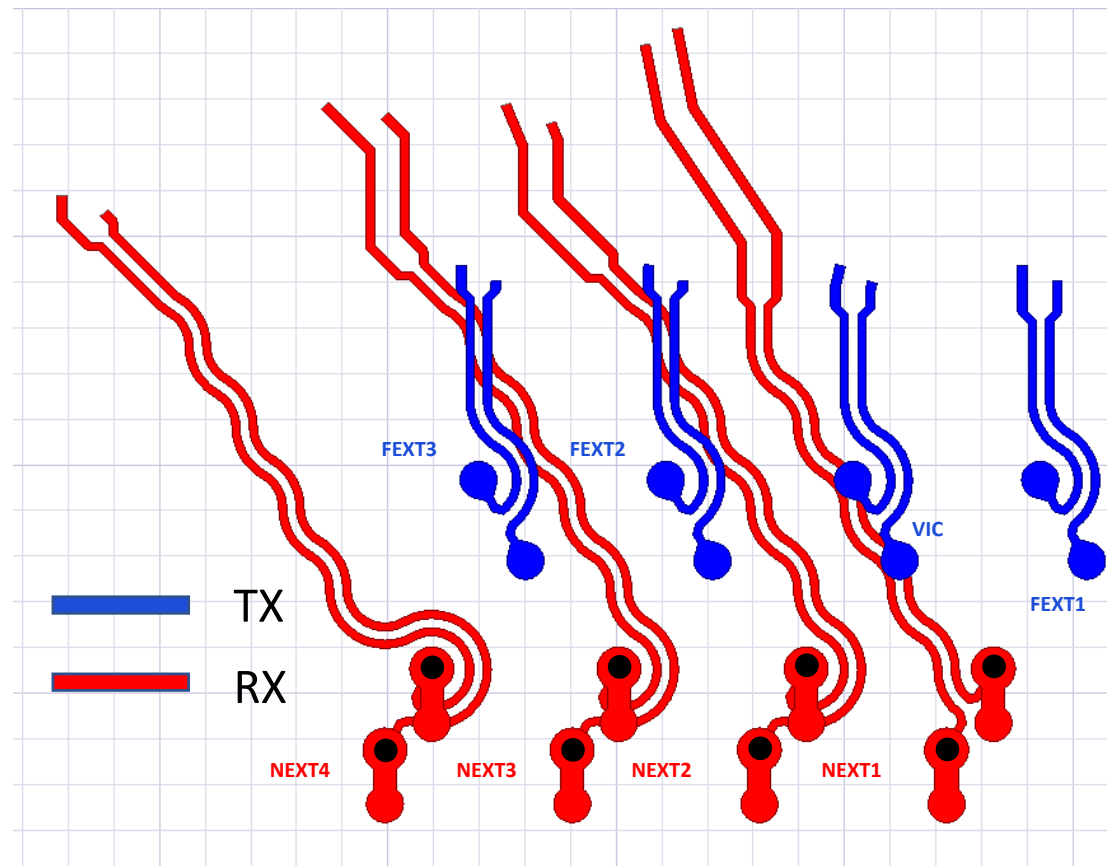
- Simulation of 200Gbps/Lane Chip-to-Module AUI using updated concept connector
- Increased number of aggressors
 - FEXT: Increased from 1 aggressor to 3 aggressors
 - NEXT: Increased from 2 aggressors to 4 aggressors
- Includes BGA escape model.
 - BGA ball not included (Prior model included the ball)
- 3 Host PCB impedance corners provided
 - 85 ohms, 93 ohms and 100 ohms
- Does NOT include Package or Silicon structures
- This v3 supersedes prior contributed v2 C2M AUI channels ([akinwale_3df_elec_01_220921.pdf](#))

Convention C2M Host (TP0 to TP1a)



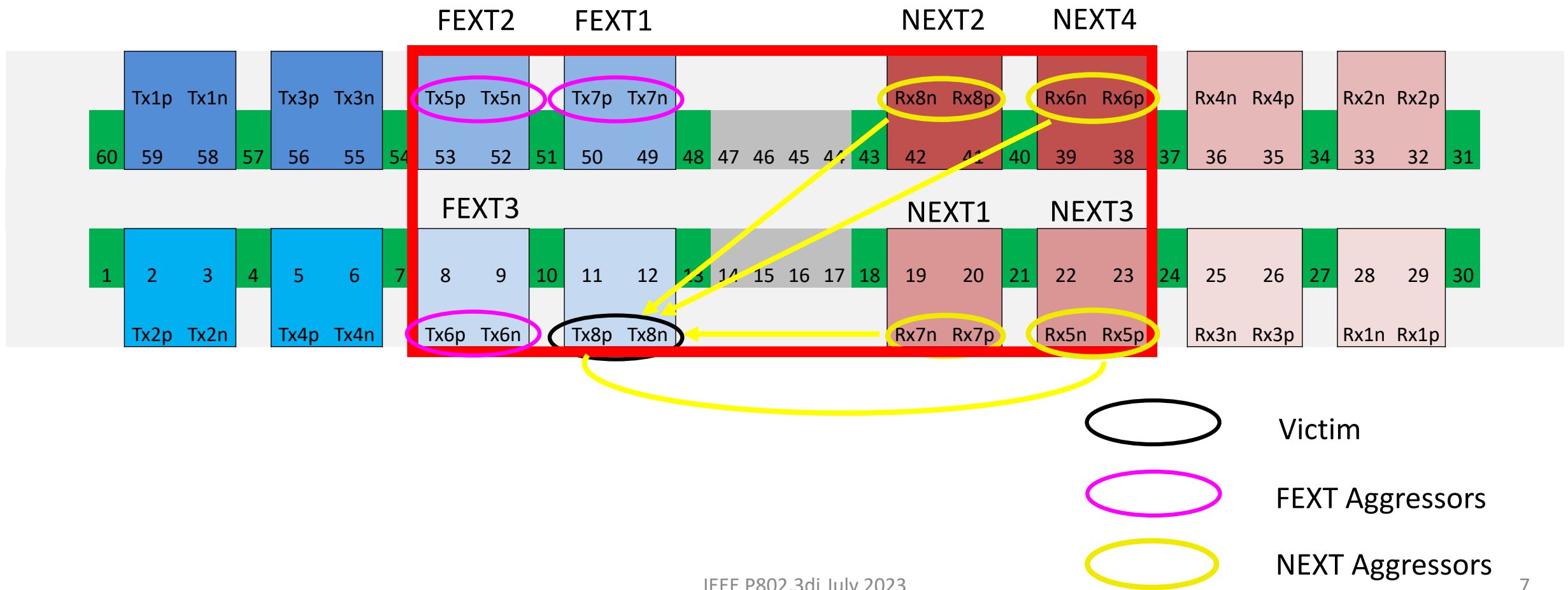
- **Updated** SMT OSFP 200Gbps/lane Connector
- Host Via Length: Tx (10 mils) and Rx (20 mils), uVias, no stub
- Host Loss: Swept from 0.5in to 13in, ~1.6dB/in loss @53.125GHz, (85 ohms/ 93 ohms/100 ohms)
- Module Loss: 2in, ~1.6dB/in loss @53.125GHz, 93 ohms
- BGA footprint and escape included. BGA ball **is not included**
- 4 Tx and 4 Tx Pairs. 3 FEXT and 4 NEXT Aggressors

PCB BGA Escape



OSFP Pin MAP

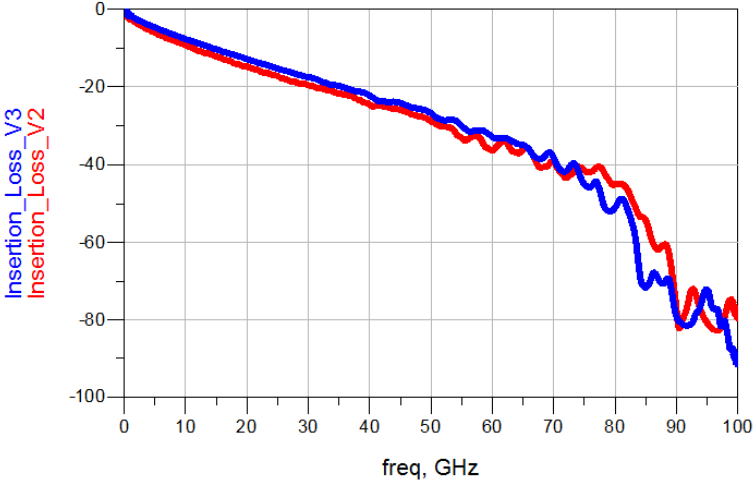
Pairs included in the channel construction



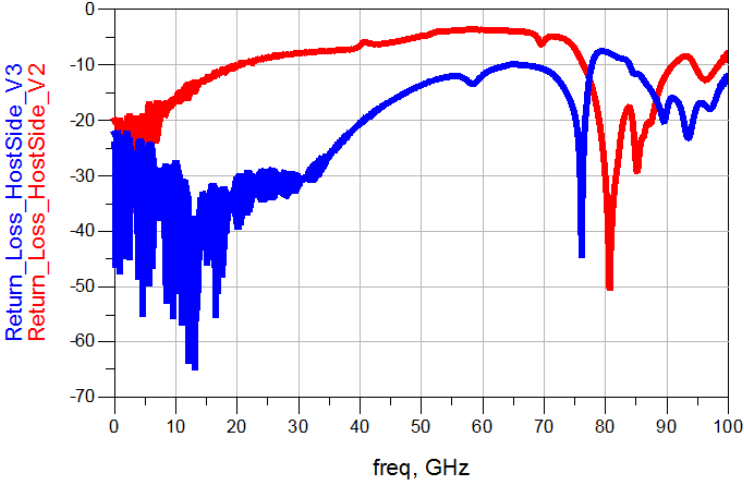
V2 = channel from [akinwale 3df elec 01 220921.pdf](#)
V3 = updated channel

Channel Comparison -13in

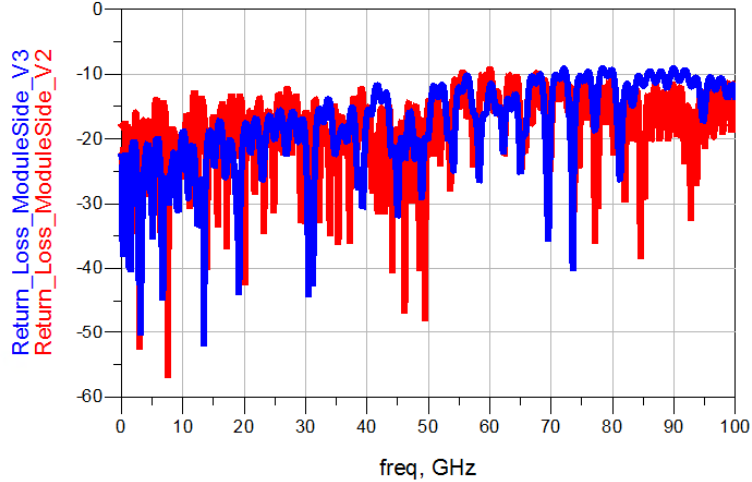
Insertion Loss – Zref = 50 ohms



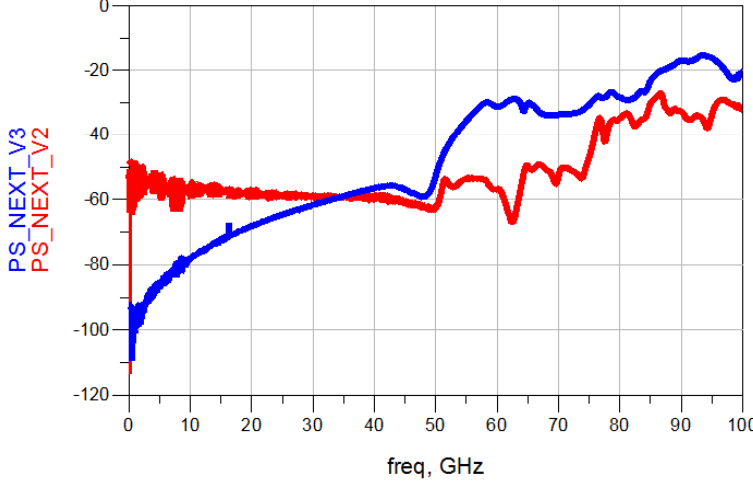
Return Loss – Host Side Zref = 50 ohms



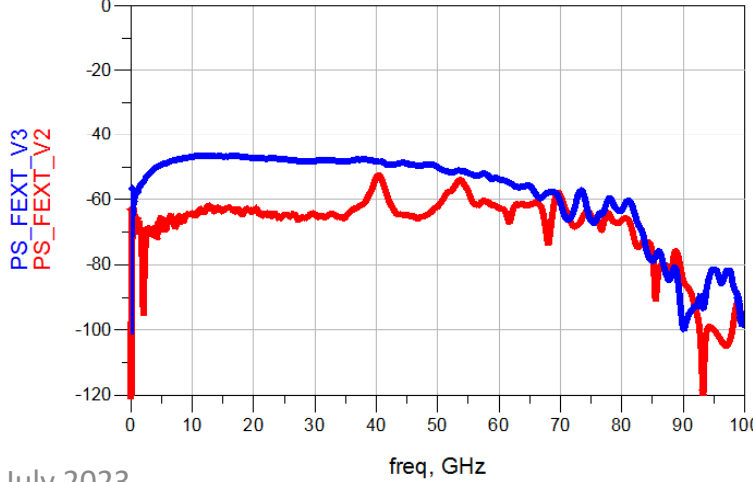
Return Loss – Module Side Zref = 50 ohms



Power Sum NEXT (4 Aggressors) Zref = 50 ohms

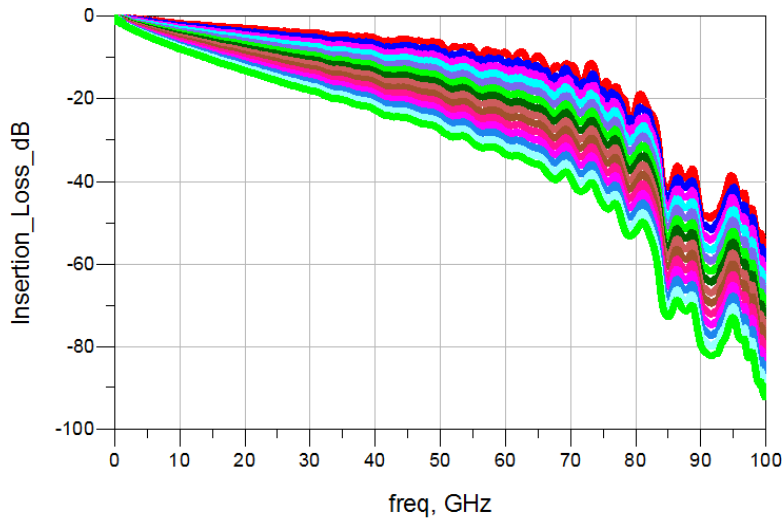


Power Sum FEXT (3 Aggressors) Zref = 50 ohms

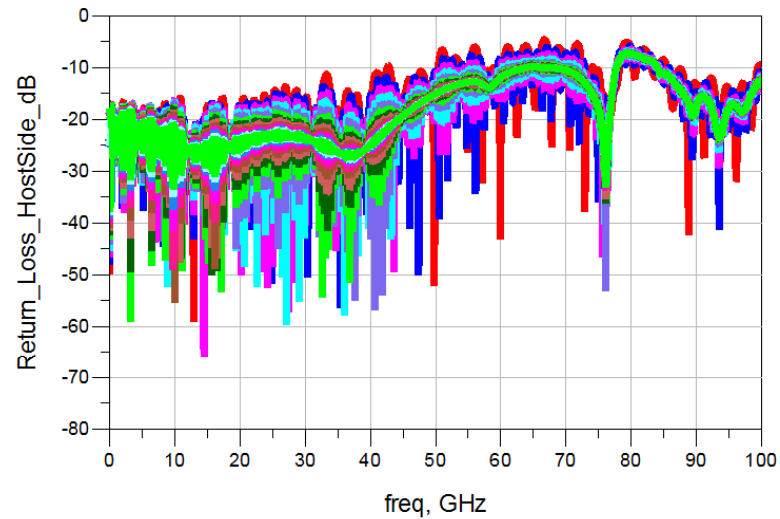


Channel Performance – PCB 93ohms

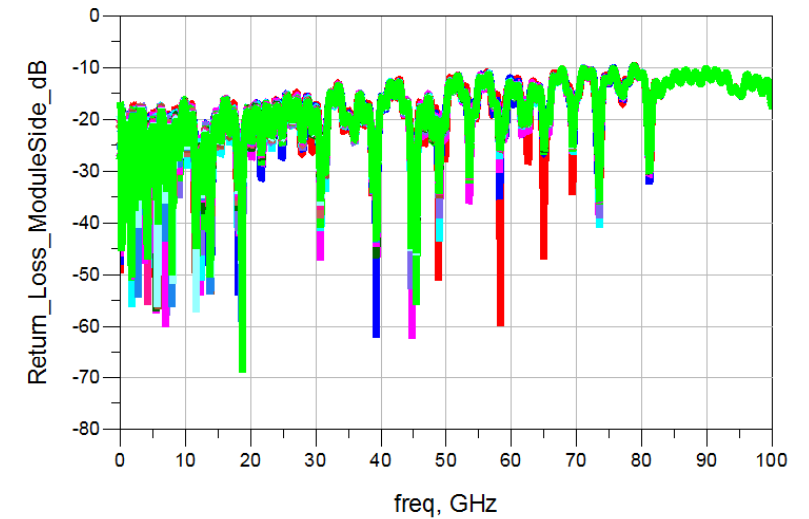
Insertion Loss – Zref = 50 ohms



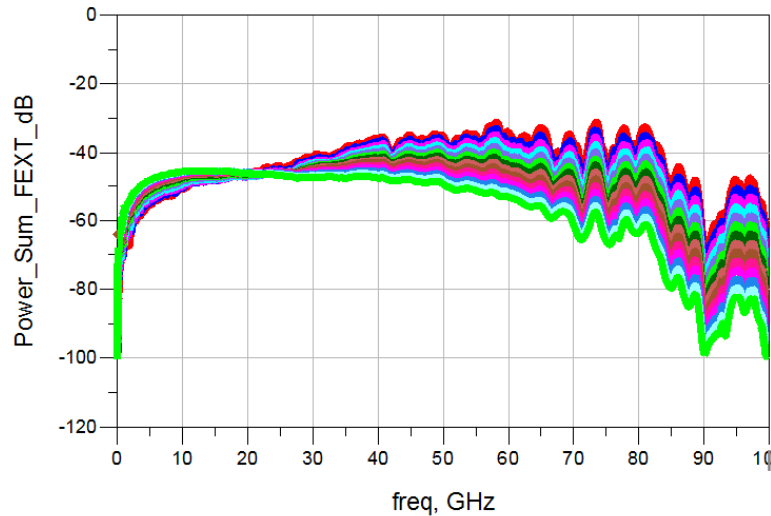
Return Loss – Host Side Zref = 50 ohms



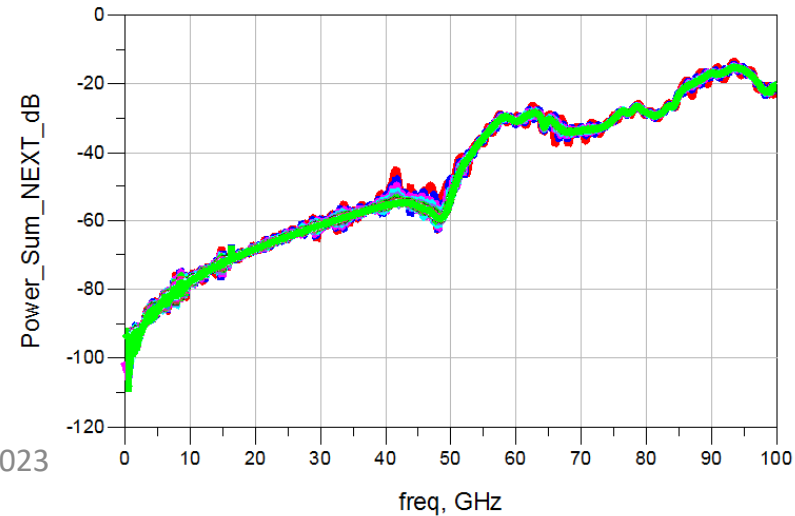
Return Loss – Module Side Zref = 50 ohms



Power Sum FEXT (3 Aggressors) Zref = 50 ohms



Power Sum NEXT (4 Aggressors) Zref = 50 ohms



COM Channel Characteristic Summary

PCB_Length	fitted_IL_dB_at_Fnq	ERL	ICN_mV	MDNEXT_ICN_92_46_mV	MDFEXT_ICN_92_47_mV
0p5in	7.2	13.4	2.5	0.4	2.5
1p0in	8.0	13.8	2.4	0.4	2.3
1p5in	8.8	14.2	2.2	0.3	2.2
2p0in	9.6	14.5	2.1	0.3	2.1
2p5in	10.4	14.8	2.1	0.3	2.0
3p0in	11.2	15.1	2.0	0.3	2.0
3p5in	12.1	15.3	2.0	0.3	1.9
4p0in	12.9	15.6	1.9	0.3	1.9
4p5in	13.7	15.8	1.9	0.3	1.9
5p0in	14.5	16.1	1.9	0.3	1.9
5p5in	15.3	16.2	1.9	0.3	1.8
6p0in	16.1	16.4	1.9	0.3	1.8
6p5in	16.9	16.6	1.9	0.3	1.8
7p0in	17.7	16.8	1.9	0.3	1.8
7p5in	18.5	16.9	1.9	0.3	1.8
8p0in	19.3	17.1	1.9	0.3	1.8
8p5in	20.1	17.2	1.9	0.3	1.8
9p0in	20.9	17.3	1.9	0.3	1.8
9p5in	21.6	17.4	1.9	0.3	1.8
10p0in	22.4	17.5	1.9	0.3	1.8
10p5in	23.2	17.6	1.9	0.3	1.8
11p0in	24.0	17.7	1.9	0.3	1.8
11p5in	24.8	17.8	1.9	0.3	1.8
12p0in	25.6	17.8	1.9	0.3	1.8
12p5in	26.4	17.9	1.9	0.3	1.8
13p0in	27.1	18.0	1.8	0.3	1.8

Summary

- ❑ Provided improved 200Gbps/Lance AUI C2M channels
 - ❑ Removes BGA ball
 - ❑ Updates connector model
- ❑ Channels include BGA Via, PCB trace, PCB Via, OSFP connector and HCB
- ❑ Channel loss ranges from 7dB to 29dB, not inclusive of package
 - ❑ TP0 to TP1a

File Naming Convention

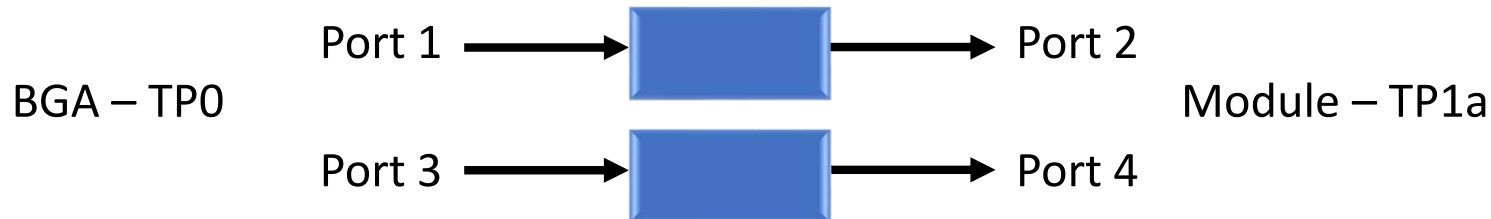
C2M_PCB_XXohms_0p5in_20230620_v3

PCB Host Impedance

85 ohms / 93 ohms / 100 ohms

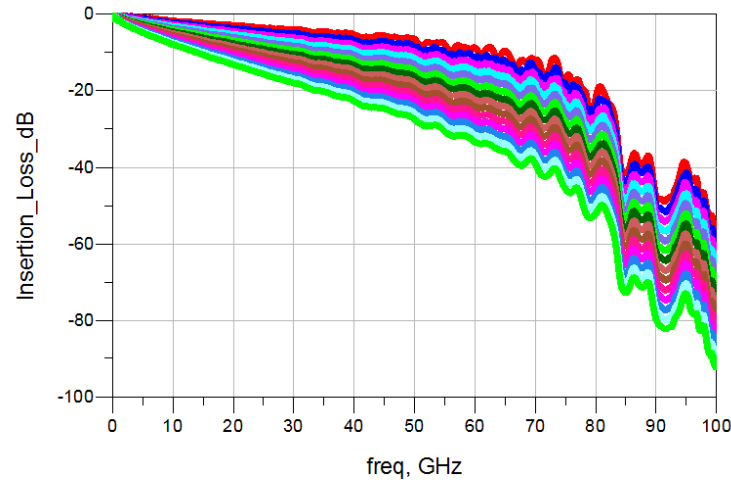
PCB Length

0.5 in – 13 in

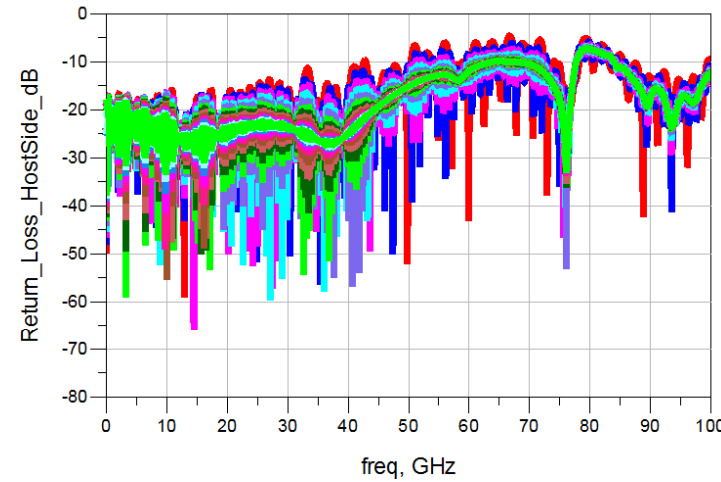


Channel Performance – PCB 85ohms

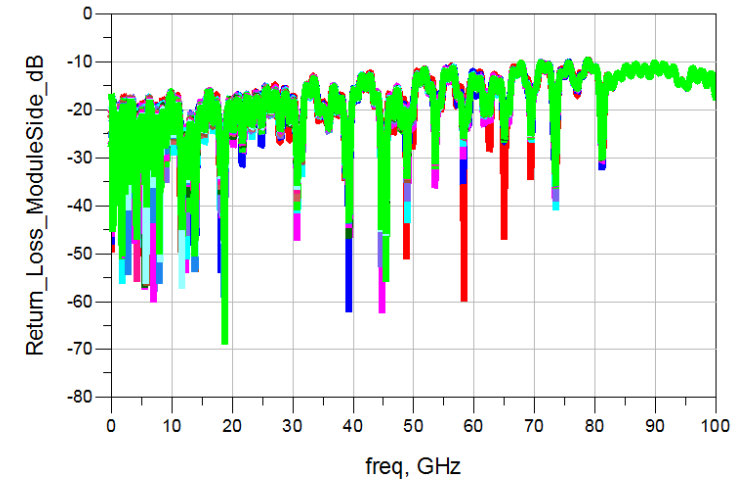
Insertion Loss – Zref = 50 ohms



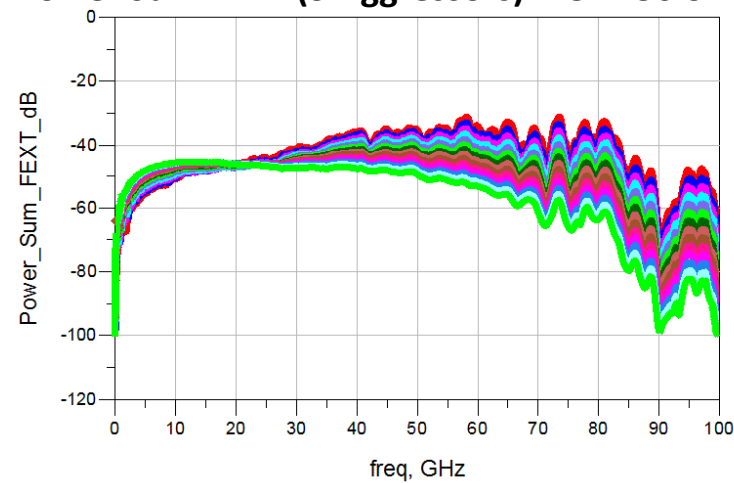
Return Loss – Host Side Zref = 50 ohms



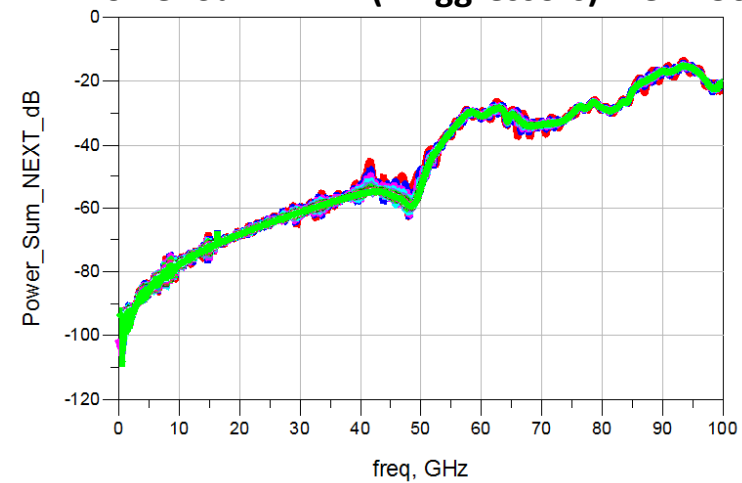
Return Loss – Module Side Zref = 50 ohms



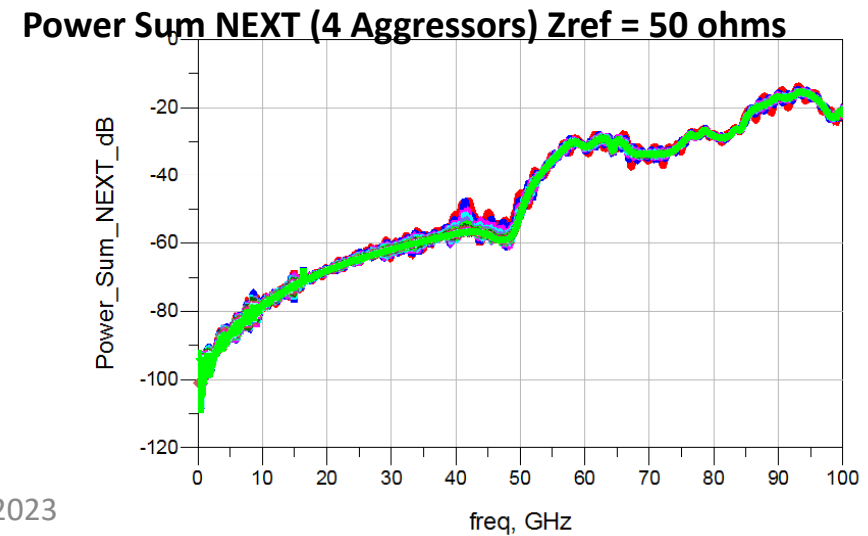
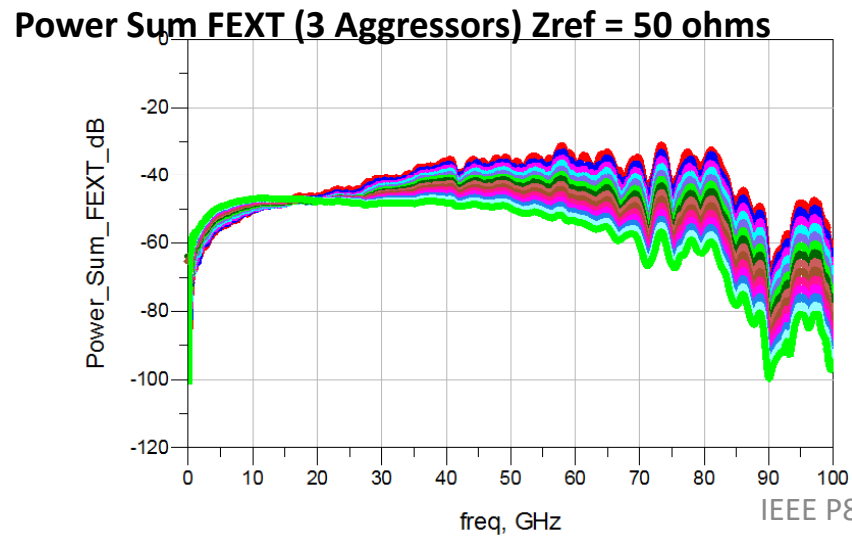
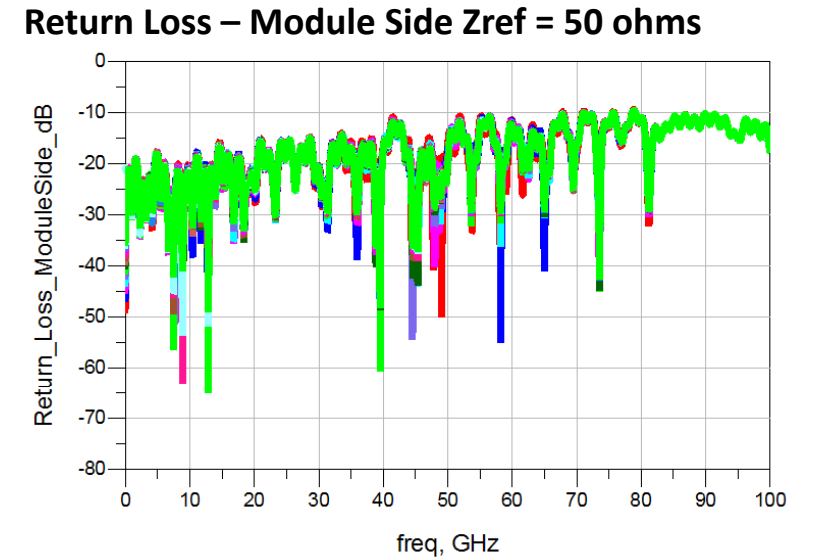
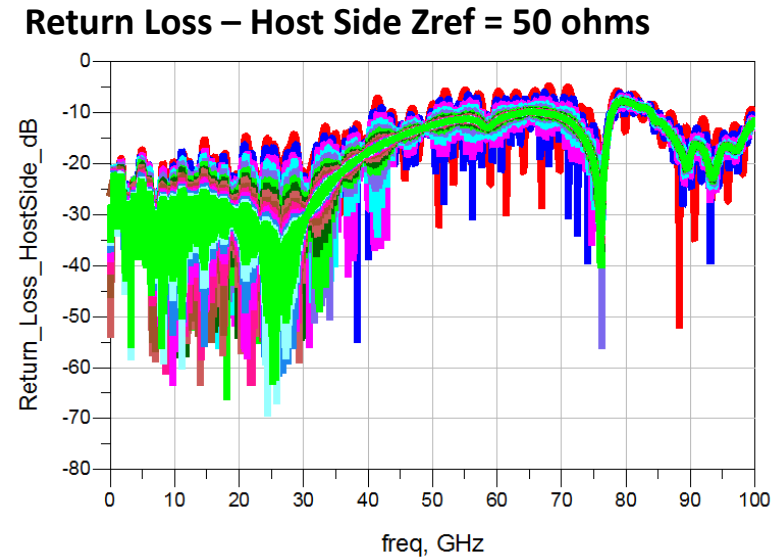
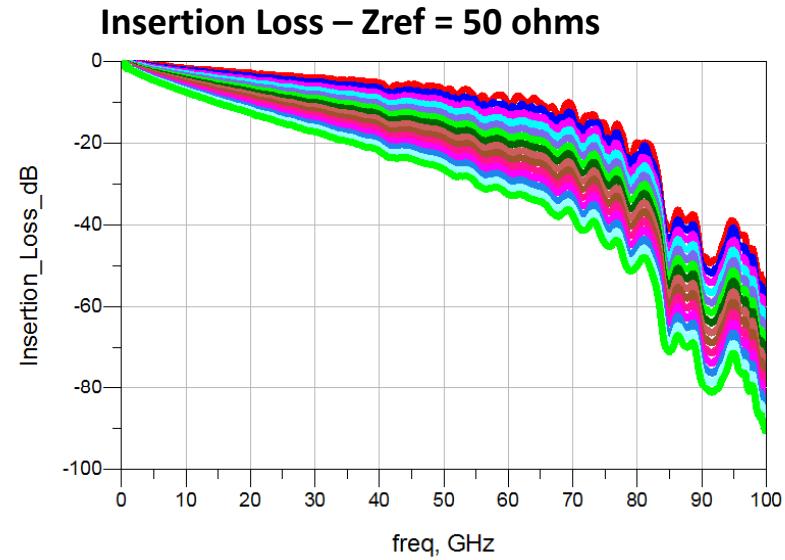
Power Sum FEXT (3 Aggressors) Zref = 50 ohms



Power Sum NEXT (4 Aggressors) Zref = 50 ohms



Channel Performance – PCB 100ohms



COM SETTINGS

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4;0 0 0]	nF	[TX RX]
L_s	[.12.15 .14;0 0 0]	nH	[TX RX]
C_b	[.3e-4 0]	nF	[TX RX]
z_p select	[1 2 3]		[test cases to run]
z_p (TX)	[12 30 45; 1 1 1 ; 0.1 0.1 0.1 ; 0.58 0.58 0.58]	mm	[test cases]
z_p (NEXT)	[0 0 0; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]
z_p (FEXT)	[12 30 45; 1 1 1 ; 0.1 0.1 0.1 ; 0.58 0.58 0.58]	mm	[test cases]
z_p (RX)	[0 0 0; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 50]	Ohm	[TX RX]
A_v	0.387	V	vp/vf=
A_fe	0.387	V	vp/vf=
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.55	*fb	
c(0)	0.65		min
c(-1)	[-0.2;0.02;0]		[min:step:max]
c(-2)	[0;.02;0.1]		[min:step:max]
c(-3)	[-0.1;.02;0]		[min:step:max]
c(1)	[-0.2;0.02;0]		[min:step:max]
N_b	8	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	0.15		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15		As/dfe2..N_b
g_DC	[-13;1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6;1:0]		[min:step:max]
f_HP_PZ	1.0625	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\c2m_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_fr55_TP1a_COM_mode	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	10	dB
VEC Pass threshold	12	db
EH_min	0	Value
DER_0	1.00E-04	
T_r	4.71E-03	ns
FORCE_TR	1	logical
Min_VEO_Test	0	mV
PMD_type	C2M	
T_O	50	mUI
samples_for_C2M	100	samples/UI
EW	1	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	1	
N_bx	8	UI
fixture delay time	[0 0.2e-9]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	4.10E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	
11-2022 BenArtsi pkg		
highlighted are under re-consideration		
mli_3df_02_220316		

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	0.02	UI
ICN parameters		
f_v	0.278	Fb
f_f	0.278	Fb
f_n	0.278	Fb
f_2	58.438	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	6	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	120	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.1	rss tail tap limit
N_tail_start	9	(UI) start of tail taps limit
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

config_com_ieee8023_93a=df_200G_PAM4_fr55_C2M_TP1a_11_2022.xlsx

[mellitz 3dj elec 02 230223](#)