A path forward following lack of complete consensus on COM package models

Liav Ben-Artsi – Marvell Technology

Contributor: Based on former work done by Richard Mellitz and jointly presented in benartsi_3df_01_2211



□Recap on package model as presented Nov 2022

□What can we agree upon?! - Justifying model construction

Package material loss consensus discussions ongoing, will be presented as part of consensus group presentation



Recap on Assumptions/Former Work

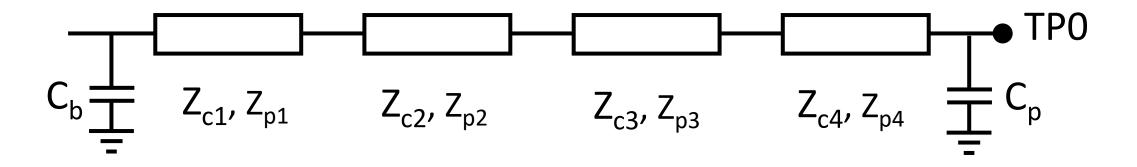
- A realistic package loss/mm for 40μ dielectric height + 27μ-45μ-27μ trace geometry was given as 0.21dB/mm (we will discuss possible cases of lowering loss); Other parts of the package model were optimistic - ~800μ core, 7-2-7 stack-up, no impedance manufacturing tolerance, etc.
- □ Routing of Tx, or Rx lanes can easily be 40-45mm long, or even longer in congestion cases Length in this stage to be TBD
- I 3D extraction was matched with a four sections package model for COM much better correlation than with 802.3ck model
 - The 4 sections are required to match higher frequency characteristics compared to 802.3ck. – Resulting COM run consistently better than when concatenating to extracted model (~0.2dB – probably some fine details are still left out when using matched model) – Slide #12

802.3dj suggested COM Model - Iteratively adjust γ_0 , a_1 , a_2 , τ

COM MODEL: IEEE802.3 ANNEX 93A.1.2.3

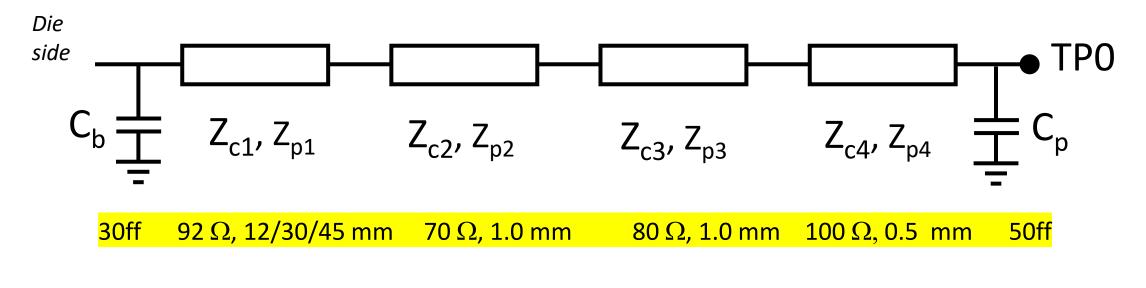
Also tune

• Z_p, Z_c, C_b, C_p



COM Model Results

COM MODEL: IEEE802.3 ANNEX 93A.1.2.3



 $\gamma_0 = 0$, $a_1 = 0.0008455$, $a_2 = 0.000340225$, $\tau = 0.00644805$

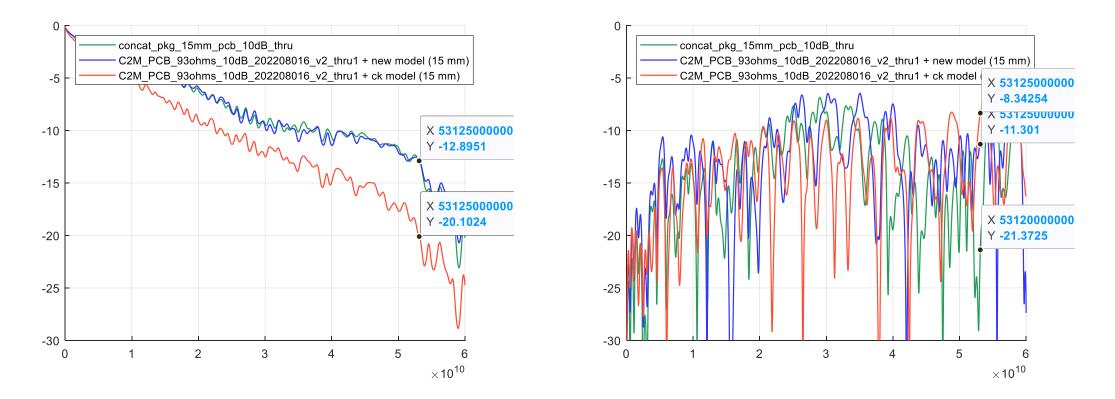
Frequency Domain Comparison

(After concatenation, how well does the "model" channel match "HFSS" channel?)

Example case: 15 mm + 10 dB

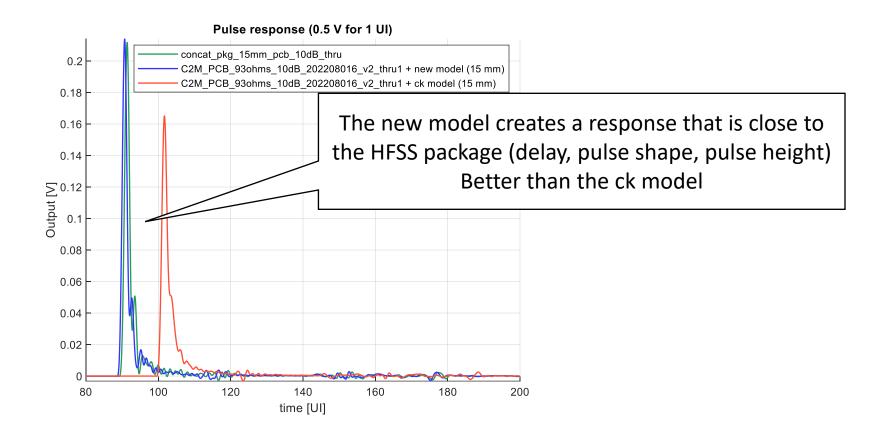
ILDD

RLDD



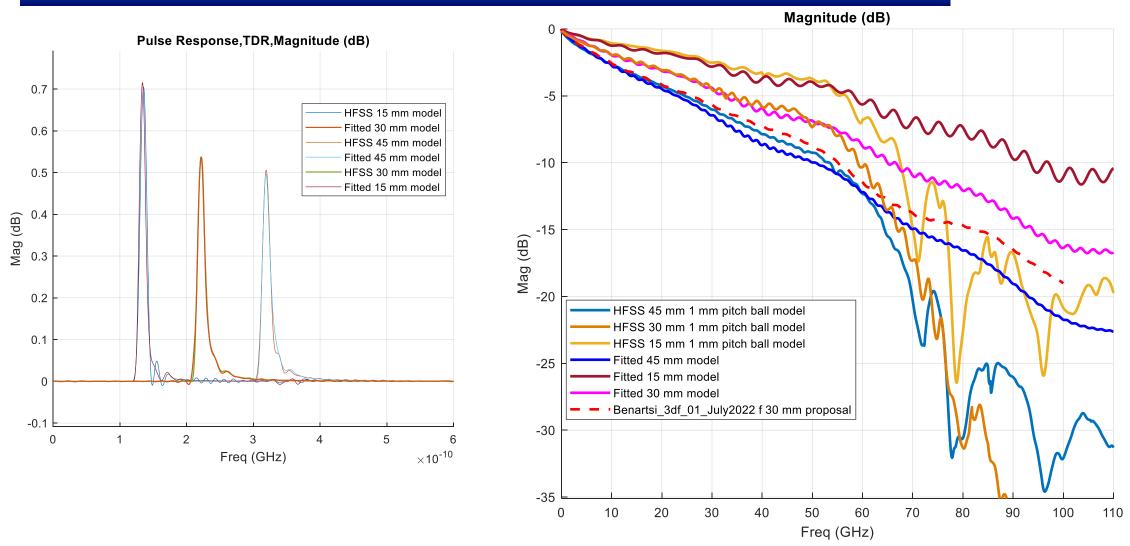
Time domain SBR comparison

Example case: 15 mm + 10 dB



Graphic View of Results

IF PACKAGE HAS A ROLL-OFF - NOT IN FITTED COM MODEL



COM Config Settings

C2M EXAMPLE

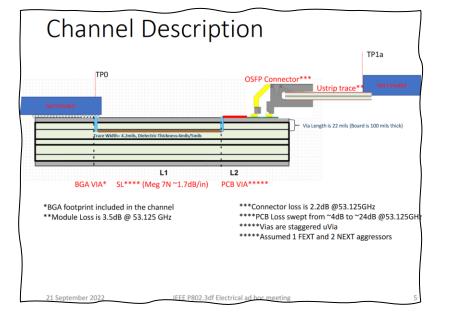
Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm

C_d	[0.4e-4 0.9e-4 1.1e-4;000]			
L_s	[.12.15.14;000]			
C_b	[.3e-4 0]			
z_p select	[1 2 3]			
z_p (TX)	[12 30 45 ; 1 1 1 ; 1 1 1 ; 0.5 0.5 0.5]			
z_p (NEXT)	[000;000;000;000]			
z_p (FEXT)	[12 30 45 ; 1 1 1 ; 0.1 0.1 0.1 ; 0.58 0.58 0.58]			
z_p (RX)	[000;000;000;000]			
С_р	[0.5e-4 0]			

Test Cases

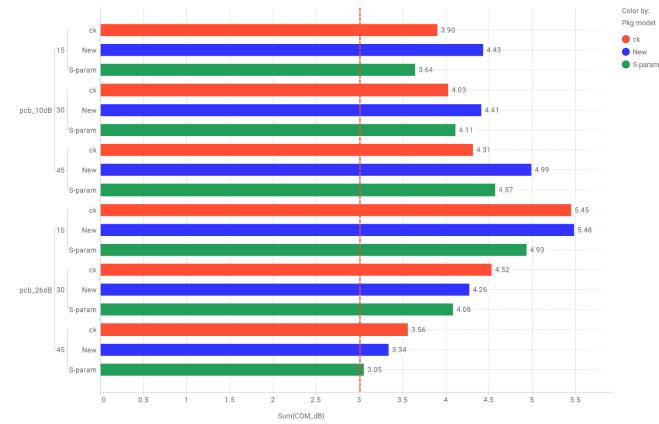
	z _p =15	z _p =30	z _p =45
C2M_PCB_93ohms_10dB_202208016_v2_thru1.s4p	concat_pkg_15mm_pcb_10dB	concat_pkg_30mm_pcb_10dB	concat_pkg_45mm_pcb_10dB
C2M_PCB_93ohms_26dB_202208016_v2_thru1.s4p	concat_pkg_15mm_pcb_26dB	concat_pkg_30mm_pcb_26dB	concat_pkg_45mm_pcb_26dB

Channels are from <u>akinwale 3df elec 01 220921</u>



COM Results Comparison

COM_dB per channel_id, host_pkg_trace_len, Pkg model



COM results with the updated fitted model (blue) are consistently higher than with HFSS S-parameter concatenation (green)

 The difference is usually 0.2-0.5 dB
 The "shortest" combination is an exception

 For the high loss channel, the new model is closer to the HFSS results than the ck model (red)

 For the low loss channel, the ck model had worse COM in 2 cases!

 The fitted model is somewhat

optimistic...?

but in a more consistent way than the old model

Conclusions & Recommendations

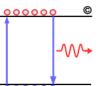
- Providing a package model for COM to account for 200Gbps PAM4 signaling requires "high amount of" details in higher frequency than before
- □ Former .ck package model failed to supply required accuracy
- A suggested higher details model showed relatively consistent results compared to concatenated 3D extracted model
- Recommend adopting new, 4 TL model as the COM model; parameters yet to be decided according to consensus group work



Ali Ghiasi's Suggested BGA Configuration

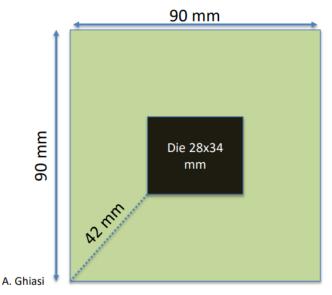
WWW.IEEE802.ORG/3/DF/PUBLIC/22_10/22_0927/GHIASI_3DF_01_220927.PDF

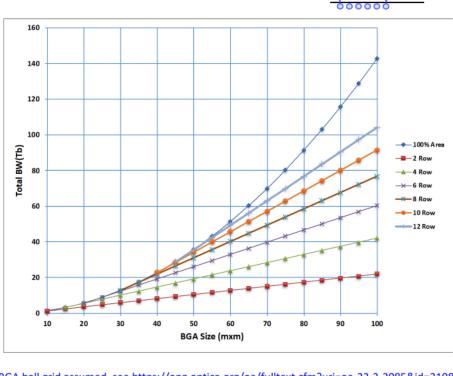
Hypothetical 512x200G Switch



Likely will require 90x90 BGA

- − Provides V2 for FEXT pairs
- Provides 2 balls separations for NEXT
- For the hypothetical switch with 28x34 mm die results in 42 mm long substrate trace!





For the BGA ball grid assumed, see https://opg.optica.org/oe/fulltext.cfm?uri=oe-23-3-2085&id=310831

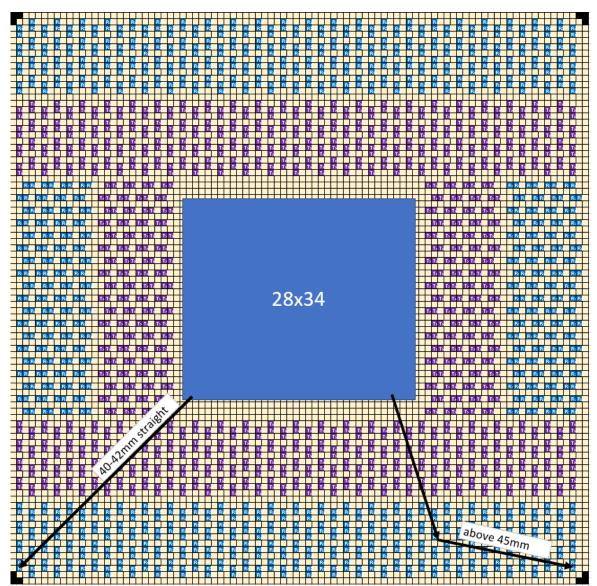
802.3df Task Force

10

Full Population of 512 Tx Lanes & 512 Rx Lanes

92X92 BALL-OUT MATRIX ACCORDING

- No overhead was taken for CMOS, PCIe, or any addition signals
- Routing of Tx, or Rx lanes can easily be 40-45mm long, or even longer in congestion cases



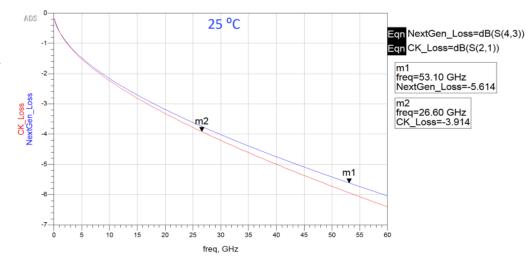
Expected Losses of Next Gen Material

□ ghiasi_3df_01_220927.pdf: "benartsi_3df_01b_2207 uses best ABF conventional 27-45-27 µm construction and reports trace loss of 0.31 dB/mm @53 GHz (loss include transition via/BGA) • Benartsi loss expect to be lower ~0.22 dB/mm after accounting for improved surface roughness"

CK and Next Gen Package Losses for Reduced Trace Width

Adjust trace width to 27 μm as suggested by <u>benartsi_3df_01b_2207</u>

- Use the same Hurray surface roughness model that was previously matched best ABF film in 2018/2019
- Reduced trace width may be required for some high radix switches implementations
- Losses for **27** μ m wide 92.5 Ω stripline traces
 - For best ABF film from 2018/2019 the CK 30 mm package trace loss is 3.94 dB or 0.13 dB/mm instead of assumed 0.109 dB/mm assumed loss @26.56 GHz
 - Next Gen 2022 ABF film the 30 mm package trace loss would be 5.6 dB or 0.19 dB/mm @53.1 GHz (6.75 dB or ~0.225 dB/mm 90°C).



Loss Reported is only for the trace and does not include transition Via/BGA

IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

000000

-

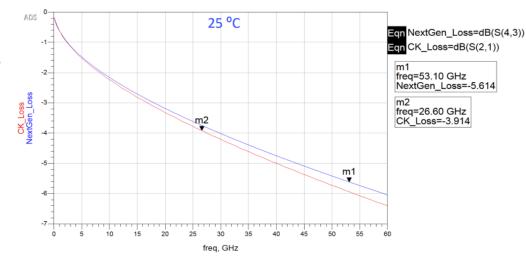
Expected Losses of Next Gen Material

□ ghiasi_3df_01_220927.pdf: "benartsi_3df_01b_2207 uses best ABF conventional 27-45-27 µm construction and reports trace loss of 0.31 dB/mm @53 GHz (loss include transition via/BGA) • Benartsi loss expect to be lower ~0.22 dB/mm after accounting for improved surface roughness"

CK and Next Gen Package Losses for Reduced Trace Width

Adjust trace width to 27 μm as suggested by <u>benartsi_3df_01b_2207</u>

- Use the same Hurray surface roughness model that was previously matched best ABF film in 2018/2019
- Reduced trace width may be required for some high radix switches implementations
- Losses for **27** μ m wide 92.5 Ω stripline traces
 - For best ABF film from 2018/2019 the CK 30 mm package trace loss is 3.94 dB or 0.13 dB/mm instead of assumed 0.109 dB/mm assumed loss @26.56 GHz
 - Next Gen 2022 ABF film the 30 mm package trace loss would be 5.6 dB or 0.19 dB/mm @53.1 GHz (6.75 dB or ~0.225 dB/mm 90°C).



Loss Reported is only for the trace and does not include transition Via/BGA

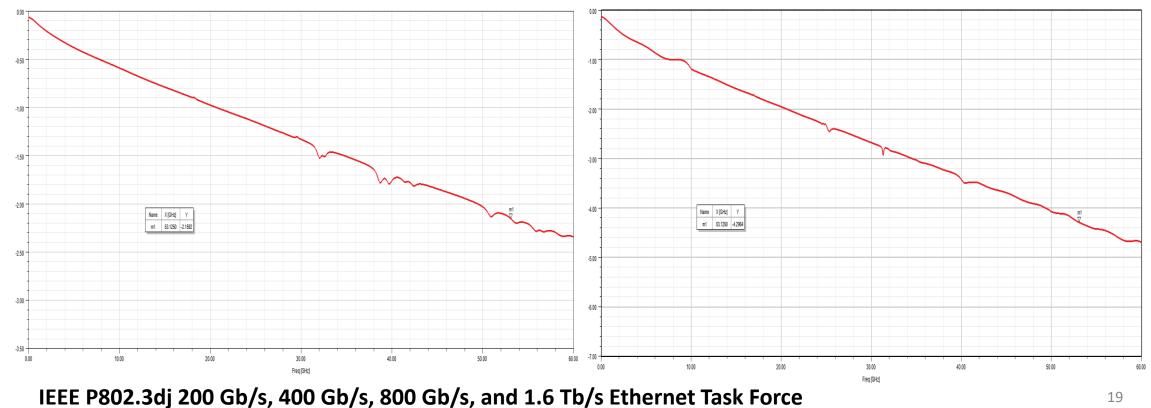
IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

000000

-

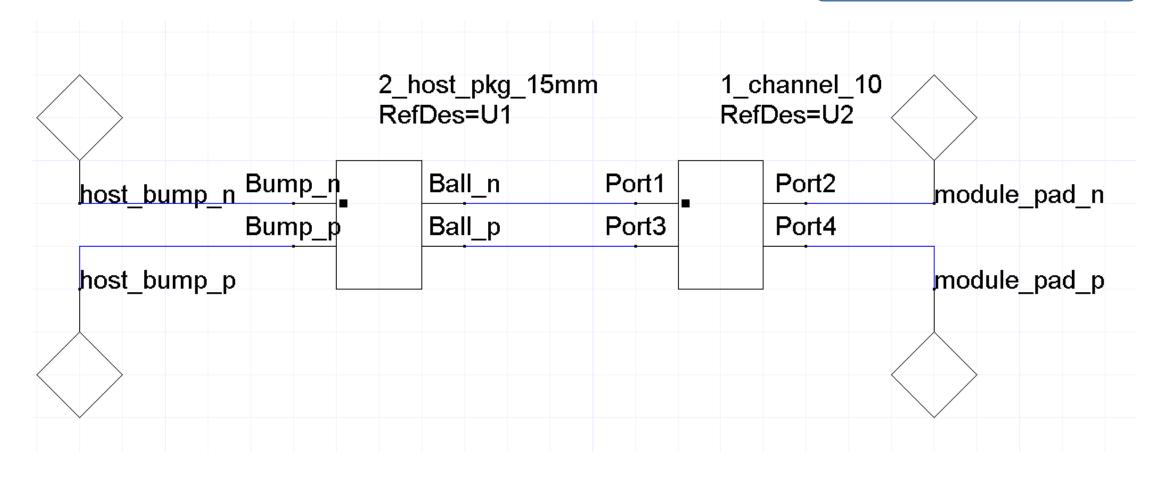
Adjusted Extraction of Loss/mm

- **Δ** 40μ dielectric height ; 15μ copper thickness ; 27μ-45μ-27μ trace geometry
- □ The resulting loss/mm \approx 0.21dB
- Conductivity was updated to correlate and account for high temperature
- Correlates to the expected and measured loss/mm



S-parameter Concatenation (HFSS model)

Example case: 15 mm + 10 dB



TDR Verification of the Concatenation



COM model parameters (pkg model added only at Tx/TP0 side)

parameters Setting Units Information I/O control Table 93A-3 parameters Parameter Setting Units Units f_b 106.25 GBd DISPLAY_WINDOW 0 logical Parameter 2 08.455e-4 3.40225e-4] Units f_min 0.02 GHz CSV_REPORT 1 logical package_t1_su 6.448E-03 ns/mm Delta_f 0.02 GHz CSV_REPORT 1 logical package_t2_c [92.92,707,80.80,100.100] Ohm C_d [40.90.10;40.90.10]*1e-6 nF [TX RX] PortOrder [13.24] Ist f_v 0.371 *Fb						i			-		:
Parameter Setting Units Information $f_{, 0}$ 1082.5 Gid Usits Information logical Parameter Setting Units $f_{, 0}$ 0.02 Gits Setting Units Information $f_{, 0}$ 0.02 Gits Setting Usits Setting Usits $f_{, 0}$ 1000000000000000000000000000000000000	Table 93A-1 parameters				I/O control			Ν	Table 93A–3 parameters		
$ \begin{array}{ c c c c c } \hline 1 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.64 & 0.02 & 0.06 & 0.02 & 0.06 & 0.02 & 0.06 & 0.02 & 0.06 & 0.02 & 0.06 &$		Setting	Units	Information	DIAGNOSTICS	1	logical	11	Parameter	Setting	Units
- $ -$ <td>f_b</td> <td>106.25</td> <td>GBd</td> <td></td> <td>DISPLAY_WINDOW</td> <td>0</td> <td>logical</td> <td></td> <td></td> <td>[0 8.455e-4 3.40225e-4]</td> <td></td>	f_b	106.25	GBd		DISPLAY_WINDOW	0	logical			[0 8.455e-4 3.40225e-4]	
Lot of the set of th	f_min	0.02	GHz		CSV_REPORT		logical		package_tl_tau	6.448E-03	ns/mm
C_0 $(20)01101, 20, 40, 0101, 20, 40, mm int int< int int int<$	Delta_f	0.02	GHz		RESULT_DIR		Path	V	package_Z_c	[92 92; 70 70; 80 80; 100 100]	Ohm
C. b. IBM-6 38e-6] nf IT.R8] RUMAG C2M, eval rf. 0.371 OHt f regeneration finst colum $xp(tr)$ (153.045, 111, 113, 05.05, 0.5) mm Itest cases] (00, 000, 000, 000, 000, 000, 000, 000,	C_d	[40 90 110; 40 90 110]*1e-6	nF	[TX RX]	SAVE_FIGURES	0	logical				
z pellect is 30 45; 111; 113; 05.05, 0.5] mm [text cases] OM_CONTRIBUTION 0 logical $z_p(RX)$ [153 045; 111; 113; 05.05, 0.6] mm [text cases] - </td <td>L_s</td> <td>[0.13 0.15 0.14; 0.13 0.15 0.14]</td> <td>nH</td> <td>[TX RX]</td> <td>Port Order</td> <td>[1324]</td> <td></td> <td></td> <td>f_v</td> <td>0.371</td> <td>*Fb</td>	L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]	Port Order	[1324]			f_v	0.371	*Fb
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	C_b	[30e-6 30e-6]	nF	[TX RX]	RUNTAG	C2M_eval_			f_f	0.371	GHz f_r specified in first colum
$z_p(NX)$ 0.05 mm ltest cases $1/2$ $1/2$ $3/2$ $3/2$ $3/2$ $z_p(NX)$ $1000,000,000,000$ mm ltest cases $1/2$ $3/2$	z_p select			[test cases to run]	COM_CONTRIBUTION	0	logical		f_n	0.371	GHz
z.p. (FEX) [153 065; 11:1; 11:0; 0505; 0] mm [test cases] z.p. (FX) [000; 000; 000; 000; 000] mm [test cases] c C.p. [300-60] nF [TX RX] c R,0 50 Ohm c c R,0 0.03 Ohm [TX RX] c A, fe 0.413 V c c A, fe 0.606 V c c M 32 Samp/Ul Tr 6.00E 03 ns FOCC_MM 100 Samp/Ul TR_0 logical c c M 32 Samp/Ul TDR logical c c T_0 50 mul c c c c c C(0) 0.5 min filter cases] TB logical c c T_0 50 mul c c c c c c C(0) 0.55 min	z_p (TX)	• • • • • • • • • • • • • • • • • • •	mm	[test cases]	Local Search	2			f_2	58.4375	GHz
Z.p. (FX1) C.p. OS1 mm Itest cases] mm Itest cases] mm Itest cases] mm	z_p (NEXT)	[0 0 0; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]	Operational				A_ft	0.600	v
C_p[50e-60]nF[TX RX]R_050OhmR_d[5050]OhmA, w0.413VA, fe0.413VL4 0 L4 0 Samples for C2M100Samp/UlT_050mU1Ac_CM, RMS0VIt100Samp/UlAc_CM, RMS0V10.55*fb1(-1)(-3.40.020)(-1)(-3.40.020)(-4)(0.001.0.03)(-1)(-3.40.020)(-4)(0.001.0.03)(-1)(-3.40.020)(-1) </td <td>z_p (FEXT)</td> <td></td> <td>mm</td> <td>[test cases]</td> <td>COM Pass threshold</td> <td>3</td> <td>dB</td> <td></td> <td>A_nt</td> <td>0.600</td> <td>v</td>	z_p (FEXT)		mm	[test cases]	COM Pass threshold	3	dB		A_nt	0.600	v
C.p Jobevul In (1X RX] CRU Pass threshold 7.3 OB Curves gaussan frama (1) Character Chararet Character Chararet	z_p (RX)	[0 0 0; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]							
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$				[TX RX]	ERL Pass threshold	7.3	dB			Gaussian	gaussian. triangle, rectangle
A v 0.413 V T r 6.00E-03 ns Table 92-12 parameters main A, fe 0.413 V 1 5 PRD, Upp C2 PRD, Upp PRD, Upp $C2$ $Doard, U, gamma, d, 1, 20$ $O0579$ nrm $SAPE, OCN (FEXM)$ 1 $logical$ $Doard, U, gamma, d, 1, 20$	R_0	50	Ohm						sigma_r	0.02	sigma in UI fo or gaus Wind
A_1^{ee} 0.413 V V A_ne 0.608 V V L 4 V $OBCE_TR$ 1 5 M 32 $3mp/U$ $OBCE_TR$ 1 100 $Oard$ $12 gameter$ $Setting$ $Oard$ $12 gameter$ $Setting$ $Samples$ for $C2M$ 100 $Samp/U$ $OBCE_TR$ 1 $10gical$ $Oard$ $12 gameter$ $Setting$ $Oard$ Oar				[TX RX]							
A_ne 0.608 V PMD_type C2C board_tl_gamma0_a1_a2 [0.8206e-04_9.5909e-05] L 4											
L 4 M M 32 SampUl M 32 SampUl TO Samples for 2CM 100 SampLot (CMAR) 1 logical TO 50 mUl PLC/CM 0 logical 2, bp (TX) 407 mm AC_CM_RMS 0 V (test case) TDR 1 logical 2, bp (TX) 407 mm c(0) 0.5 min FRL 1 logical 2, bp (FX) 407 mm c(-1) [-0.34:0.020] (minstep:maxl TR TDR 0.01 ns C_1 0 nf c(-3) [-0.06:0.020] (minstep:maxl N 1200 1 1 logical f.c(-4) [0:0.01:0.03] (minstep:maxl 0 1 1 logical 1 Nb.x 0 1 1 logical b_max(1) 1 As/dffe1 As/dffe1 Nb.x 0 UI Nbx							5				
M 32 Samp/U SAVE_CONFIG2MAT 1 logical $z_c C$ 100 Ohm r_O 50 mU PLOT_CM 0 logical $z_b p(RKT)$ 407 mm AC_CM_RMS 0 V [test cases] TDR 1 logical $z_b p(RKT)$ 407 mm ftr and Eq Imm Imm Imm TDR 1 logical $z_b p(RKT)$ 407 mm c(0) 0.5 min min Imminstep:maxi RR_L_ONLY 0 logical C_0 0 nft c(-3) [-0.06.0.02:0] [minstep:maxi] M 1200 Imminstep:maxi rho_x 0.618 C_1 0 nft b_max(1) 1 As/dffe1 As/dffe1 N_b N_b 2 Maximum Maximum Maximum Mifter Method Maximum Mifter Method Maximum Maximum Maximum Maximum Maximum Maximum Maximum Maximum </td <td></td> <td></td> <td>V</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>			V								
$\begin{array}{c c c c c c c c c c c c c c c c c c c $											
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		-									-
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $						0	logical			-	
filter and Eq Image: Second seco										-	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		0	V	[test cases]			· ·			-	
C(0) 0.5 min c(-1) (-0.34.002:0) [min:step:max] c(-2) [0:002:0.14] [min:step:max] c(-3) (-0.06:0.02:0) [min:step:max] c(-4) [0:0.01:0.03] [min:step:max] c(-4) [0:0.01:0.03] [min:step:max] c(1) [-0.10:02:0] [min:step:max] fxture delay time [0:0] h_max(1) 1 As/dtfe1 h_max(2.N_b) 0.3 As/dtfe1 h_min(2.N,b) 0.15 As/dtfe1 f_z 42.5 GHz g_DC [-181::8] dB f_p1 42.5 GHz g_D_LHP [-3:0.5.0] [min:step:max]			+0				· ·				
C(-1) [-0.34:0.02:0] [min:step:max] N 1200 Include PCB 0 logical c(-2) [0.0.02:0.14] [min:step:max] beta x 0 include PCB 0 logical c(-3) [-0.060.02:0] [min:step:max] rho_x 0.618 include PCB 0 logical c(-4) [0:0.01:0.03] [min:step:max] fnxure delay time [0:0] 1 include PCB 0 logical c(-4) [0:0.01:0.03] [min:step:max] fnxure delay time [0:0] 1 ifferent for each test fixture ifferent for each test fixture c(1) [-0.1:0.02:0] [min:step:max] TDR_W_TXPKG 0 UI b_max[1] 1 As/dffe1 N_bx 0 UI Udated for 802.3df/dj igma 8BN step SOR-03 V g_DC [-181::-8] dB [min:step:max] Sigma 8BN step 5.00E-03 V Noise, jitter igma 8BN step igma 8L A,DD 0.02 UI A,DD A,DD QL			*fb	an ta			-	-	-		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $							ns				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $								-	Include PCB	0	logical
c(-4) [0:0.01:0.03] [min:step:max] fixture delay time [0 0] [port1 port2] c(1) [-0.1:0.02:0] [min:step:max] fixture delay time [0 0] 1 N_b 24 UI TDR_W_TXPKG 0 UI b_max(1) 1 As/dffe1 N_bx 0 UI b_max(1,1) 0.3 As/dffe1 Tukey_Window 1 b_min[2.N_b) -0.15 As/dffe1 Receiver testing											
c(1) [-0.1:0.02:0] [min:step:max] TDR_W_TXPKG 0 I N_b 24 UI N_b 0 UI b_max(1) 1 As/dffe1 N_b 0 UI b_max(2.N_b) 0.3 As/dffe1 Receiver testing I b_min(2.N_b) -0.15 As/dffe1 Rx_CALIBRATION 0 logical g_DC [-18:1:8] dB [min:step:max] Sigma 8BN step 5.00E-03 V f_z 42.5 GHz Sigma RI 0.01 UI f_p2 106:25 GHz A,DD 0.02 UI eta_0 4.00E-09 V12/GHz g.DC HP [-3:0.5:0] SNR_TX 32.5 dB							[port1 port2	2	different for each test fixtur	e	
N_b 24 UI N_bx 0 UI b_max(1) 1 As/dffe1 Tukey_Window 1 updated for 802.3df/dj CM b_max(2N_b) 0.3 As/dffe1 Tukey_Window 1 updated for 802.3df/dj CM b_min(1) 0.3 As/dffe1 Receiver testing Receiver testing Receiver testing b_min(1) 0.3 As/dfe1 Sigma BBN step 5.00E-03 V g_DC [181:-8] dB [min:step:max] Noise, jitter Sigma RJ 0.01 UI f_p1 42.5 GHz ADD 0.02 UI Sigma RJ 0.01 UI f_p2 106.25 GHz Eta_0 4.00E-09 V^2Q/GHz GHz g_D_LHP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB GHz	c(1)	[-0.1:0.02:0]		[min:sten:max]	TDR W TXPKG						
b_max(1) 1 As/dffe1 Tukey_Window 1 updated for 802.3df/dj (2M) b_max(2.N_b) 0.3 As/dffe1 Receiver testing Image: Comparison of the participation of the pa			UI	[ministepimox]			UI				
b_max[2N_b] 0.3 As/dfe2N_b Receiver testing b_min(1) 0.3 As/dfe1 RX_CALIBRATION 0 logical b_min(2N_b) -0.15 As/dfe2N_b RX_CALIBRATION 0 logical b_min(2N_b) -0.15 As/dfe1 Sigma BBN step 5.00E-03 V g_DC [-18:1:-8] dB [min:step:max] Nolse, jitter				As/dffe1	_						
b_min(1) 0.3 As/dffe1 RX_CALIBRATION 0 logical b_min(1) -0.15 As/dffe1 Sigma BBN step 5.00E-03 V g_DC [18:1:-8] dB (min:step:max) Sigma BBN step 5.00E-03 V f_2 42.5 GHz Sigma BBN step 5.00E-03 V f_p1 42.5 GHz Sigma RU 0.01 UI f_p2 106:25 GHz A,DD 0.02 UI eta_0 4.00E-09 V*2/GHz SNR_TX 32.5 dB	b max(2N b)			As/dfe2N b	Receiver testing			1'			
b_min[2N_b] -0.15 As/dfe2N_b Sigma BBN step 5.00E-03 V g_DC [-18:1:-8] dB [min:step:max] Noise, jitter f_z 42.5 GHz sigma_RU 0.01 UI f_p1 42.5 GHz eta_0 4.00E-09 V^2/GHz g_DC_HP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB					•	0	logical	1.			
g_DC [-18:1:-8] dB [min:step:max] Noise, jitter f_z 42.5 GHz sigma_RJ 0.01 UI f_p1 42.5 GHz A DD 0.02 UI f_p2 106.25 GHz eta_0 4.00E-09 V^A2/GHz g_DC_HP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB	,										
f_z 42.5 GHz sigma_RI 0.01 UI f_p1 42.5 GHz A_DD 0.02 UI f_p2 106.25 GHz eta_0 4.00E-09 V^22/GHz g_DC_HP [-3.0.5.0] [min:step:max] SNR_TX 32.5 dB			dB					1			
f_p1 42.5 GHz A_DD 0.02 UI f_p2 106.25 GHz eta_0 4.00E-09 V^2/GHz g_DC_HP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB			-	,,		0.01	UI	1			
f_p2 106.25 GHz eta_0 4.00E-09 V^2/GHz g_DC_HP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB								1			
g_DC_HP [-3:0.5:0] [min:step:max] SNR_TX 32.5 dB								1			
				[min:step:max]				1			
			GHz					1			

Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f		UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
N_tail_start	24	
B float RSS MAX	0.1	

Thank You!