802.3dj - CR
Considerations for
Insertion Loss Budget Baseline

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Purpose

- Consideration for CR insertion loss budget baseline
  - Compliance test points and insertion losses
    - die-to-die
    - Cable assembly, TX/RX, test fixtures

Contributors

- Michael Rowlands, Sam Kocsis; Amphenol
- Nathan Tracy, Megha Shanbhag; TE Connectivity
- Scott Sommers; Molex
- Adee Ran; Cisco Systems
- Richard Mellitz; Samtec
- Mike Li, Kent Lusted; Intel

Supporters

- Nathan Tracy, Megha Shanbhag; TE Connectivity
- Scott Sommers; Molex
- Mike Li; Intel
- Priyank Shukla; Synopsys
- Ali Ghiasi; Ghiasi Quantum
- Howard Heck; Intel

CR Compliance Test Points

- Normative: Cable Assembly, Transmitter, Receiver, Test Fixtures
- Informative: Die-to-die, TP0 to TP5, recommended device package + host IL

Table XXX–X—Test points

Test points	Description
$TP0_d$ to $TP5_d$	The channel including the device package, the host transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure xxx-x. The cable assembly test fixture of Annex xxxx, or its equivalent, is required for measuring the cable assembly specifications in xxx.x at TP1 and TP4.
$TP0_d$ to TP2 TP3 to $TP5_d$	A mated connector pair has been included in both the transmitter and receiver specifications defined in xxx.x and xxx.x. The recommended maximum insertion loss from $TP0_d$ to TP2 or from TP3 to $TP5_d$ including the test fixture is provided in xxx.x.
TP2	Unless specified otherwise, all transmitter measurements defined in xxx.x are made at TP2 utilizing the test fixture specified in Annex xxxx.
TP3	Unless specified otherwise, all receiver measurements and tests defined in xxxx are made at TP3 utilizing the test fixture specified in Annex xxxx.

$TP0_d$- $TP5_d$ Insertion Loss (informative Annex)

- Align with KR die-to-die insertion loss ≤ 40 dB

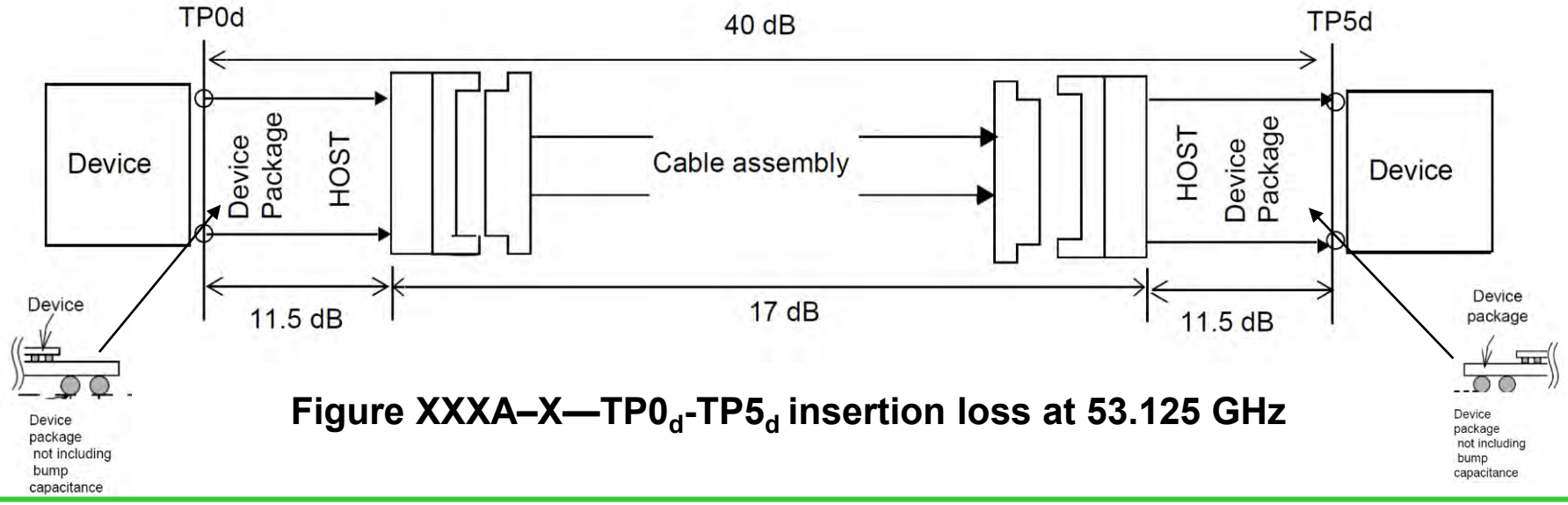

Figure XXXA–X—$TP0_d$-$TP5_d$ insertion loss at 53.125 GHz

Straw Poll #1

I would support a one-lane 200 GbE, a two-lane 400 GbE, a four-lane 800 GbE, and an eight-lane 1.6 TbE backplane objective of the form:

"Define a physical layer specification that supports [n*200] Gb/s operation over [n] lanes over electrical backplanes supporting a die-to-die insertion loss ≤ X dB at 53.125 GHz"

Results (all) Y: 56 , N: 11 , A: 14

X = 40

Channels which reached X of 40 dB with 7 dB loss packages

- ❑ Channels in this presentation (with key)
  - tracy_3dj_02_2303 (T)
    - TE_KR3_2p7dBPCB_10in30AWG_Conn_1m26AWG_Conn_10in30AWG_2p7dBPCB_THRU
  - weaver_3dj_02_2303 (w)
    - KR_ch_3in_PCB_NPC_300mm_29AWG_BP_800mm_27AWG_thru
  - mellitz_3dj_02_2303 (m)
    - KRCA_wXTALK_25_PCB-25-25_mm_FO-300-300_mm_CA-1000_mm_thru
  - mellitz_3dj_03_2303 (m)
    - KRCA_wXTALK_LD_25_PCB-25-25_mm_FO-300-300_mm_CA-1000_mm_thru
  - mellitz_3dj_02_elec_230504 (m)
    - KRCA_wXTALK_MX_4_PCB-25-25_mm_FO-200-200_mm_CA-200_mm_thru

IEEE P802.3df 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

mellitz_3dj_elec_04a_230504.pdf

$TP0_d$-TP2/TP3 Insertion Loss (informative Annex)

- Partition loss budget allocation for device package + host
- No change to test point reference TP2/TP3 i.e., testing of normative TX/RX

Annex 162A
(informative)

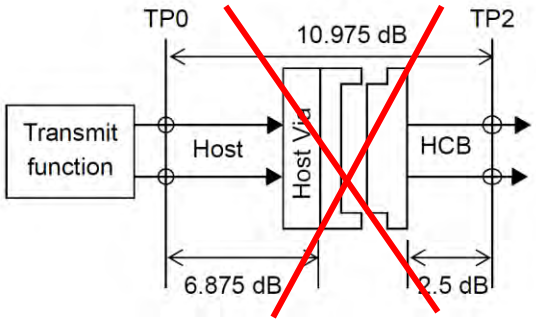

Table XXX–X—Test points

Test points	Description
$TP0_d$ to $TP5_d$	The channel including the device package, the host transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
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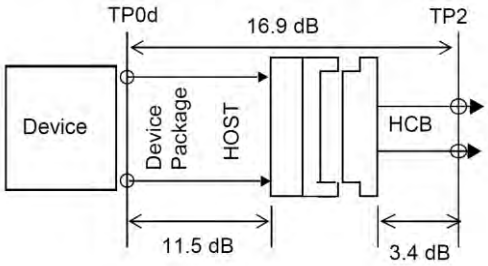
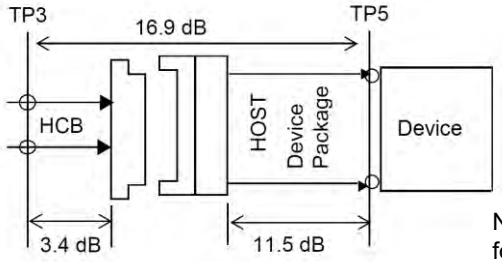
TP3	Unless specified otherwise, all receiver measurements and tests defined in xxxx are made at TP3 utilizing the test fixture specified in Annex xxxx.



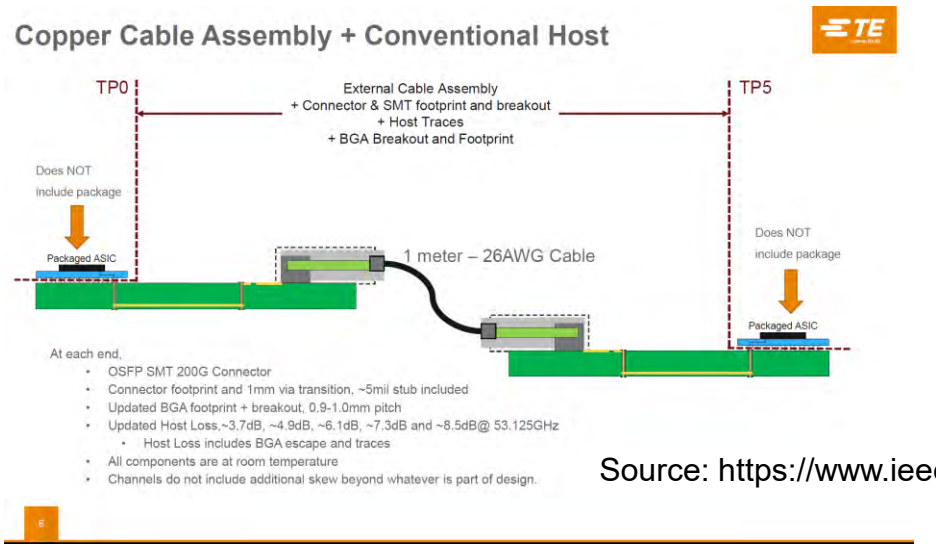


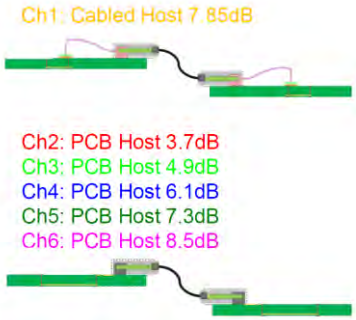
NOTE—The 11.5 dB ILdd includes allowance for BGA and connector footprint vias.
NOTE—Device package not including bump capacitance

Figure XXXA–X—$TP0_d$-TP2/TP3 Insertion loss at 53.125 GHz

Mated Cable Assembly - ≤17 dB @ 53.125 GHz

- Mated Cable Assembly ≤17 dB @ 53.125 GHz supported by contributions





	TP0 – TP5 IL, dB @53.125GHz
Ch1	28.4
Ch2	23.5
Ch3	25.9
Ch4	28.8
Ch5	30.8
Ch6	33.6

Source: https://www.ieee802.org/3/dj/public/23_05/shanbhag_3dj_01a_2305.pdf

CR Copper Cable Channel Configurations

Amphenol COMMUNICATIONS SOLUTIONS

Configuration	TP0 Side Host Loss (dB@53.125GHz)	Copper Cable Length (m)	TP5 Side Host Loss (dB@53.125GHz)	TP0-TP5 Loss (dB@53.125GHz)
1	8	1	8	30.75
2	10	1	10	34.51
3	4	1.5	4	26.65
4	3	1	9	26.74
5	9	1	3	26.74

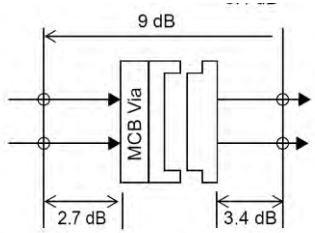
- Configurations 1 and 2 represent symmetric, switch-switch links
- Configuration 3 represents case with physical reach >1.5m
- Configurations 4 and 5 represent asymmetric, switch-server links

Package length adjusted to maintain 40dB "die-to-die" in each analysis

Source: https://www.ieee802.org/3/dj/public/23_05/kocsis_3dj_01a_2305.pdf

TP1-TP4 Cable Assembly- Mated Test Fixtures

- Need further discussions on test fixtures
  - inclusion of RF connector
  - Time gated propagation delay methods
- Consider test reference points $TP1_r$ and $TP4_r$

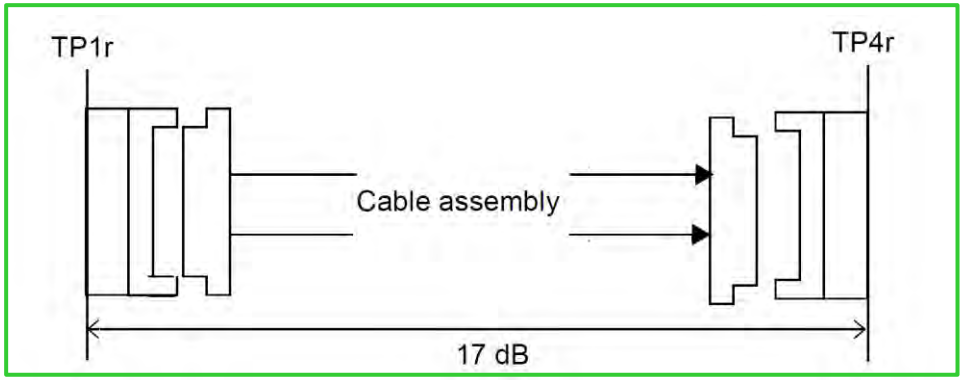


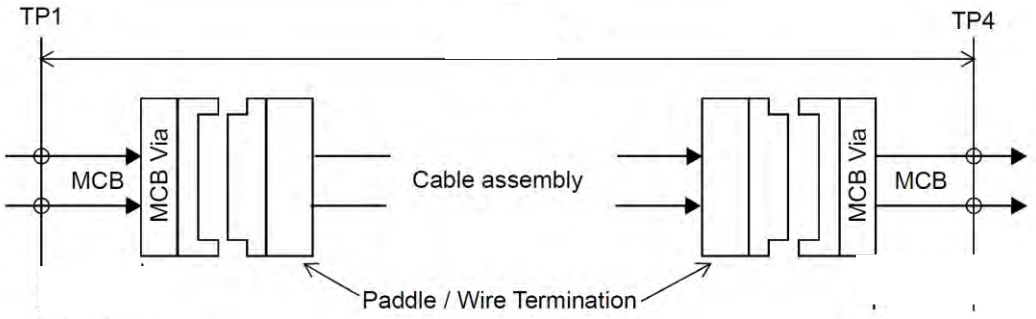
Mated cable assembly
and test point test fixture

NOTE—RF connector inclusion and MCB via allowance TBD

Source:
https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf

- Adopt cable assembly test point reference pending methodology





TP0-TP5

- XXX.X Transmitter characteristics at TP0
- The recommended transmitter characteristics at TP0 as measured at TP0v are described in XXX.X.
- XXX.X Receiver characteristics at TP5
- The recommended receiver characteristics at TP5 as measured at TP5v are describe in XXX.X.
- TP0-TP5 Min host insertion loss for all cable assemblies

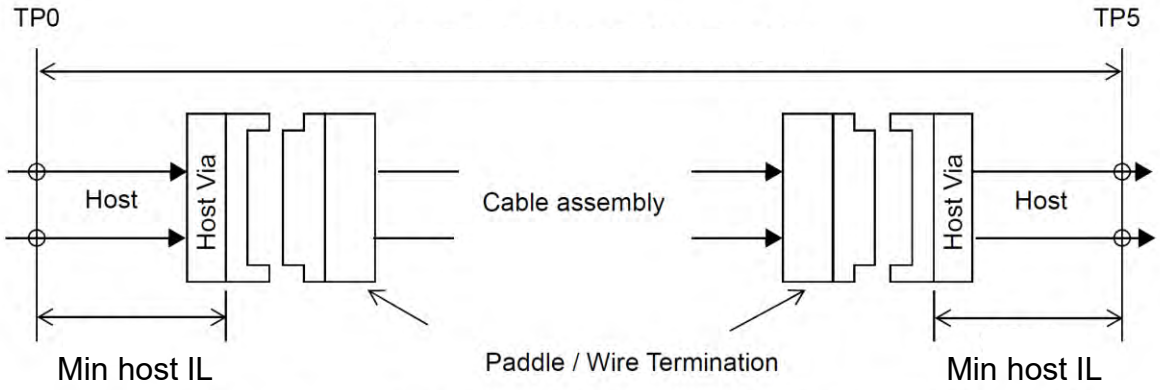
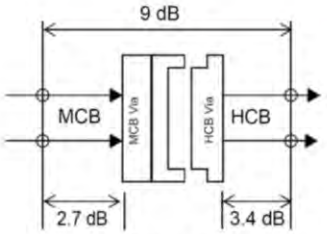


Figure xxxA–x—Minimum Channel insertion loss at 53.125 GHz

Supplemental

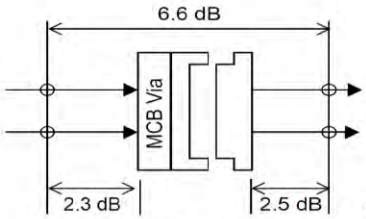
TP1-TP4,TP2,TP3- tested with compliant fixtures

Mated test fixture insertion loss - HFSS model



Mated cable assembly and test point test fixture

insertion loss @ 53.125 GHz



Mated cable assembly and test point test fixture

insertion loss @ 26.56 GHz

Figure source: IEEE Draft P802.3ck/D3.1

Component	Insertion Loss (dB)
Module Compliance Board (MCB) PCB - 2" of ~1.35 dB/in	2.7
Host Compliance Board (HCB) - 1inch*1.35dB/in + 6inch coax * .28dB/inch + 0.5dB via and co-ax transitions.	3.4
Mated Test Fixture (MTF)	9
MTF connector + 2 via's	2.9

Mated test fixture and host insertion loss allocations @ 53.125 GHz

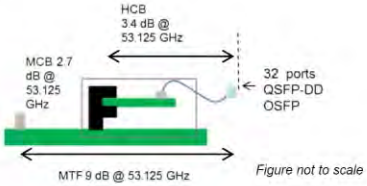


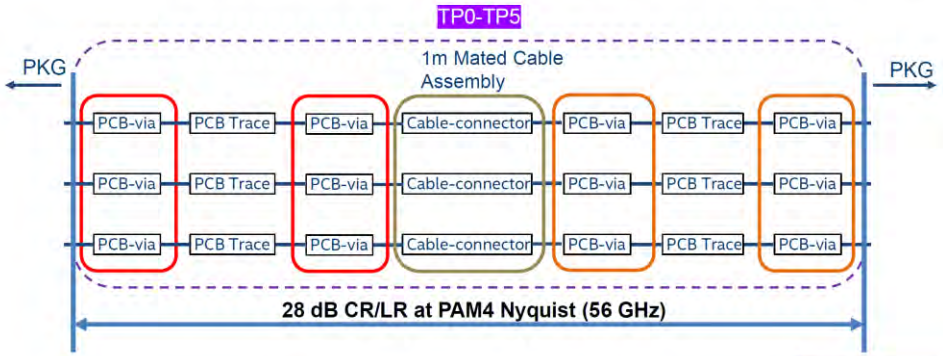
Table 162–8—Test points

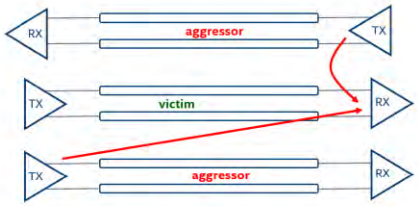
Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 162–2. The cable assembly test fixture of Annex 162B, or its equivalent, is required for measuring the cable assembly specifications in 162.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 162.9.4 and 162.9.5. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 162.9.4.5.
TP2	Unless specified otherwise, all transmitter measurements defined in 162.9.4 are made at TP2 utilizing the test fixture specified in Annex 162B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 162.9.5 are made at TP3 utilizing the test fixture specified in Annex 162B.

Source: https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf

A 224 Gbps-PAM4 1 Meter DAC Long Reach Channel and Its Characteristics: Design A

224 Gbps-PAM4 CR Channel Structure



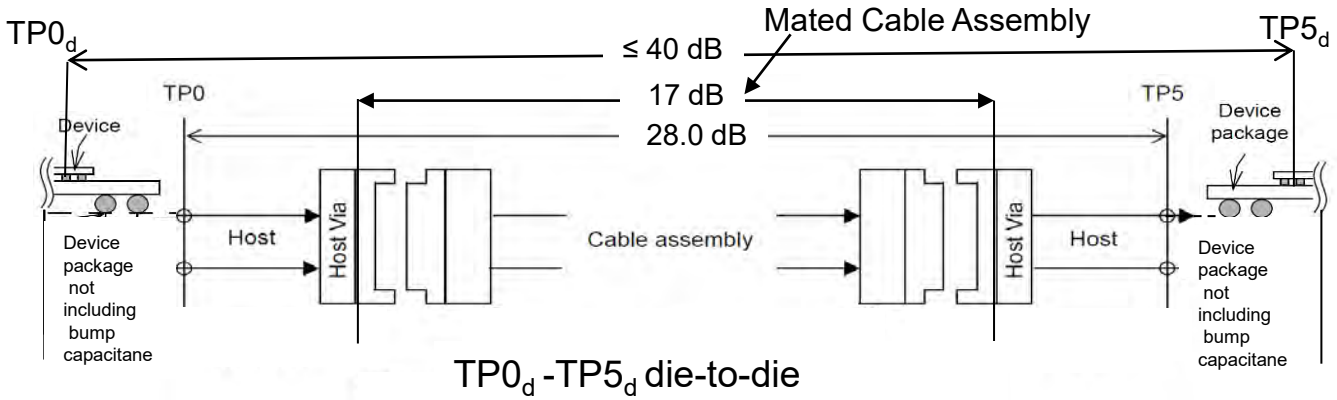


TP0-TP5 Characteristics (DC-56GHz)

- **IL: 28.0dB @ 56GHz**
- RL <~ 12dB (<56GHz)
- FEXT < 44dB (<56GHz)
- NEXT < 51dB (<56GHz)

Component	TP0-TP5 Insertion Loss (dB) @ 56GHz
	Design A
PCB via	1.7 dB
PCB Trace	7.5 inch (TX+RX, 1.3 dB/inch)
Mated Cable Assembly	17.0 dB
Total	28.0 dB

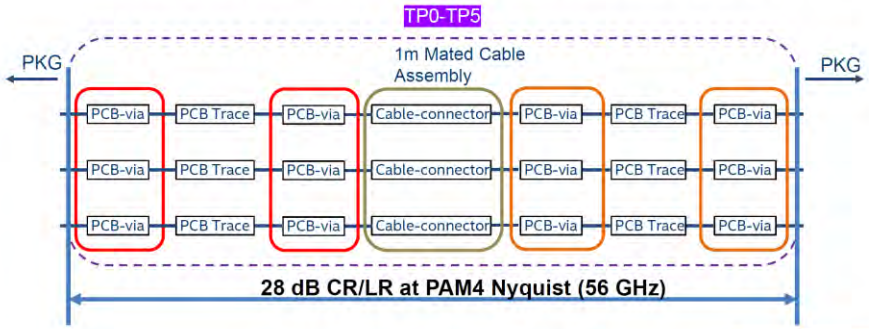
https://www.ieee802.org/3/dj/public/23_05/li_3dj_08a_2305.pdf



$TP0_d$ -$TP5_d$ die-to-die

A 224 Gbps-PAM4 1 Meter DAC Long Reach Channel and Its Characteristics: Design B

224 Gbps-PAM4 CR Channel Structure



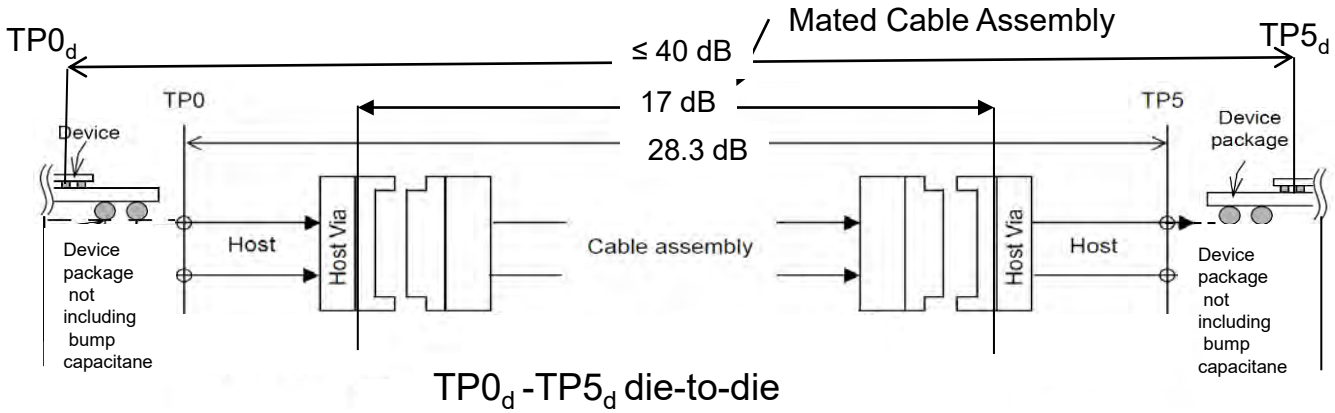
https://www.ieee802.org/3/dj/public/23_05/li_3dj_10a_2305.pdf

TP0-TP5 Characteristics (DC-56GHz)

- **IL: 28.3dB @ 56GHz**
- RL <~ 11dB (<56GHz)
- FEXT < 45dB (<56GHz)
- NEXT < 45dB (<56GHz)

Component	TP0-TP5 Insertion Loss (dB) @ 56GHz
	Design B
PCB via	1.7 dB
PCB Trace	7.5 inch (TX+RX, 1.3 dB/inch)
Mated Cable Assembly	17.0 dB
Total	28.3 dB

P802.3dj May 2023 IEEE 4



$TP0_d$ -$TP5_d$ die-to-die