The Merits of Common AUI Application

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IEEE 802.3dj Task Force
Plenary Meeting
Berlin

July 10, 2023

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Overview

- **Background medium loss and high loss AUI**
  - Based on promise that medium loss have will have much simpler and lower power
  - Does the data support to define medium loss AUI?
- **Need to engineer PCB-PKG to meet the max CR/KR loss ≤ 40 dB**
  - Moderate AUI host-PKG engineering better than assuming worst-worst PCB-PKG combinations
- **The benefit of common AUI with max bump-bump loss ≤32 dB**
- **Summary.**

Background on Med and High Loss AUIs

- **During October session there was strong support to define Med and High Loss AUI considering splintering C2M application with assumption that there will significant power saving**
  - https://www.ieee802.org/3/df/public/22_10/motions_3df_221004.pdf

Straw Poll #1

For the front panel pluggable use case, I am interested in 200 Gbps/lane AUI C2M specifications for:

A. medium loss only (e.g. up to ~22 dB IL die-die per lusted_3df_01_220927)
B. higher loss only (e.g. up to ~36 dB IL die-die per lusted_3df_01_220927)
C. both medium and higher loss
D. need more information

pick one

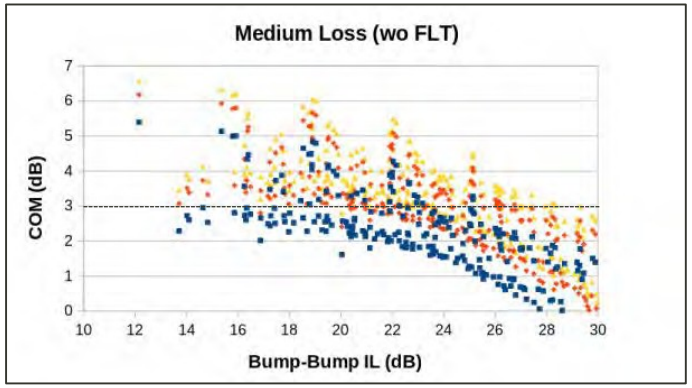
Results: A: 17, B: 11, C: 49, D: 12

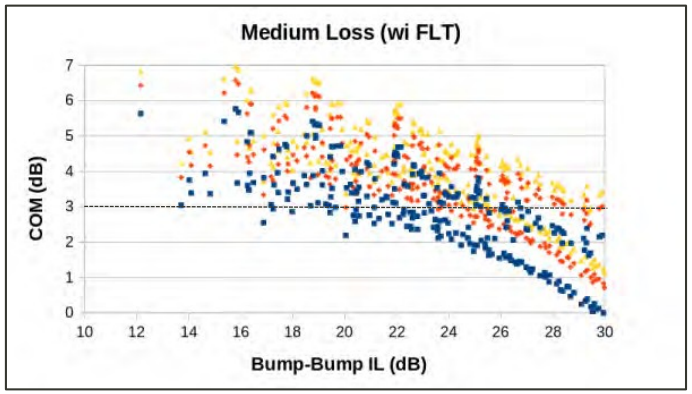
Background on Med and High Loss AUIs, cont.

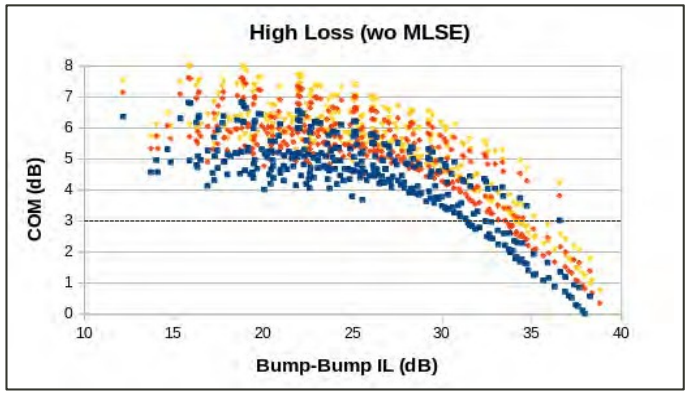
- **During Nov. 2022 several contribution investigated various implementation of Med/High loss AUIs**
  - Lusted explored higher loss AUI
    - https://www.ieee802.org/3/df/public/22_11/lusted_3df_02_2211.pdf
  - Lusted explored Med loss AUI
    - https://www.ieee802.org/3/df/public/22_11/lusted_3df_03a_2211.pdf
  - Ghiasi and et. al. bottom-up analysis of medium and high Loss AUIs
    - https://www.ieee802.org/3/dj/public/23_01/23_0116/ghiasi_3dj_02a_230116.pdf
  - li_3dj_01a_2303 COM analysis show that ~50% of medium loss AUIs fails with assumed less capable 8 tap DFE equalizer
    - More capable equalizer 24 tap DFE +6x2 banks of FLT with 80 UI operates with margin on channel up to ~35 dB.

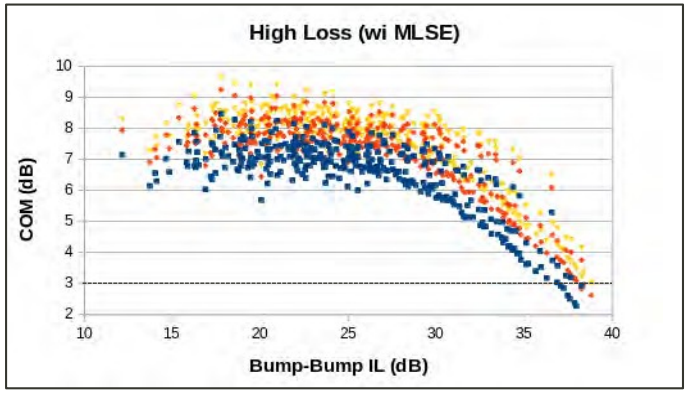
AUI Medium/High Loss COM Analysis

- **li_3dj_01a_2303 COM analysis indicates**
  - Med loss equalizer 8 DFE is inadequate (optional FLT is 3 banks of 3 with 80 UI span is needed even for 22 dB AUIs)
  - High loss equalizer 24 DFE + 6 banks of 3 DFEs with span of 80 UIs
  - Evan at DER of 5E-5 to support channel up to 22 dB require floating taps due to channel reflections
  - High loss AUIs without MLSE pass all channels up to ~34 dB, but MLSE may be need for margin!









How to Partition and Split AUI Application

- **li_3dj_01a_2303 data indicate assumed type I equalizer is under-powered for medium loss AUI**
- **lusted_3dj_01_2307 suggest categorizing AUI equalizer from mild to spicy**
  - For DSP implementation taps are implemented as FFE what drives the power is the span of the equalizer and is not clear that type I and II will have that different a power dissipation
  - Type III is with the addition of the MLSE with added power penalty that should be avoided even for high loss AUI due to module PD!

- Class I/II/III

Parameter	802.3ck C2M	802.3ck CR	802.3ck KR	802.3ck C2M-like + FLT (Exploratory of 802.3dj Medium Loss AUI C2M)	802.3ck CR-like (Exploratory of 802.3dj High Loss AUI C2M)	802.3ck CR-like + MLSE (Exploratory of 802.3dj High Loss AUI C2M)
DER_0	1E-5	1E-4	1E-4	1.33E-5 / 2.67E-5	1.33E-5 / 2.67E-5	1.33E-5 / 2.67E-5
SNR_TX	32.5	32.5	33	32.5	33	33
R_LM	0.95	0.95	0.95	0.95	0.95	0.95
TxFIR Length	4 (2 pre)	5 (3 pre)	5 (3 pre)	5 (3 pre)	6 (4 pre)	6 (4 pre)
eta_0	4.10E-08	9E-09	8.2E-09	2.05E-08	1.25E-08	1.25E-08
N_b	4	12	12	8	1	1
	-	-	-	0	4	4
	-	-	-	0	24	24
N_bg	0	3	3	3	6	6
N_bf	-	3	3	3	3	3
N_f	-	40	40	60	60	60
MLSE	0	0	0	0	0	1
Ref TX/RX Class				**I**	**II**	**III**

Note: these classes are starting points, not specific recommendations.

(Mild) (Spicy!)

AUI Bottom-Up Analysis

- **Not allowed host PCB-PKG combinations are based on ghiasi_3dj_03_230116.xlsx bottom-Up Analysis by also including worst/nominal losses**
  - Updated spreadsheet increases connector loss and plug board/HCB to better align with Daminico_3dj_01_2307
  - A modest amount of PCB-PKG engineering allows meeting bump-bump loss ≤32 dB
  - With CDR PKG loss accounting for ~ 2.5 dB
  - Proposed common AUI application for all front pluggable TP0b-TP1a loss ≤29.5 dB
  - The above recommendation exclude XSR+/NPO where the equalizer potentially can be lower power and simpler.

Loss Parameters @ 53 GHz A. Ghiasi - Rev 1.2 7/5/2023	Worst Loss	Nom. Loss	Length or #	AUI Type Conventional PCB Worst Case	AUI Type Conventional PCB Nom. Case	AUI Type II Cabled Host	AUI NIC Conventional PCB	AUI Type III Cabled Substrate	XSR+ NPO
Host PCB Loss (dB/in)	1.5	1.3	10	15	13	NA	NA	NA	NA
NIC PCB Loss (dB/in)	1.65		5	NA	NA	NA	8.25	NA	NA
Cabled Host PCB Loss (dB/in)	1.5	1.3	2	NA	NA	3	NA	NA	NA
Cable Loss (dB/in)	0.3		12	NA	NA	3.6	NA	3.6	NA
Plug Board/PIC/HCB Loss (dB/in)	1.5	1.5	2	3	3	3	3	3	3
AUI Connector Loss (dB)	2.1	2.1	1	2.1	2.1	2.1	2.1	2.1	NA
Host Via Loss (dB)	0.8	0.8	2	1.6	1.6	1.6	NA	NA	NA
NIC Via Loss (dB)	0.6		2	NA	NA	NA	1.2	NA	NA
Host Package Loss (dB/mm)	0.21	0.18	45						
NIC Package Loss (dB/mm)	0.225		16						
CDR Package Loss (dB/mm)	0.225	0.21	10						
Host/NIC PKG Mode Con. Loss (dB)	1	1	NA	10.45	9.1	10.45	4.6	10.45	10.45
CDR PKG Mode Con. Loss (dB)	0.4	0.4	NA	2.65	2.5	2.65	2.65	2.65	NA
TGA Connector Loss (dB)	0.3		NA	NA	NA	0.3	NA	NA	NA
Socket Loss (dB)	0.2		NA	NA	NA	NA	NA	0.2	0.2
NPO Substrate Loss (dB/mm)	0.095		50						
NPO Substrate Loss (dB)	4.75		NA	NA	NA	NA	NA	4.75	4.75
TP0-TP1a Loss (dB)	NA		NA	21.7	19.7	13.6	14.55	13.65	4.95
Bump-TP1a (dB)	NA		NA	32.15	28.8	24.05	19.15	24.1	15.4
Bump-Bump Loss (dB)	NA		NA	34.8	31.3	26.7	21.8	26.75	18.4

Common AUI Application

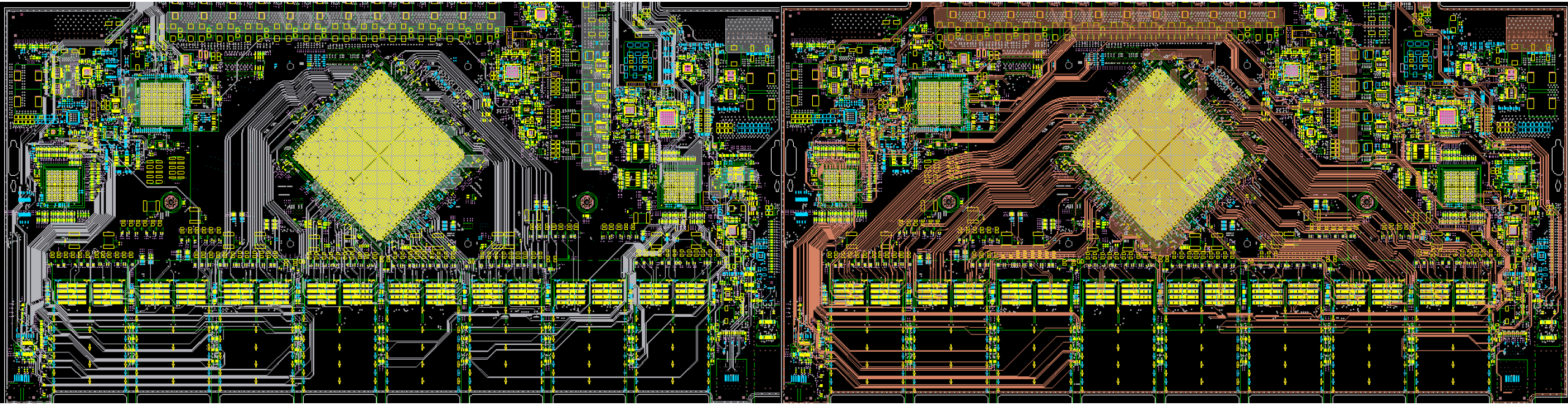
XSR+

Existing 12.8T OCP Designs

- **OCP reference design based on 32xQSFP-DD modules traces vary from ~1.9-9.5”**
  - Loss already managed by connecting middle port to ASIC far side lanes and furthest ports to nearest ASIC lanes
  - To managed 200G max channel loss to ≤32 dB some degree of package-PCB trade off maybe required for some designs
  - http://files.opencompute.org/oc/public.php?service=files&t=961a5462ded325f40d065a4f3b5eb637 .

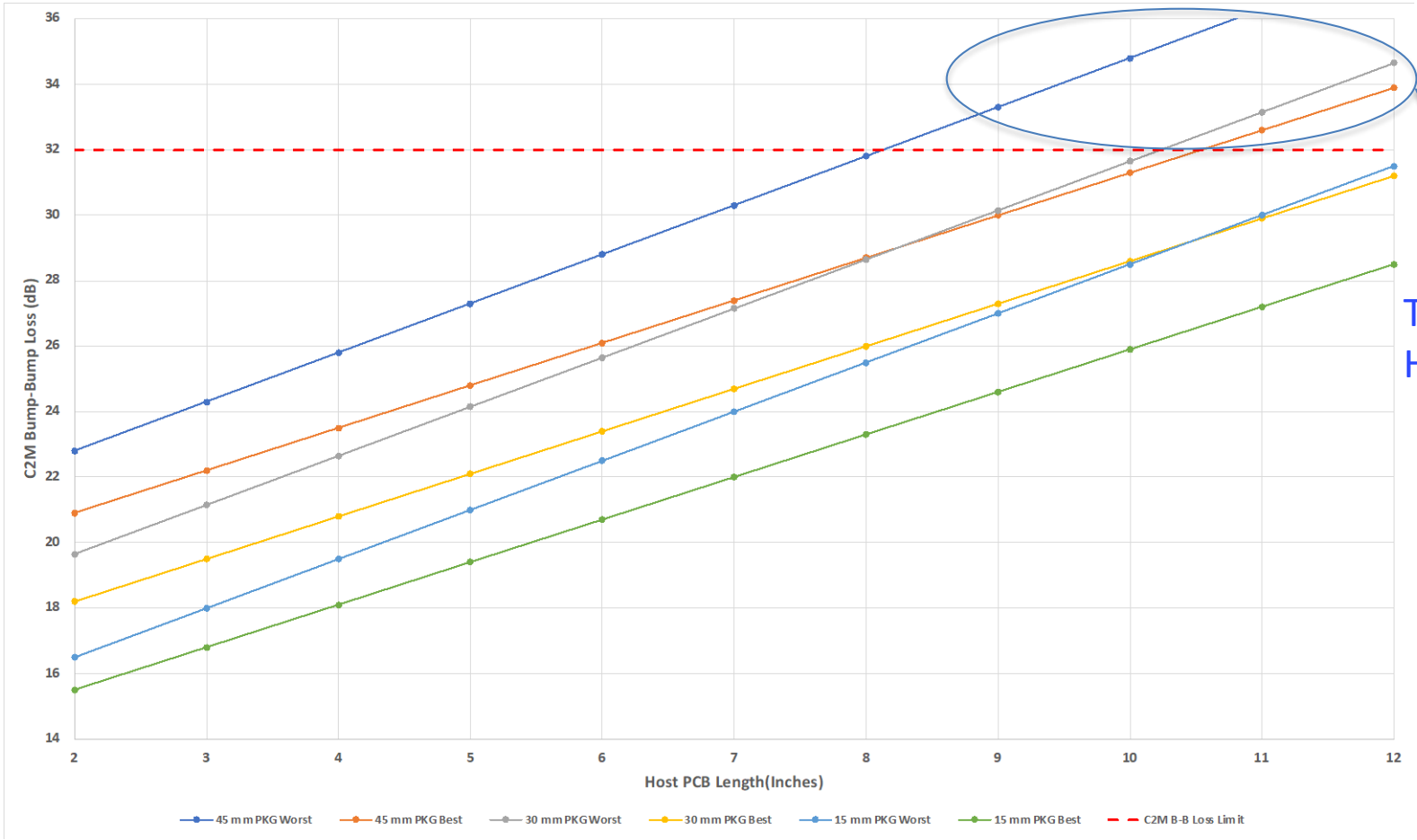
Layer 7

Layer 9



Modest Engineering Package-PCB Losses

- **CR/KR applications require significant package-PCB engineering to meet ≤40 dB**
  - Requiring a modest engineering of AUI channels for max bump-bump loss of ≤32 dB is not unreasonable!



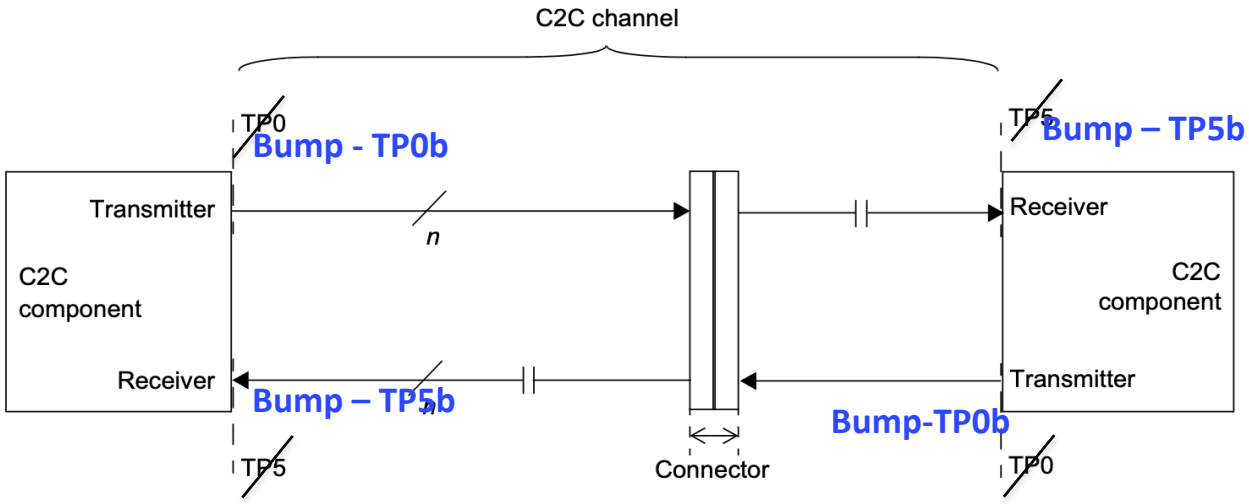
These Combinations of Host PCB-PKG not allowed

Why Task Force Should Consider Defining a Common AUI?

- **The premise of defining Medium and High loss C2M AUIs where:**
  - The high loss AUI ~34-36 dB require 60+ taps equalizer with MLSE
    - KR/CR links require significant PCB-PKG engineering to meet ≤40 dB loss
    - A modest engineering where we are not assuming worst-worst pair combination allow limiting C2M max loss ≤32
    - With 33-36 dB channel removed the high loss equalizer become more like medium loss equalizer
  - It was assumed medium loss AUI will have just 2-3x number of taps compared to 100G C2M AUI
    - On representative channel 8-12 taps equalizer is nonstarter
    - Due to higher reflection the medium loss channel equalizer may require 60+ tap equalizer and potentially MLSE
- **By limiting high loss channel to 32 dB and given reflective nature of medium loss channels the solution equalizer ends up to be similar**
  - One can't justify defining two incompatible C2M AUIs for just a modest power benefit at best
  - It has been 9+ month since we started investigating two C2M AUI applications with hope of defining Med-power/loss and High-power/loss AUIs.

AUI C2C Application Reference Model

- **AUI C2C total loss for DJ will be changed from TP0-TP5 to bump-bump**
  - Recommend to use TP0b for Tx bump
  - Recommend to use TP5b for Rx bump
  - C2C max bump-bump loss ≤ 32 dB at 53.125 GHz

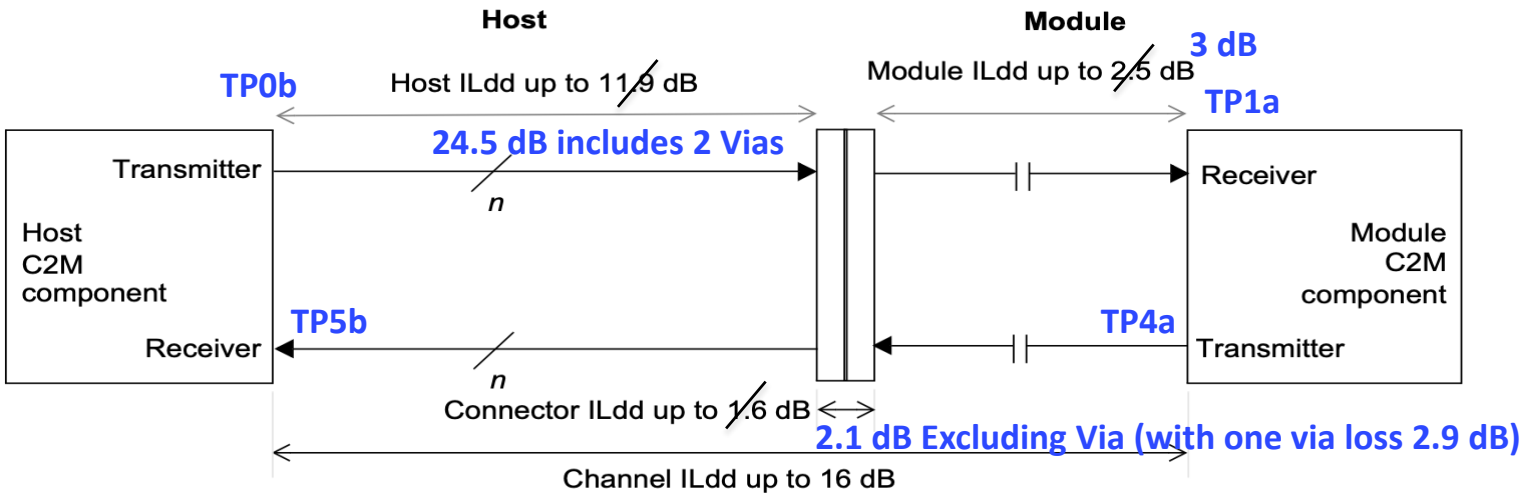


NOTE—The number of lanes *n* is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, and 4 for 400GAUI-4.

Figure 120F–2—Typical 100GAUI-1, 200GAUI-2, and 400GAUI-4 C2C application

AUI C2M Application Reference Model

- **AUI C2M total loss for DJ proposed to be from TP0b(bump) -TP1a**
  - Recommend to use TP0b for Tx bump
  - Recommend to use TP5b for Rx bump
  - C2M max TP0b -TP1a (TP4a-TP5b) loss ≤ 29.5 dB at 53.125 GHz
  - Max host + package losses including two vias ≤ 24.5 dB (rounded up).



NOTE—The number of lanes *n* is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, and 4 for 400GAUI-4.

Figure 120G–2—100GAUI-1, 200GAUI-2, and 400GAUI-4 C2M insertion loss budget at 26.56 GHz

Summary

- **Proposed AUI C2C and C2M both have max bump-bump loss of 32 dB and will be based on common SerDes Technology**
  - Normative loss specifications for C2C will be from TP0b(bump)-TP5b
  - Normative loss specifications for C2M will be from TP0b(bump)-TP1a (TP4a-TP5b)
- **The Task Force has done excellent job investigating the merits of medium and high loss C2M AUIs**
  - However, the finding to date have not corroborated reducing complexity and power for medium loss AUI due to reflective nature of these channels
  - Without significant power saving and benefits the task force should not define two incompatible C2M AUIs
- **CR/KR links will require significant host-PKG engineering to meet bump-bump loss of ≤40 dB**
  - It is not unreasonable to ask a moderate amount of host-PKG engineering also for the AUIs instead of assuming worst-worst PCB-PKG combinations
  - Limiting AUI C2M max bump-bump loss to 32 dB (informative) or 29.5 dB from TP0b-TP1a addresses originally envisioned high loss AUI application due to modest PKG-PCB engineering
  - Proposed common 32 dB AUI SerDes expect to be have similar complexity/power to what is need to support the task force medium loss AUI (~20-25 dB) channels.

Recommend Task Force Consider Adopting Following Items Toward AUI Baseline

- **FEC definition per ran_3dj_02_2305.pdf with DER0=2.67E-4 per PHY with division between C2C and C2M TBD per May-2023 motion**
- **Recommend the task force to adopt a single AUI C2C with a loss ≤ 32 dB with equalizer TBD**
- **Task force adopts single AUI C2M with bump-bump loss ≤ 32 dB (informative given that module and host are separable interfaces) – we should at least decide on C2M bump-bump loss in Berlin**
  - Option- I Follow 802.3ck architecture but with further optimization to follow
    - Task force adopts single AUI C2M with a TP0b(bump)-TP1a (TP4a-TP5b) loss ≤ 29.5 dB (assume 2.5 dB CDR package loss) with equalizer TBD
    - Recommend task force to adopt host PCB/PKG informative loss ≤24.5 dB
  - Option – II Defer host and module loss breakdown in Berlin
    - One further optimization is to allow trade-off HCB-CDR package losses to allow increasing host PCB/PKG loss from 24.5 dB by 1-1.5 dB.