A consensus baseline proposal for Inner FEC processing rate for Type 2 PHYs

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Goal of this Presentation

This presentation describes a consensus proposal to adopt a common rate for FEC_I lane for 200GbE, 400GbE, 800GbE, 1.6TbE MAC configuration.
Recap of Status of FEC_I Architecture & Work in Progress

200G, 400G, 800G, 1.6T PCS is already adopted as per CL-119, CL-172 PCS

200G Symbol Muxing PMA scheme is already adopted: ran_3dj_01a_2303.pdf

* Most of the Inner Code FEC sublayer is adopted except few blocks

Work in Progress:
- Rate of Convolutional Interleaver for 200G/400G/800GbE
- Inner FEC sublayer for 1.6TbE

P802.3dj Task Force

Type 2 scheme
Recap of Rate of FEC_I Convolutional Interleaver for Both Proposals

Lenin’s Proposal:
- Rate specific Alignment Logic blocks
- 20b or 40b symbol distribution based **1:8 demux before** Convolutional Interleaver
- Rate specific convolutional Interleaver

Xiang’s Proposal:
- Rate independent Logic blocks
- One common Convolutional Interleaver
- 120b codeword distribution based **1:8 demux after** Convolutional Interleaver

** Topic of debate between both the proposal was**
- **Position of 1:8 Demux before** or **After** Convolutional Interleaver
Progress of FEC_I Architecture since then:

• Symbol-pair muxing has been fully adopted for 200G/lane signaling.
  • See ran_3dj_01a_2303, and motions_3dfdj_2303.

• 4xRS CWs interleaving in the PMA has been proposed to ensure same performance for 200GE and 400GE when using 200G/lane signaling. Essentially – for every MAC up to 1.6TbE, FEC codeword will be aligned with 40b symbol boundaries.
  • See he_3dj_02_2305

• If 4XRS CW interleaving scheme gets adopted, then it simplifies the implementation of rate dependent logic blocks to one common universal Logic blocks.

• This presentation provides the details of a common rate for convolutional interleaver and proposes a universal 200G/Lane rate based CI for FEC_I sublayer with final delay numbers
Proposed Architecture Overview:

- The current proposals focused on inner FEC implementations inside module DSP.
- Symbol-pair muxing PMA sublayer is assumed to be above the FEC_I sublayer for all proposals.
- One **common interleaver** and **de-interleaver** is proposed to complete the FEC_I sublayer architecture.

Highlighted PMA is the symbol pair mux PMA

Source: patra_3dj_01b_2303.pdf
Proposed Update to Symbol-pair Muxing PMA:

- FEC_I sublayer is the sublayer below symbol-pair muxing PMA.

<table>
<thead>
<tr>
<th>PMA family</th>
<th>Specific PMAs</th>
<th>Sublayer/interface above</th>
<th>Sublayer/Interface below</th>
</tr>
</thead>
<tbody>
<tr>
<td>R8F</td>
<td>PMA(8:1)</td>
<td>200GBASE-R PCS / DTE XS</td>
<td>200GAUI-1 / FEC_I / PMD</td>
</tr>
<tr>
<td></td>
<td>PMA(16:2)</td>
<td>400GBASE-R PCS / DTE XS</td>
<td>400GAUI-2 / FEC_I / PMD</td>
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<tr>
<td></td>
<td>PMA(32:4)</td>
<td>800GBASE-R PCS / DTE XS</td>
<td>800GAUI-4 / FEC_I / PMD</td>
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<tr>
<td>R2F</td>
<td>PMA(2:1)</td>
<td>200GAUI-2</td>
<td>200GAUI-1 / FEC_I / PMD</td>
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<tr>
<td></td>
<td>PMA(4:2)</td>
<td>400GAUI-4</td>
<td>400GAUI-2 / FEC_I / PMD</td>
</tr>
<tr>
<td></td>
<td>PMA(8:4)</td>
<td>800GAUI-8</td>
<td>800GAUI-4 / FEC_I / PMD</td>
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<td>R1</td>
<td>PMA(1:1)</td>
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<td>200GAUI-1 / FEC_I / PMD</td>
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<td>PMA(2:2)</td>
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<td>PMA(4:4)</td>
<td>800GAUI-4</td>
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<tr>
<td></td>
<td>PMA(8:8)</td>
<td>1.6TAUI-8</td>
<td>1.6TAUI-8 / FEC_I / PMD</td>
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<td>1.6TBASE-R PCS / DTE XS / 1.6TAUI-16</td>
<td>1.6TAUI-8 / FEC_I / PMD</td>
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</tbody>
</table>

Source: ran_3dj_01a_2303, with modifications in Blue
Example of Transmit and Receive Processing for FEC_I Sublayer with 200G/Lane & 100G/Lane AUI

**TX Processing Path**

From 2x 100G AUI:
- R2F: Symbol-pair mux PMA
- Convolutional interleaver
- 120-b distribution
- CS & encode
- 8:1 baud interleaver
- To 1x 200G PMA_I and PMD

From 1x 200G AUI:
- R1: Symbol-pair mux PMA
- Convolutional interleaver
- 120-b distribution
- CS & encode
- 8:1 baud interleaver
- To 1x 200G PMA_I and PMD

1, 2, 4 or 8 instances (200GE, 400GE, 800GE or 1.6TE)

**RX Processing Path**

To 2x 100G AUI:
- R2B or 8:16
- Symbol-pair mux PMA
- Convolutional de-interleaver
- 120-b distribution
- Decode & inv CS
- 8:1 baud de-interleaver
- From 1x 200G PMA_I and PMD

To 1x 200G AUI:
- R1: Symbol-pair mux PMA
- Convolutional de-interleaver
- 120-b distribution
- Decode & inv CS
- 8:1 baud de-interleaver
- From 1x 200G PMA_I and PMD

1, 2, 4 or 8 instances (200GE, 400GE, 800GE or 1.6TE)
Transmit path overview

BASE-R PMA (Symbol Muxing PMA – aligned to Symbol pair or Quartet boundaries)

Convolutional interleaver

1:8 Demux for 120-bit Codeword Distribution

Circular shift

Hamming encoder

Hamming interleaver, pad insertion

PMA:IS_UNITDATA_0.request  PMA:IS_UNITDATA_(q-1).request

PMA

PMD

Receive path overview

BASE-R PMA (Symbol Muxing PMA – aligned to Symbol pair or Quartet boundaries)

Convolutional de-interleaver

8:1 MUX for 120b codeword distribution

Inverse Circular Shift

Hamming decoder

Frame sync, Hamming de-interleaver & padding removal

PMA:IS_UNITDATA_0.indication  PMA:IS_UNITDATA_(q-1).indication

PMA

PMD
An universal 200G/lane convolutional interleaver is proposed for different MACs to unify the processing.

If 4x RS CWs interleaving in the PMA proposal is adopted, the convolutional interleaver logics will be further shared among all the MACs.

For latency sensitive applications, convolutional interleaver can be bypassed.

<table>
<thead>
<tr>
<th>Rate</th>
<th>d (RS symbol)</th>
<th>P</th>
<th>Q</th>
<th>Depth</th>
<th>Latency ns</th>
<th>FEC_I Lane Rate</th>
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<tbody>
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<td>1.6TE</td>
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<td>3</td>
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<td>24</td>
<td>12x RS</td>
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<td>800GE</td>
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<td>3</td>
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<td>12x RS</td>
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<td>96</td>
<td>12x RS</td>
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<td>192</td>
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<tr>
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<td>6</td>
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<tr>
<td>200GE</td>
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<td>6</td>
<td></td>
<td>96</td>
<td>12x RS</td>
<td>271.1</td>
</tr>
</tbody>
</table>

*If 4x RS interleaving for 200GE/400GE is adopted.
A complete View of **FEC_I Sublayer** Architecture with Common Convolutional Interleaver
Summary

• A common 200G/lane based convolutional interleaver for FEC_I sublayer is presented in this proposal for 200G/400G/800G/1.6T MAC configurations.
  • This is the key TBD item for a complete FEC_I sublayer baseline.
• The presented proposal also works well with already adopted FEC_I sublayer and 200G/lane symbol muxing based PMA sublayers.
Thank you!