A consensus baseline proposal for Inner FEC processing rate for Type 2 PHYs

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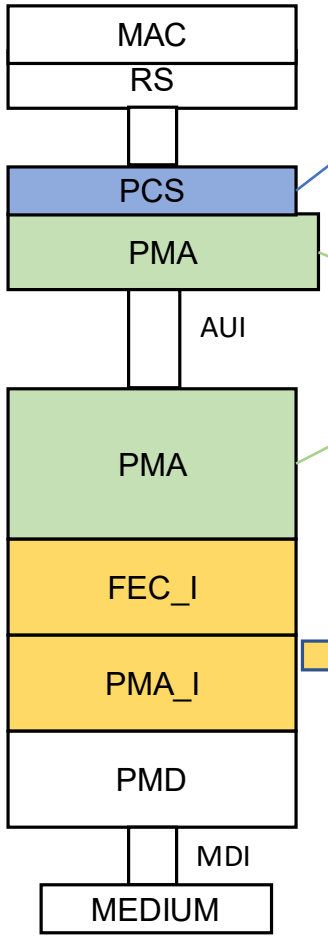
Goal of this Presentation

This presentation describes a consensus proposal to adopt a common rate for FEC_I lane for 200GbE, 400GbE, 800GbE, 1.6TbE MAC configuration.

Recap of Status of FEC_I Architecture & Work in Progress



Type 2 scheme

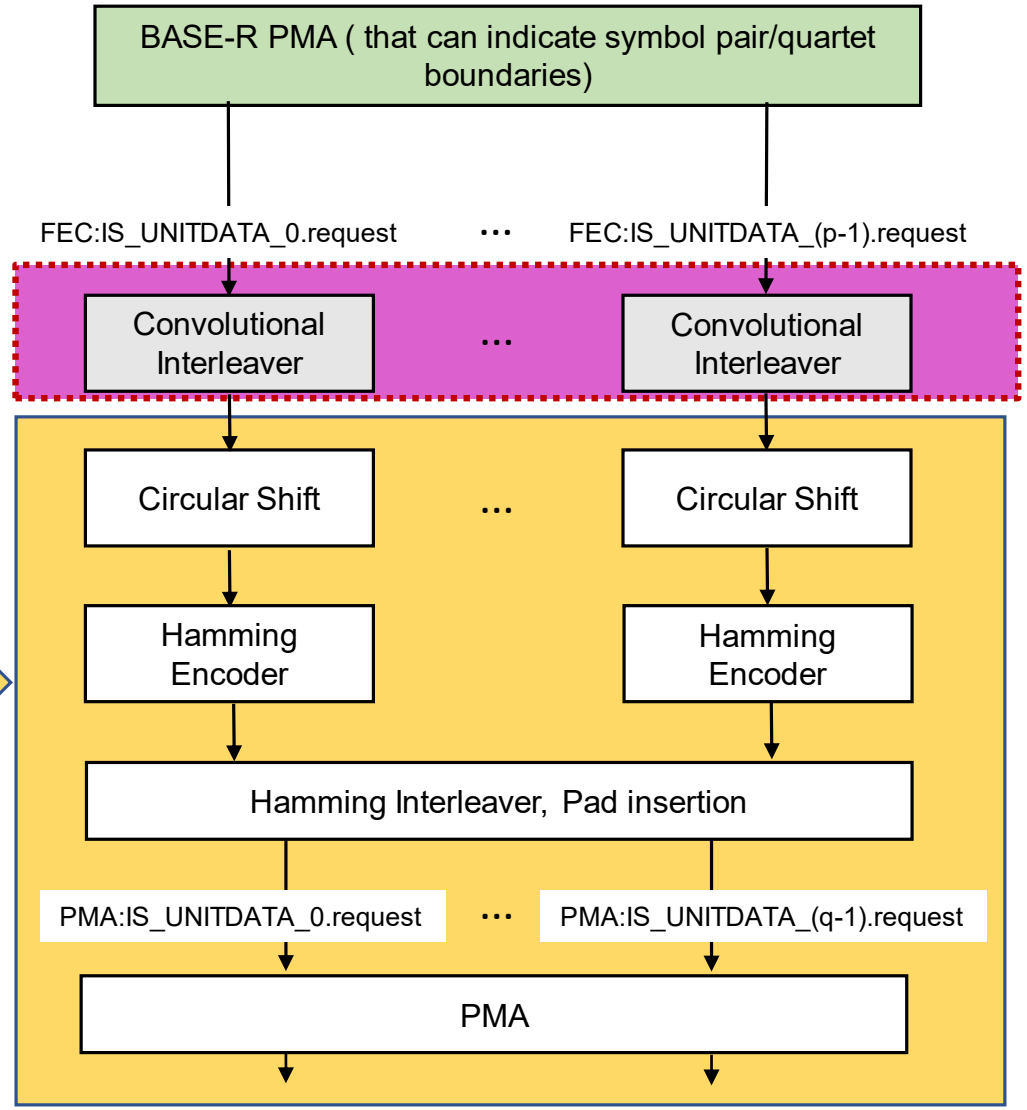
200G, 400G, 800G, 1.6T PCS is already adopted as per CL-119, CL-172 PCS

200G Symbol Muxing PMA scheme is already adopted: *ran_3dj_01a_2303.pdf*

* Most of the Inner Code FEC sublayer is adopted except few blocks

Work in Progress:

- Rate of Convolutional Interleaver for 200G/400G/800GbE
- Inner FEC sublayer for 1.6TbE



Recap of Rate of FEC_I Convolutional Interleaver for Both Proposals

Lenin's Proposal:

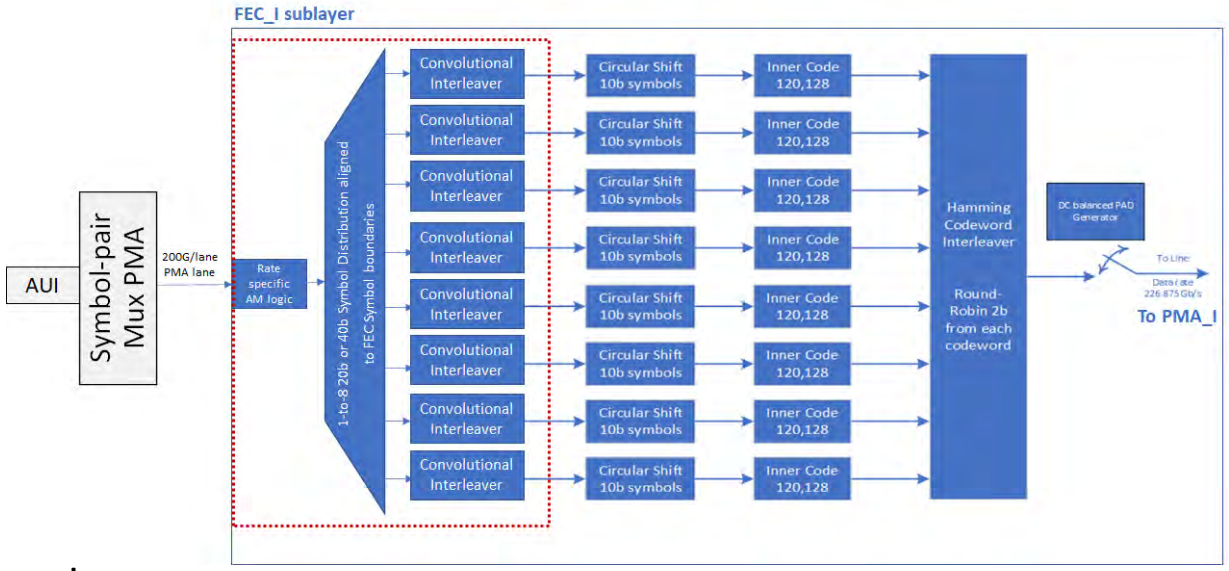
- Rate specific Alignment Logic blocks
- 20b or 40b symbol distribution based **1:8 demux** **before** Convolutional Interleaver
- Rate specific convolutional Interleaver

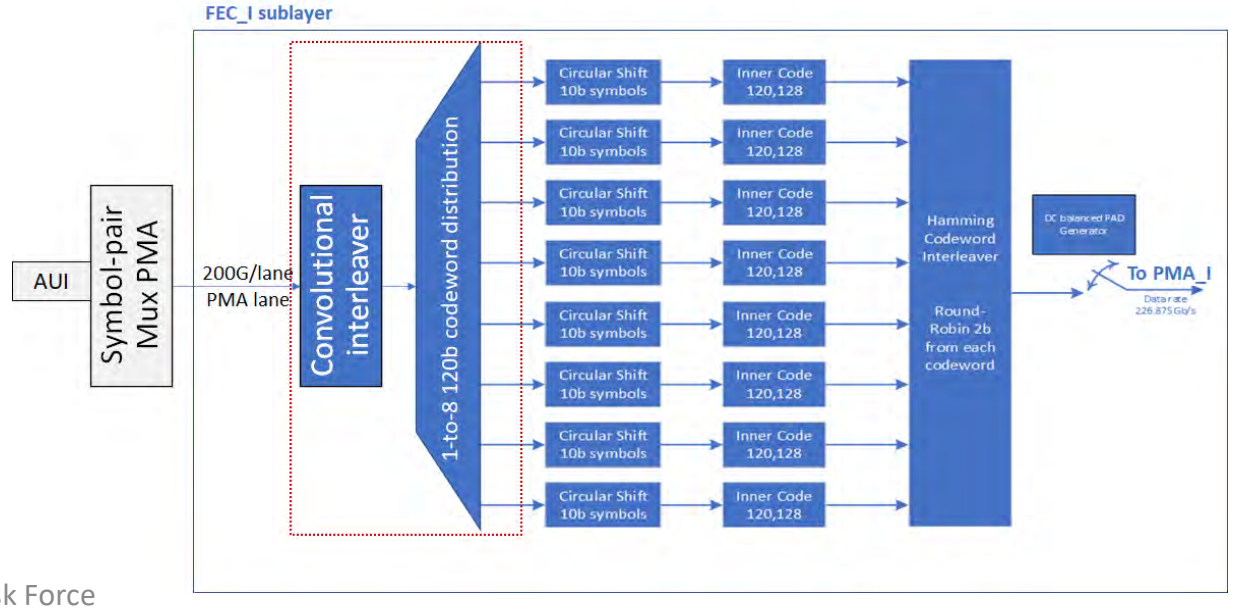
** Topic of debate between both the proposal was

- **Position** of **1:8 Demux** before or After Convolutional Interleaver

Xiang's Proposal:

- Rate independent Logic blocks
- One common Convolutional Interleaver
- 120b codeword distribution based **1:8 demux** **after** Convolutional Interleaver





Progress of FEC_I Architecture since then:

- Symbol-pair muxing has been fully adopted for 200G/lane signaling.
  - See ran_3dj_01a_2303, and motions_3dfdj_2303.

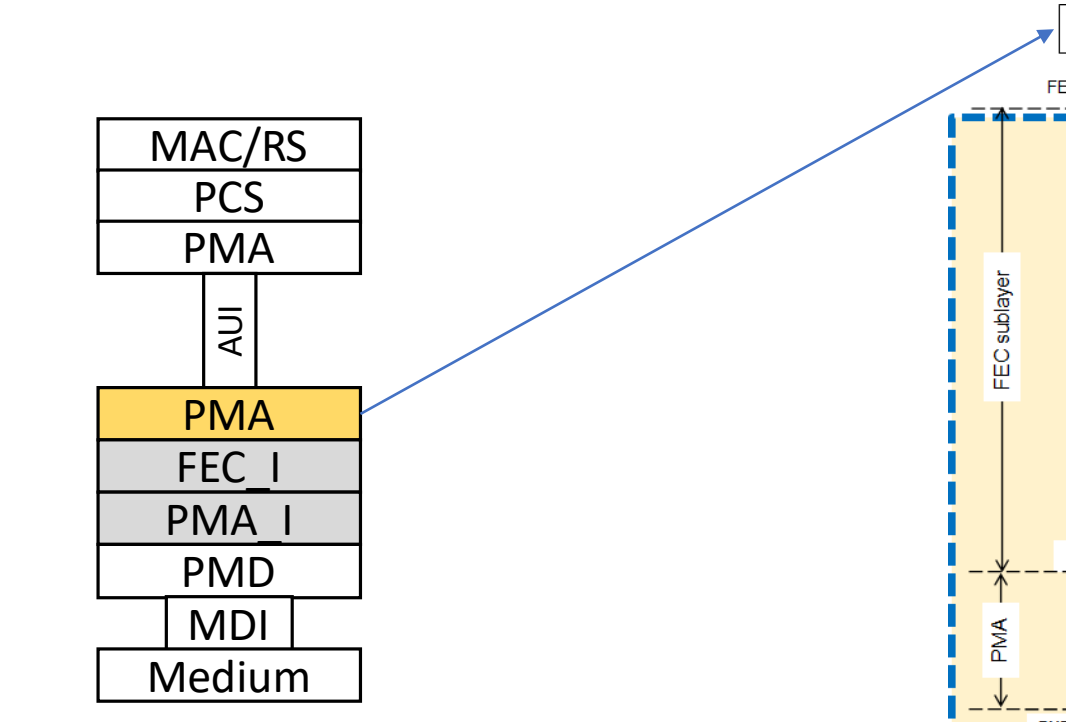
- 4xRS CWs interleaving in the PMA has been proposed to ensure same performance for 200GE and 400GE when using 200G/lane signaling. Essentially – for every MAC up to 1.6TbE, FEC codeword will be aligned **with 40b symbol** boundaries.
  - See he_3dj_02_2305

- If 4XRS CW interleaving scheme gets adopted, then it simplifies the implementation of rate dependent logic blocks to one common universal Logic blocks.

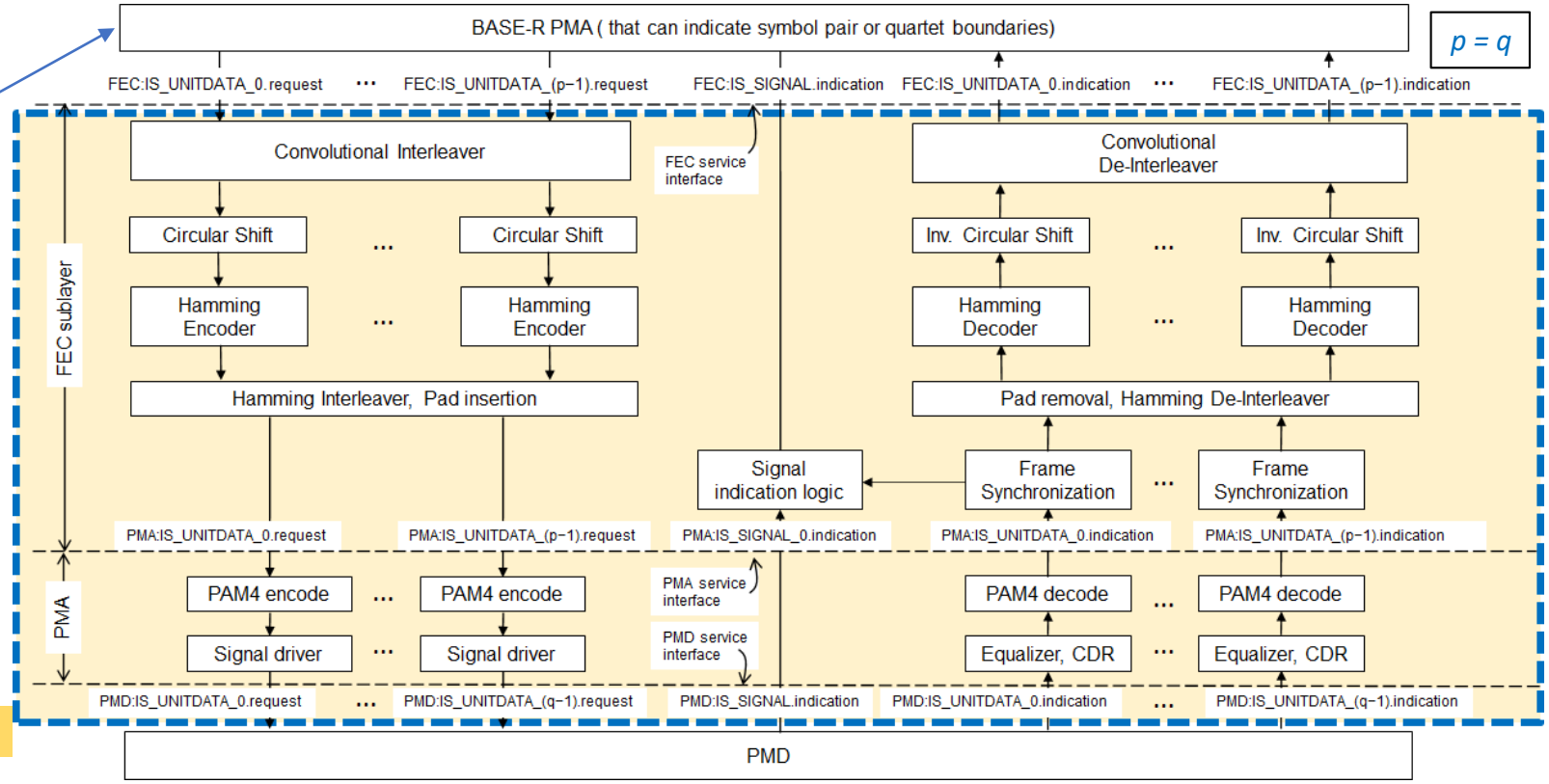
- This presentation provides the details of a common rate for convolutional interleaver and proposes a **universal 200G/Lane rate based CI** for FEC_I sublayer with final delay numbers

Proposed Architecture Overview:

- The current proposals focused on inner FEC implementations inside module DSP.
- Symbol-pair muxing PMA sublayer is assumed to be above the FEC_I sublayer for all proposals.
- One **common interleaver** and **de-interleaver** is proposed to complete the FEC_I sublayer architecture



Highlighted PMA is the symbol pair mux PMA



Source: patra_3dj_01b_2303.pdf

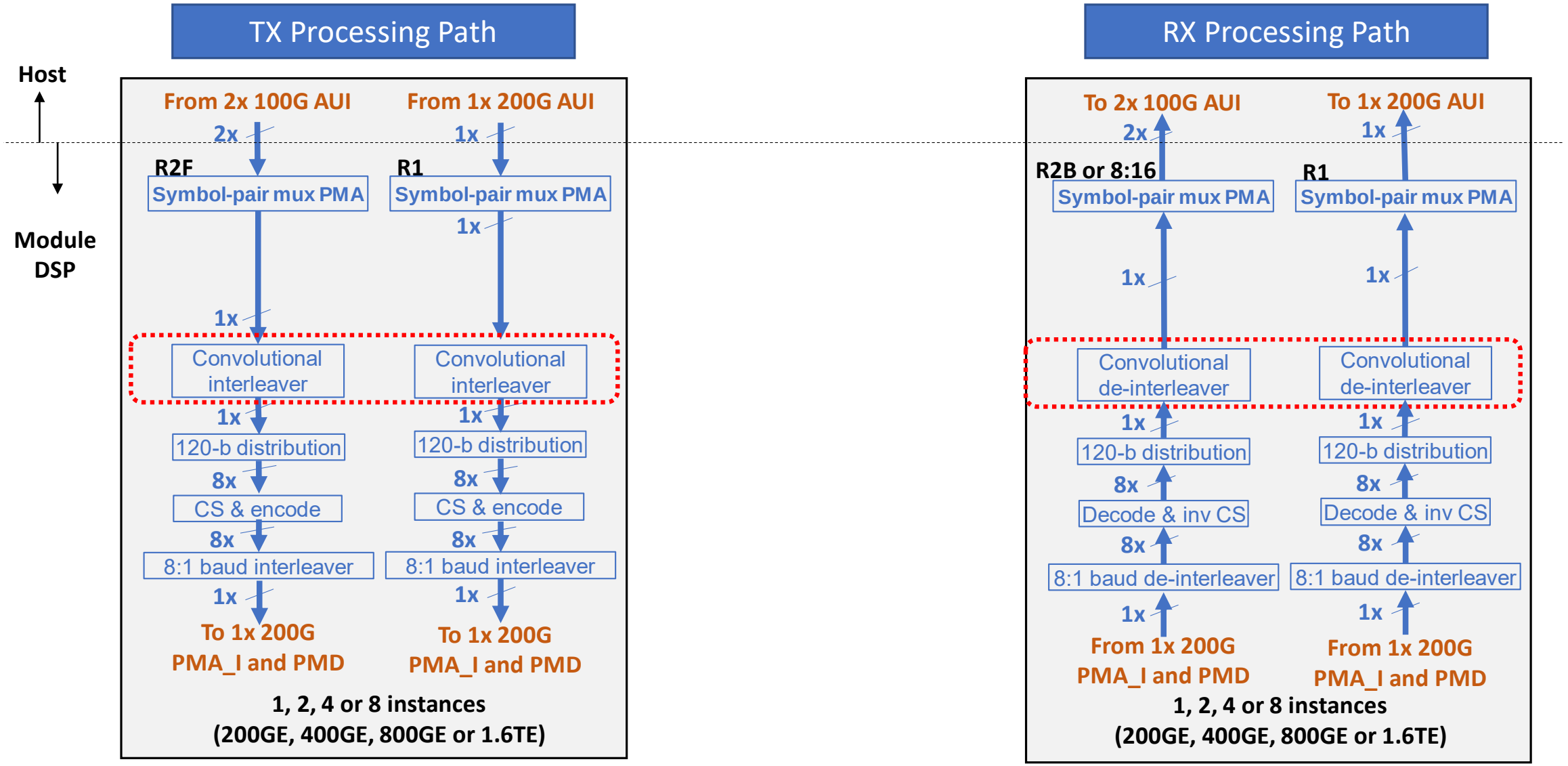
Proposed Update to Symbol-pair Muxing PMA:

- FEC_I sublayer is the sublayer below symbol-pair muxing PMA.

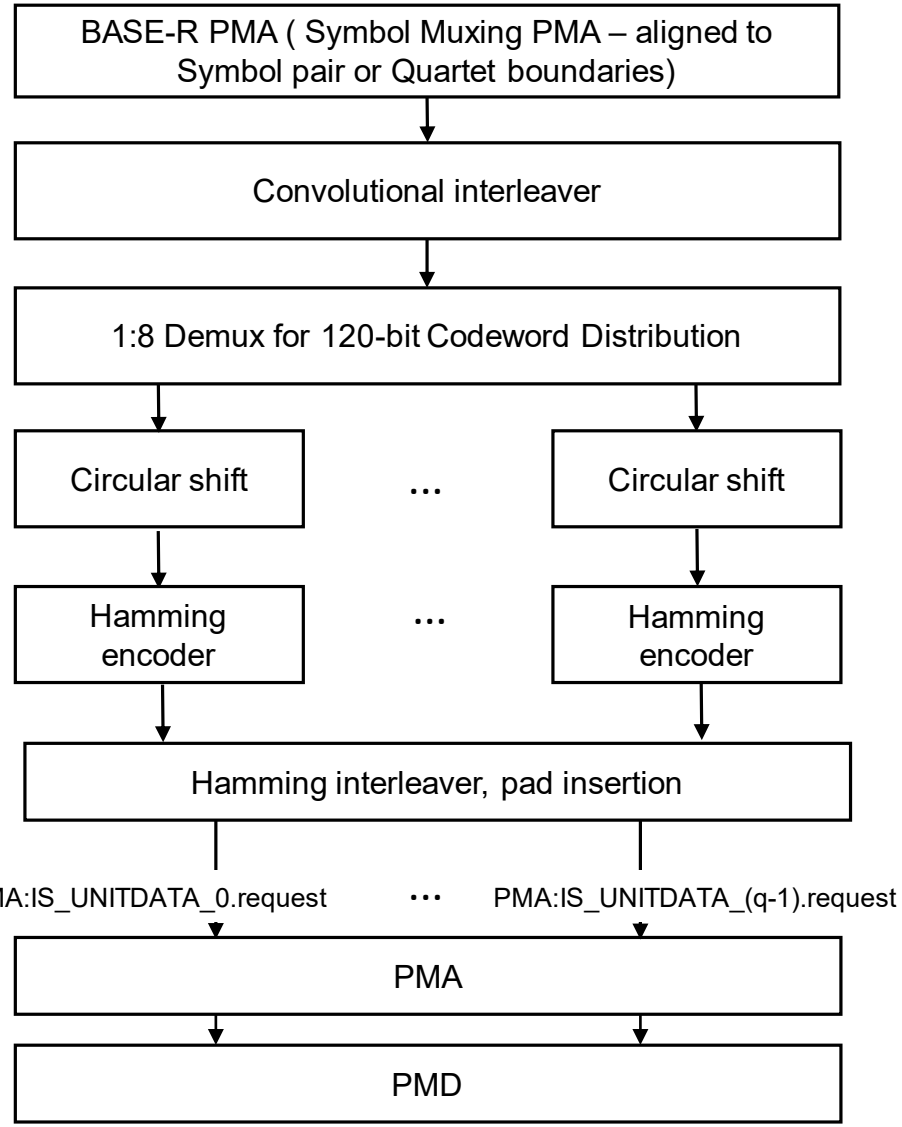
PMA family	Specific PMAs	Sublayer/interface above	Sublayer/Interface below
R8F	PMA(8:1)	200GBASE-R PCS / DTE XS	200GAUI-1 / **FEC_I** / PMD
	PMA(16:2)	400GBASE-R PCS / DTE XS	400GAUI-2 / **FEC_I** / PMD
	PMA(32:4)	800GBASE-R PCS / DTE XS	800GAUI-4 / **FEC_I** / PMD
R2F	PMA(2:1)	200GAUI-2	200GAUI-1 / **FEC_I** / PMD
	PMA(4:2)	400GAUI-4	400GAUI-2 / **FEC_I** / PMD
	PMA(8:4)	800GAUI-8	800GAUI-4 / **FEC_I** / PMD
R1	PMA(1:1)	200GAUI-1	200GAUI-1 / **FEC_I** / PMD
	PMA(2:2)	400GAUI-2	400GAUI-2 / **FEC_I** / PMD
	PMA(4:4)	800GAUI-4	800GAUI-4 / **FEC_I** / PMD
	PMA(8:8)	1.6TAUI-8	1.6TAUI-8 / **FEC_I** / PMD
	PMA(16:8)	1.6TBASE-R PCS / DTE XS / 1.6TAUI-16	1.6TAUI-8 / **FEC_I** / PMD

Source: ran_3dj_01a_2303, with modifications in **Blue**

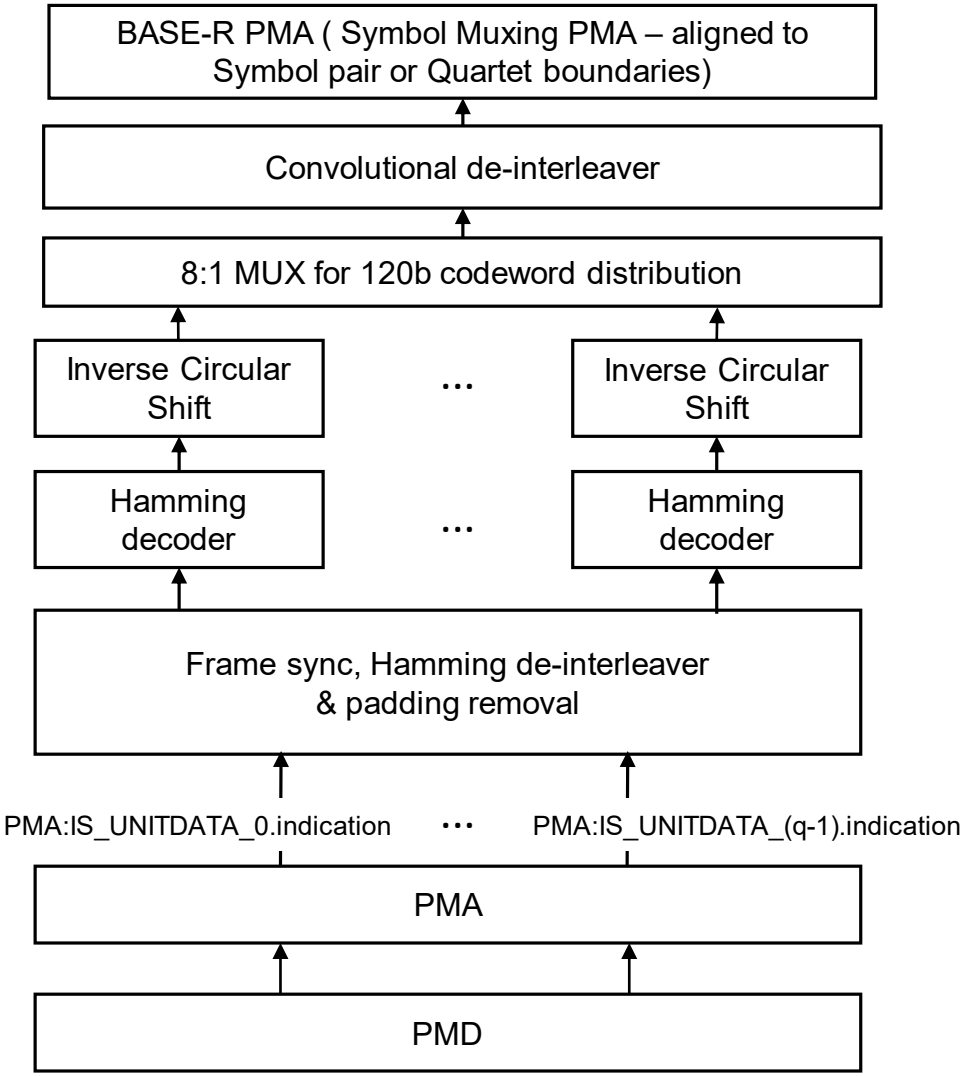
Example of Transmit and Receive Processing for FEC_I Sublayer with 200G/Lane & 100G/Lane AUI



Transmit path overview

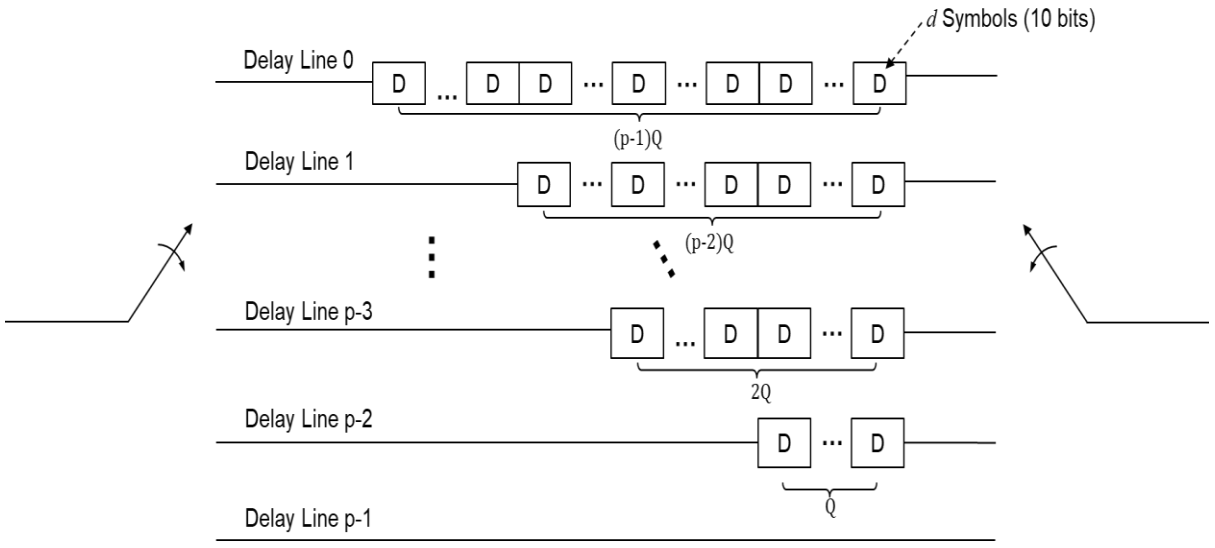


Receive path overview



200G/lane Common Convolutional Interleaver Design for 200G/400G/800G/1.6TbE

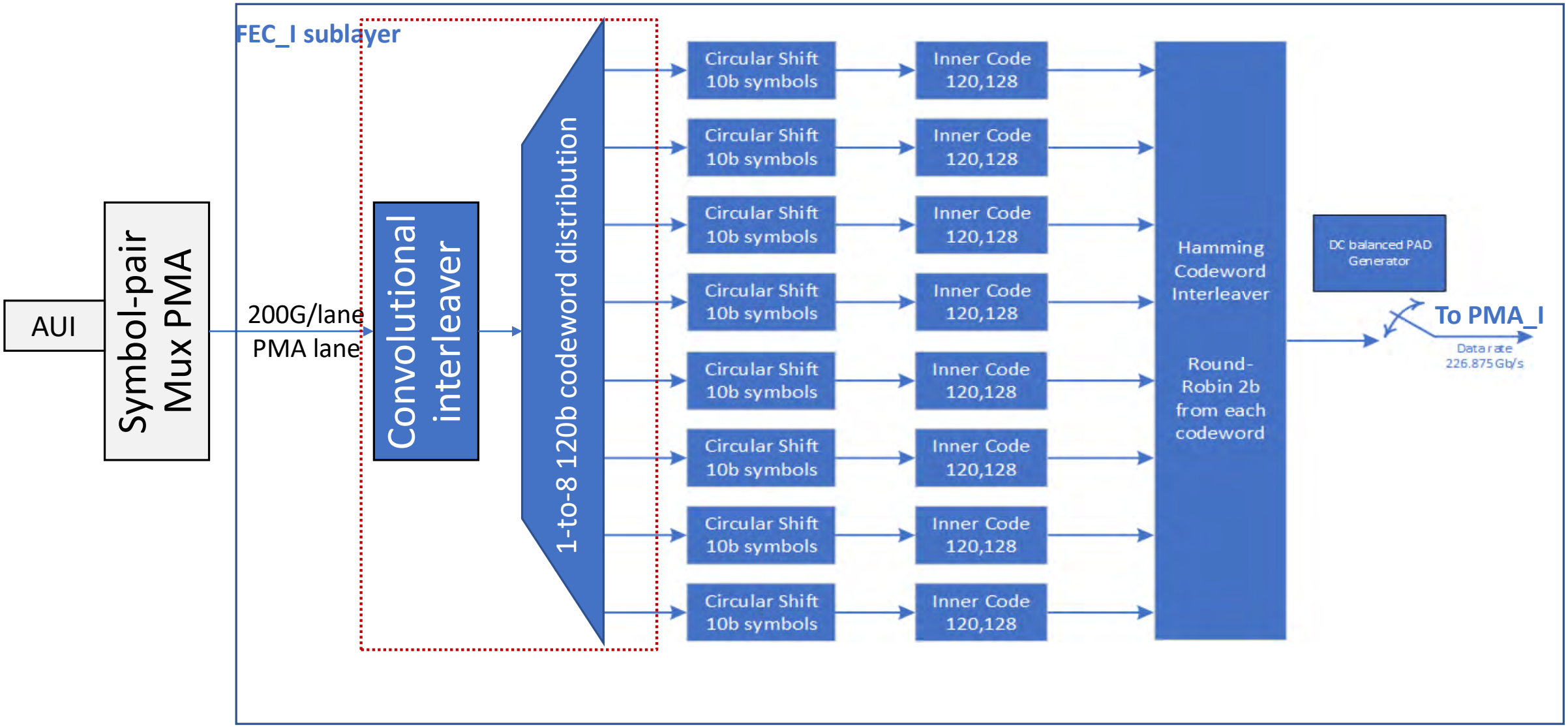
- An universal 200G/lane convolutional interleaver is proposed for different MACs to unify the processing
  - If 4x RS CWs interleaving in the PMA proposal is adopted, the convolutional interleaver logics will be further shared among all the MACs .
- For latency sensitive applications, convolutional interleaver can be bypassed.



Rate	d (RS symbol)	P	Q	Depth	Latency ns	FEC_I Lane Rate
1.6TE	4	3	24	12x RS	27.1	200G/lane
800GE	4	3	48	12x RS	54.2	
400GE	4*	3	96	12x RS	108.4	
200GE	4*	3	192	12x RS	216.8	
400GE	2	6	48	12x RS	135.5	
200GE	2	6	96	12x RS	271.1	

*If 4x RS interleaving for 200GE/400GE is adopted.

A complete View of FEC_I Sublayer Architecture with Common Convolutional Interleaver



Summary

- A common 200G/lane based convolutional interleaver for FEC_I sublayer is presented in this proposal for 200G/400G/800G/1.6T MAC configurations .
  - This is the key TBD item for a complete FEC_I sublayer baseline.
- The presented proposal also works well with already adopted FEC_I sublayer and 200G/lane symbol muxing based PMA sublayers.

Thank you!