Updates on Baseline Proposal for 200Gbps/Lane High-Loss AUIs

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IEEE P802.3dj Task Force

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Outline

- Background and Introduction
- BER Status Recap
- Loss Target Update
- Reference Receiver Consideration
- Summary & Proposal

Background and Introduction

- This presentation is the update to lit_3dj_elec_01_230622 with
  - COM analysis using the revised and new channels
  - Trending direction of reference receiver
- This presentation will focus on the following topics of high-loss AUI baseline
  - BER budget partitioning
  - AUI loss target
  - Reference receiver architecture

BER Status Recap

- **DER_0 value of 2.67e-5 was adopted for the higher-loss AUIs within a PHY**
  - **See motion #8, motions_3cwdfdj_2305**
  - **This is equivalent to random BER of 2e-5, or measured BER of 4e-5 with precoding ON**
    - See slide 5, ran_3dj_02_2305

- **ran_3dj_elec_02_230622 proposed the BER budget division between C2C and C2M**
- **lit_3dj_elec_01_230622 has shown a ~0.34dB dCOM between DER_0 of 1.33e-5 and 2.67e-5**

Motion #8

Move to:

- adopt a DER0 value of 2.67e-5 (equivalent to measured BER of 4e-5 with precoding ON) as the total allocation for higher-loss AUIs within a PHY (BER division between C2C and C2M as well as the measurement method to be determined later)

M: Adee Ran
S: Kishore Kota
Technical (>=75%) Procedural (>50%)
802.3 voters only
Results: Y: 75, N: 3, A: 20 passed 10:33 a.m.

Possible paths forward

A. Have different C2M BER allocation based on whether C2C is used or not
- Implies two sets of C2M specs for both hosts and modules

B. Allocate the whole error budget to the C2M
- If COM will be used, then DER_0=2.67e-5
- C2C can still be used in an xGMII Extender with a large error budget

C. Split the error budget evenly between C2M and C2C
- If COM will be used for both, then DER_0=1.33e-5 for both

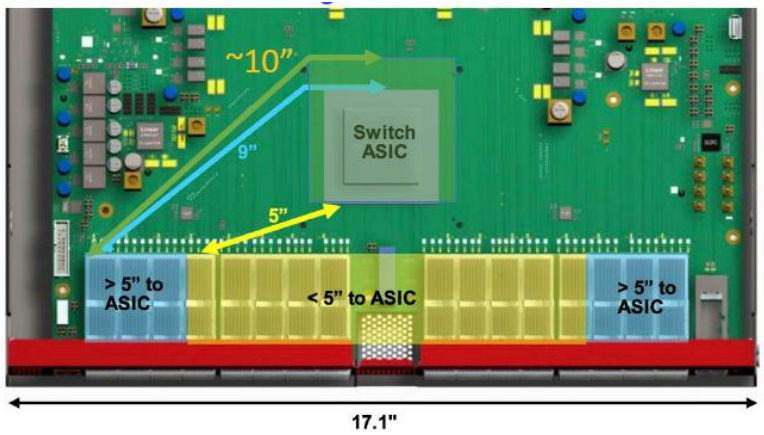
D. Give C2M a larger share
- A specific division: 90% for C2M and 10% for C2C

E. Give C2C a larger share
- Does not look interesting

Loss Target Updates

- **C2M bump-to-bump loss have been updated in kareti_3dj_01_2307**
  - **Considering high radix system with PCB implementation**
  - **Worst case loss is a little over 36dB**
  - **2/3 of channels have a loss less than 32dB**
- **C2C loss budget summarized in lit_3dj_01a_2305**
  - **mellitz_3dj_elec_01_230504 contributed Mezzanine channels of TP0-TP5 loss ~20.xdB with a total length of 260mm**
  - **Total package loss at two sides ~12dB**
    - 6-8dB package losses proposed in benartsi_3df_01a_2211, ghiasi_3df_01_220927, and li_3dj_02_2305
  - **Bump-to-bump loss ~32dB**

Source: stone_3ck_01a_0518 & ghiasi_3df_01_2211



Reference Parameter Highlights

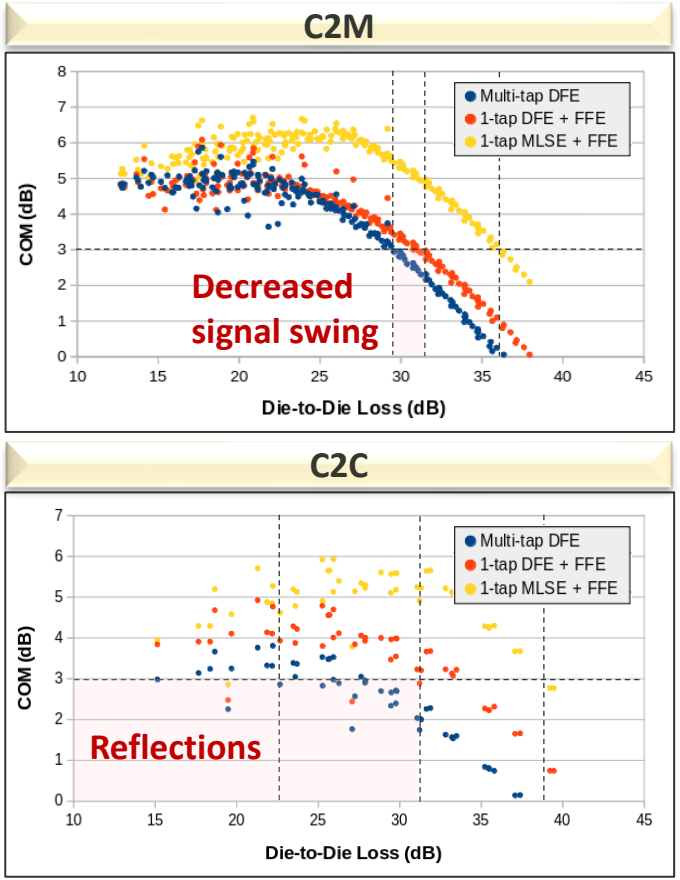
- **COM 4.0 used, test channels and spreadsheet in appendix**
- **Exploratory of reference receiver for 802.3dj AUIs**

Parameter	802.3ck C2M	802.3ck C2C	802.3ck CR	802.3ck KR	Multi-tap DFE	1-tap DFE + FFE	1-tap MLSE + FFE
DER_0	1E-5	1E-5	1E-4	1E-4	1.33E-5	1.33E-5	1.33E-5
SNR_TX	32.5	33	32.5	33	33	33	33
R_LM	0.95	0.95	0.95	0.95	0.95	0.95	0.95
TxFIR Length	4 (2 pre)	5 (3 pre)	5 (3 pre)	5 (3 pre)	6 (4 pre)	6 (4 pre)	6 (4 pre)
eta_0	4.10E-08	2E-08	9E-09	8.2E-09	8.2E-09	1.25E-08	1.25E-08
N_b	4	6	12	12	24	1	1
b_max(1)	0.4	0.65	0.85	0.85	0.75	0.75	0.75
ffe_pre_tap_len	-	-	-	-	0	4	4
ffe_post_tap_len	-	-	-	-	0	24	24
N_bg	0	0	3	3	6	6	6
N_bf	-	-	3	3	3	3	3
N_f	-	-	40	40	80	60	60
MLSE	-	-	-	-	0	0	1

Direction of Reference RX Architecture

** DER_0= 1.33e-5*

- DER_0 of 2.67e-5 generally improves SNR ~0.34dB from DER_0 of 1.33e-5
- RX architecture with multi-tap DFE is challenging to support the proposed IL target, regardless of DER_0 value, due to
  - Reflections
  - Signal swing reduction in handling pre-cursor ISI
- MLSE will be required in the baseline equalizer if we
  - Adopt AUI loss budget as 36 dB
  - Allow highly reflective channels
- Suggest to define AUI C2C and C2M based on 32dB loss target with receiver architecture of "1-tap DFE + FFE"
  - More details on the RxFFE implementation need further study, as proposed by [mellitz_3dj_01_2307]



Residual ISI Distribution: DFE- vs FFE-based Receiver

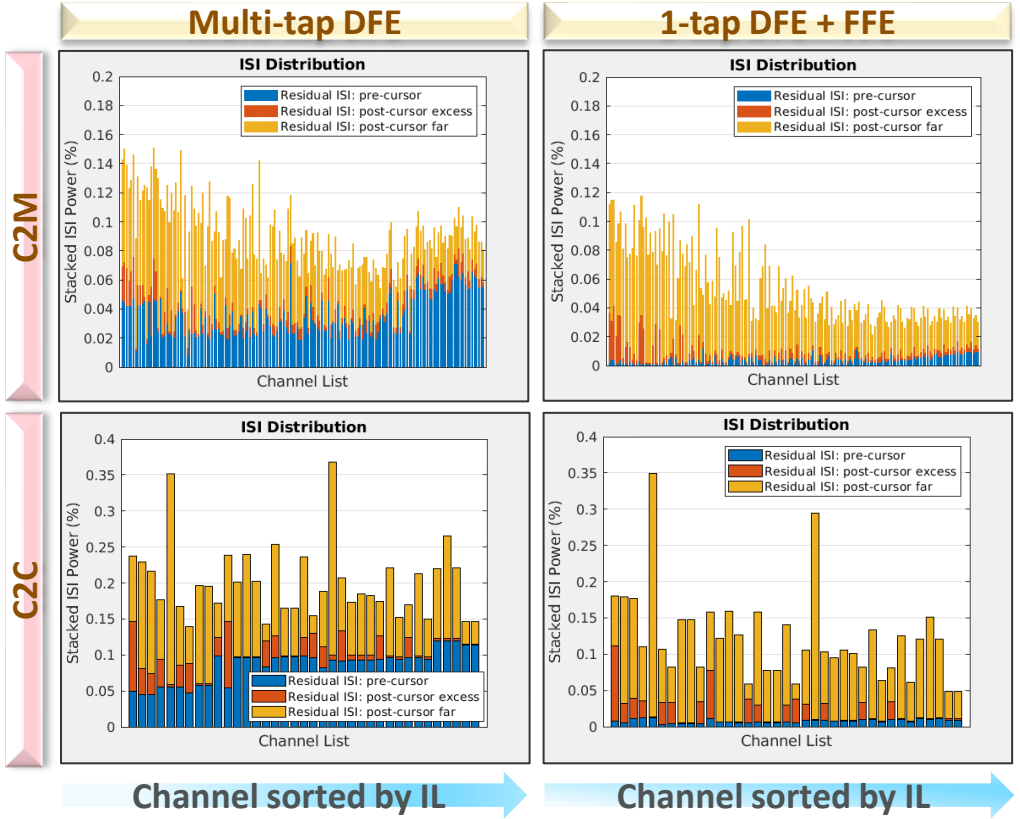
- **Medium loss AUIs will suffer from far-end reflections**

→ **Define proper channel spec or use longer EQ length**

- **High loss AUI will suffer from signal swing reduction and noise enhancement**

→ **Use RxFFE to mitigate pre-cursor ISI**

- *Two receiver architectures are compared under the identical noise assumption and equalization length*



Summary & Proposal

- Recommend a maximum die-to-die IL of 32dB for high-loss AUI C2C and C2M
- Recommend a reference RX architecture with “1-tap DFE + FFE” to support the proposed loss target for high-loss AUIs, regardless of DER_0 target
- Next step
  - Considering the necessity of low-loss AUI specification
  - More works required to complete RxFFE functionality in COM
  - Identify the key reference parameters based on a selected subset of representative channels
- Straw Poll requested to TF leadership on the
  - Die-die IL target for C2C and C2M
  - Direction of reference receiver architecture

Appendix

Channel List

Application	Contribution
C2M	rabinovich_3df_01_2209
	rabinovich_3df_02_2209
	rabinovich_3dj_02_230116
	rabinovich_3dj_03_230116
	Shanbhag_3dj_03_2305
	akinwale_3dj_02_2307
	akinwale_3dj_03_2307
	akinwale_3dj_04_2307
	lim_3dj_01_230629
	lim_3dj_02_230629
C2C	mellitz_3dj_elec_01_230504

Example COM Configuration for 200Gbps/L C2M

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[8 8 8; 0 0 0; 0 0 0 ; 0 0 0]	mm	[test cases]
z_p (FEXT)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 8 8; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.25E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Enforce Causality	1	
S-parameter magnitude extrapolation policy	trend_to_DC	

Filter: RxFFE		
ffe_pre_tap_len	4	UI
ffe_post_tap_len	24	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	0	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**

Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI

ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V

Floating Tap Control		
N_bg	6	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
MLSE	1	logical

Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Example COM Configuration for 200Gbps/L C2C

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (RX)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.25E-08	V^2/GHz
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R_LM	0.95	

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ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	

Table 93A-3 parameters		
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package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	0	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**

Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
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f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V

Floating Tap Control		
N_bg	6	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxs	0.2	max DFE value for floating taps

MLSE	0	logical

Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Thank you

Questions and Discussions