Impacts of FEC architectures on optical baselines and manufacturing

Guangcan Mi
Huawei Technologies Co. Ltd

Xu Sun
Crealights

Supporters

- Haifeng Liu, HG Genuine
- Wanchao Gao, Accelink
- Chenhui Jiang, Sicoya
- Frank Chang, Source Photonics
- Greg Le Cheminant, Keysight

Introduction

- 200G/lane optical transmission is challenging.
- Type II of FEC structure is adopted for optical PMDs based on 200G-PAM4 signaling
- What comes with the coding gain of the inner code is the additional latency, which is becoming unfavorable in DC applications, especially for AI and HPC.
- In welch_3dj_03c_2305 and dudek_3dj_optx_01_230629, enable by-pass function for the inner code was proposed, looking for balance between latency and link performance.
- The authors are in favor of the effort on providing low latency solutions, yet, with concerns over its change to optical specs, and more importantly, its impact to the optical module industry.
- To support future discussions on this topic, this contribution brings some consideration from manufacturing perspective.

Why we care: manufacturing matters

Manufacturing steps

- Component sorting
- Packaging
- Calibration Vectors
  - Include Tx bias points, DRV/TIA settings, DSP equalizer settings, etc
- Testing Vectors
  - OMA/RS/SRS/TECQ/TDECQ
  - BER curve
- Calibration and Testing are performed on EVERY module
  - For 200G/lane module, the calibration and test duration is estimated to be over 30mins,
- Burn in (VCSEL)
- Reliability validation
  - Long Hours performed on selected modules/lot

Impacting factors

- Automation & Testing Instrument
- Testing Time Counts
- Yield and Cost

Testing is a significant contributor to component cost
The baseline of testing is the standardized optical PMD specifications

How will FEC choice influence optical PMD specs

Case	A	B	C
FEC Configuration	With inner FEC	With inner FEC & **w/o interleaver**	Without inner FEC
Baudrate	113.4375 GBd		106.25 GBd
FEC limit	~4.85e-3[1] ~3.36e-3[2]	~3.46e-3[1] ~1.95e-3[2]	2.4e-4
Bessel-Thomson filter TDECQ	56.71875 GHz		53.125 GHz
Measurement Instrument (O/E converter and Oscilloscope)	3dB BW 56.76875 GHz 4thB-T response considered for 1.*x* * 113.4375GHz		3dB BW 53.125 GHz 4thB-T response considered for 1.*x* *106.25GHz
Rule of thumb targeting component BW（design)	79.40625 GHz		74.375 GHz

1: w/o Burst
2: w/ Burst Error(1tap DFE 0.5)

Leads to two sets of optical specs for one PMD
(e.g. 800G-DR4, 800G-DR4-2, 800G-FR4, 200G-FR1, etc.)

The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

How will the manufacturing change accordingly

If each optical PMD is mandated to satisfy both **Case A + Case C**

- Component sorting
  - Bypass mode likely requires higher performance components, especially with the already challenging 200G/lane
- Packaging
- Testing and Calibration x2
  - **Calibration Vectors** will be different for each case, especially for RF performance, so individual calibrations are required
  - **Testing Vectors ,** Tx TECQ/TDECQ, Rx RS/SRS will be tested in different settings
  - **BER curves** quite different for the two cases
- Burn in
- Reliability validation x2

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- Automation add new process flow
  - The manufacture flow of module will be different in consideration of different requirement of each case.
  - Testing instruments will need new settings
- Testing Time doubled
- Yield lowered and Cost added

If each optical PMD is mandated to satisfy both **Case A + Case B**

- Component sorting
- Packaging
- Testing and Calibration
  - Calibration Vectors
  - Testing Vectors
  - BER curves + 1 recording point
- Burn in & Reliability validation

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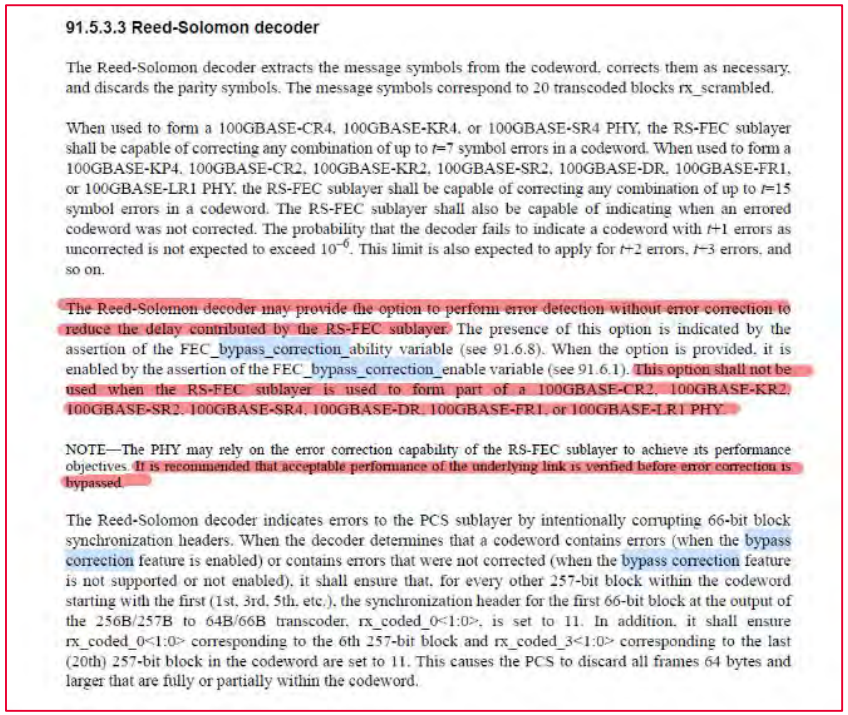
- Automation add one recording point of BER curve
- Testing Time ~minimally added
- Yield and Cost remain intact

Past example of FEC bypass handling

- FEC bypass is widely used in practice for 25G-NRZ based optical modules.
- IEEE defined FEC_bypass_correction in RS-FEC sublayer for 100GBASE-R PHYs, as detailed in CL91.5.3.3
  - Encode and decode still works: SAME signaling rate
  - Only bypassing correction to save on latency
- Optical modules are mass manufactured and tested against the spec table based on FEC_correction_on
- Sorting out those modules that could achieve the more stringent BER target, e.g. 1e-12, during the single process.



91.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols. The message symbols correspond to 20 transcoded blocks rx_scrambled.

When used to form a 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-SR4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 91.6.8). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 91.6.1). This option shall not be used when the RS-FEC sublayer is used to form part of a 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-SR4, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY.

NOTE—The PHY may rely on the error correction capability of the RS-FEC sublayer to achieve its performance objectives. It is recommended that acceptable performance of the underlying link is verified before error correction is bypassed.

The Reed-Solomon decoder indicates errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure rx_coded_0<1:0> corresponding to the 6th 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. This causes the PCS to discard all frames 64 bytes and larger that are fully or partially within the codeword.

Thoughts to carry when moving forward

- Though AI and HPC is rapidly growing, Ethernet optical modules see broad market in enterprise DC and telecom, where in stead of latency, reliability is highly valued.
- Testing cost constitutes a significant portion of the overall cost of modules.
- Looking at the various options of optical PMD baseline structures
  - A: Develop in-force optical PMD baselines based on FEC with inner code, 113.4375GBd signaling rate – Discrete Spec.
  - A + B: A + add an additional Receiver Sensitivity OMA value for bypass interleaver. – Integrated Spec.
  - A + C: Develop in-force optical PMD baselines based on FEC both with and without inner code , 113.4375GBd & 106.25GBd signaling rate– Integrated Spec.

  Other possibilities:
  - For particular PMDs, e.g. 500m, develop baseline based on KP4 FEC ONLY, provided data prove feasible – Discrete Spec.
  - List optical PMD baselines based on KP4 FEC only as informative
- It is good practice to maintain the structure of optical baseline, one spec for one PMD.
  - Easy to **share** the same manufacturing platform among **multiple modules and multiple Ethernet generations.**
  - Good for time-to-market and cost reduction.
- This contribution brings to the TF's attention the impact on implementation and manufacturing, when making changes to logic layer detail and optical specs.

Thank you.

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