Consensus Building on 800GBASE-FR4

Brian Welch (Cisco)

Guangcan Mi (Huawei)

Roberto Rodes (Coherent)

Supporters

- Drew Guckenburger (Maxlinear)
- Frank Chang (Source Photonics)
- Ed Ulrichs (Intel)
- Sridhar Ramesh (Maxlinear)
- John Johnson (Broadcom)
- Mark Kimber (Semtech)
- Tom Palkert (Samtech/Macom)
- Jeff Maki (Juniper Networks)

Overview

- Continuation of work in:
 - <u>https://www.ieee802.org/3/dj/public/23_05/rodes_3dj_02b_2305.pdf</u>
 - <u>https://www.ieee802.org/3/dj/public/23_05/mi_3dj_01a_2305.pdf</u>
 - <u>https://www.ieee802.org/3/dj/public/23_05/welch_3dj_02a_2305.pdf</u>
- Reconciliation of differences in power levels and budget
- Discussion ongoing on parameters related to TDECQ/TECQ/SECQ: FFE depth & tap limits, SER, Value, SRS

BER Requirements

This contribution does not recommend a specific option on the FEC architecture. FEC options are under study and still require more information

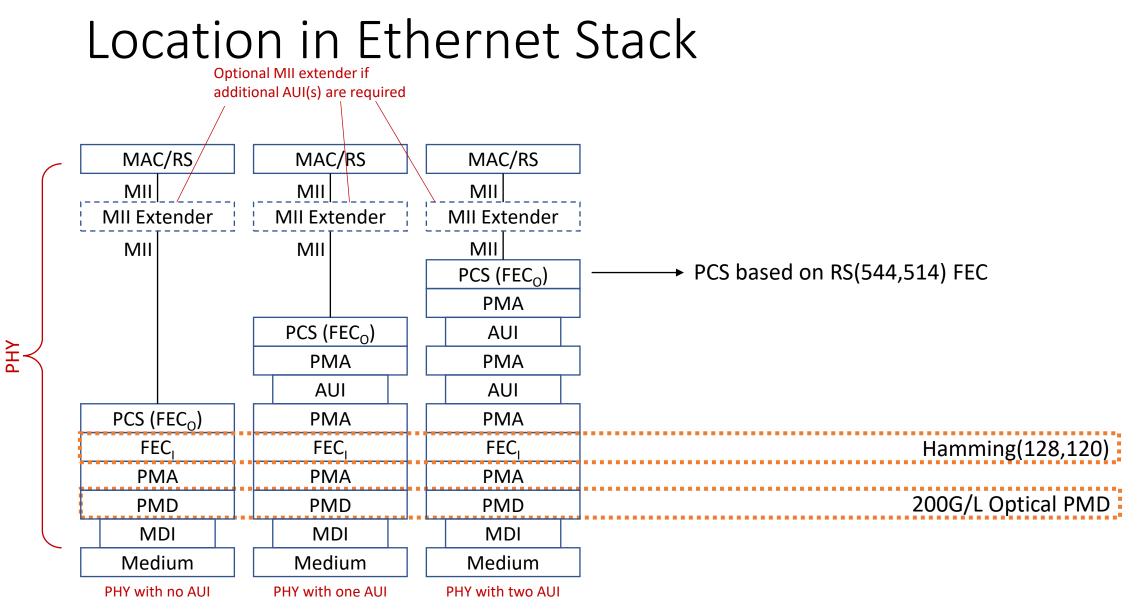
- The BER of the PMD link shall be less than 3 x 10⁻³ provided that the error statistics are sufficiently random that this results in a frame loss ratio of less than 1.7 x 10⁻¹² for 64-octet frames with minimum interpacket gap when processed with an 800GBASE-R/1.6TBASE-R PCS and inner code FEC sublayer.
 - Note: Exact pre-FEC BER level Hamming(128,120) inner FEC is not finalized.

TDECQ/TECQ/SECQ Reference Receiver

- TDECQ reference filter expanded from FFE5 (1 main + 4 pre/post cursors) to FFETBD (1 main + TBD pre/post cursors)
 - Introduce tap weight limits → Mitigate concerns of extreme TX BW restriction that could have deleterious effects on receiver performance/design

Tap Limits	Min	Max
Main Cursor	TBD	TBD
First Pre/Post Cursor	TBD	TBD
Second Pre/Post Cursor	TBD	TBD
All Other	TBD	TBD
Sum off all taps	1	1

 Note: TECQ/TDECQ/SECQ values and target SER revised to TBD, pending resolution of the questions raised in: https://www.ieee802.org/3/dj/public/adhoc/optics/0623 OPTX/leyba 3dj optx 01 230629.pdf



IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

Proposed Transmitter Specifications

Description	800GBASE-FR4	Unit
Signaling rate, each lane (Range)	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	
Lane wavelengths (range)	1264.5 to 1277.5	nm
	1284.5 to 1297.5	
	1304.5 to 1317.5	
	1324.5 to 1337.5	
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power, each lane (max)	4.9	dBm
Average launch power, each lane (min)	-1.8	dBm
Outer Optical Modulation Amplitude (OMA _{outer}), each lane(max)	4.8	dBm
Outer Optical Modulation Amplitude (OMA _{outer}), each lane(min) [†]		
for TDECQ < 1.4dB	1.3	dBm
for 1.4 dB \leq TDECQ \leq TDECQ (max)	-0.1+TDECQ	dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max) †	TBD	dB
TECQ (max) ⁺	TBD	dB
TDECQ - TECQ (max) ⁺	TBD	dB
Average launch power of OFF transmitter, each lane (max)	-15	dBm
Extinction ratio, each lane, (min)	3.5	dB
Transmitter transition time (max)	8	ps
Transmitter over/under-shoot (max)	22	%
RIN _x OMA (max)	-139	dB/Hz
Optical return loss tolerance (max)	17.1	dB
Transmitter reflectance (max)	-26	dB

⁺ Measured with FFETBD reference equalizer with SER = TBD

Proposed Receiver Specifications

Description	800GBASE-FR4	Unit
Signaling rate, each lane (Range)	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5	nm
Damage threshold, each lane	5.9	dBm
Average receive power, each lane (max)	4.9	dBm
Average receive power, each lane (min)	-5.6	dBm
Receive power, each lane (OMA _{outer}) (max)	4.8	dBm
Receiver reflectance (max)	-26	dB
Receiver sensitivity (OMA _{outer}), each lane (max)		
for TECQ < 1.4dB	-3.2	dBm
for 1.4 dB \leq TECQ \leq TECQ (max)	-4.6 + TECQ	dBm
Stressed receiver sensitivity (OMA $_{outer}$), each lane (max) †	TBD	dBm
Conditions of stressed receiver sensitivity test:		
SECQ [†]	TBD	dB
OMA _{outer} of each aggressor lane	1.9	dBm

⁺ Measured with FFETBD reference equalizer with SER = TBD

Proposed Link Budget

Description	800GBASE-FR4	Unit
Power budget (for max TDECQ)	TBD	dB
Operating distance	2000	m
Channel insertion loss	4	dB
Maximum discrete reflectance	-35	dB
Allocation for penalties (for max TDECQ)	TBD	dB
Additional insertion loss allowed	0	dB

Summary

- A Baseline proposal for 800GBASE-FR4 has been presented, representing the current state of consensus between the co-authors
- Parameters derived from a target SER (including TDECQ, TECQ, SECQ, and SRS) have been indicated as TBD