800GBASE-FR4 with Inner FEC Bypass

Brian Welch (Cisco)

Supporters

- Drew Guckenburger (Maxlinear)
- Ed Ulrichs (Intel)
- Sridhar Ramesh (Maxlinear)
- John Johnson (Broadcom)
- Mark Kimber (Semtech)
- Tom Palkert (Samtech/Macom)

Overview

- Expansion of work in welch_3dj_02_2307:
- Addition of Inner_FEC Bypass Mode

BER Requirements

This contribution does not recommend a specific option on the FEC architecture. FEC options are under study and still require more information

- Inner_FEC Bypassed: The BER of the PMD link shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed with an 800GBASE-R/1.6TBASE-R PCS.
- Inner_FEC Enabled: The BER of the PMD link shall be less than 3×10^{-3} provided that the error statistics are sufficiently random that this results in a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed with an 800GBASE-R/1.6TBASE-R PCS and inner code FEC sublayer.
 - Note: Exact pre-FEC BER level for Option B is not finalized.

TDECQ/TECQ/SECQ Reference Receiver

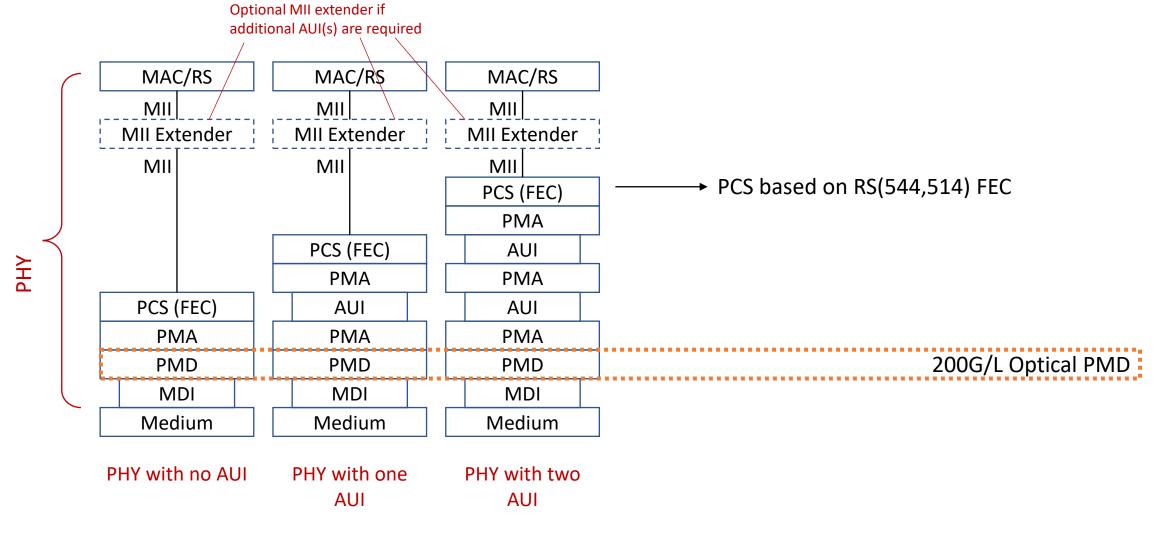
- TDECQ reference filter expanded from FFE5 (1 main + 4 pre/post cursors) to FFETBD (1 main + TBD pre/post cursors)
 - Introduce tap weight limits → Mitigate concerns of extreme TX BW restriction that could have deleterious effects on receiver performance/design

Tap Limits	Min	Max
Main Cursor	TBD	TBD
First Pre/Post Cursor	TBD	TBD
Second Pre/Post Cursor	TBD	TBD
All Other	TBD	TBD
Sum off all taps	1	1

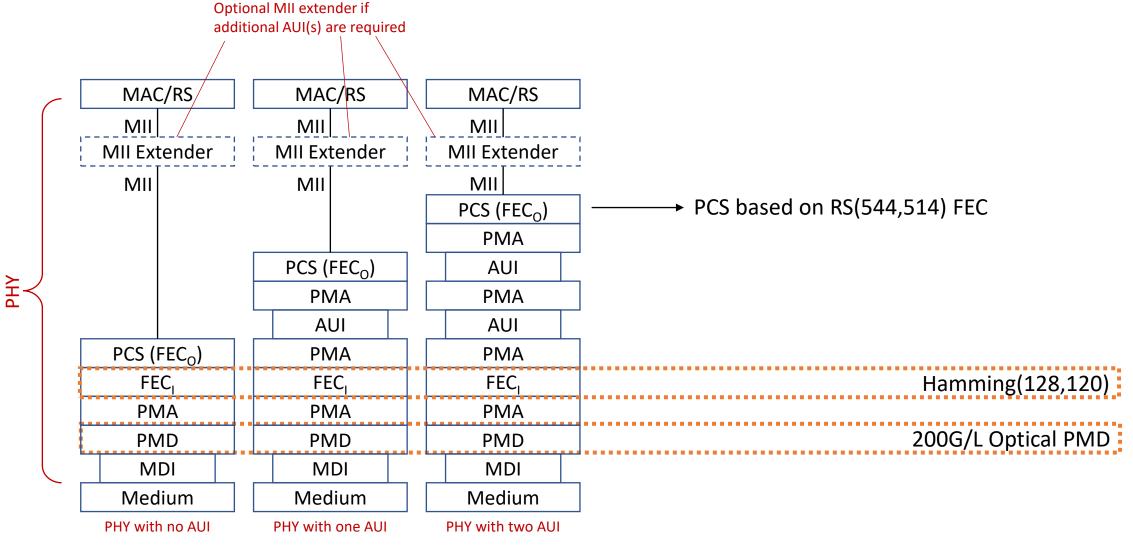
 Note: TECQ/TDECQ/SECQ values and target SER revised to TBD, pending resolution of the questions raised in:

https://www.ieee802.org/3/dj/public/adhoc/optics/0623 OPTX/leyba 3dj optx 01 230629.pdf

Location in Ethernet Stack: Inner FEC Bypassed



Location in Ethernet Stack: Inner FEC Enabled



Proposed Transmitter Specifications

Description	800GBA	800GBASE-FR4	
	RS(544,514)	RS(544,514) +Hamming(128,120)	
Signaling rate, each lane (range)	106.25 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PA	PAM4	
Language and the (range)	1264.5 t	1264.5 to 1277.5	
	1284.5 t	1284.5 to 1297.5	
Lane wavelengths (range)	1304.5 t	1304.5 to 1317.5	
	1324.5 t	1324.5 to 1337.5	
Side-mode suppression ratio (SMSR), (min)	3	30	
Average launch power, each lane (max)	4	4.9	
Average launch power, each lane (min)	-1	-1.8	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane(max)	4	4.8	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane(min)			
for TDECQ < 1.4 dB	1	1.3	
for 1.4 dB ≤ TDECQ ≤ TDECQ (max)	-0.1+TDECQ		dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	3.6ª	TBD ^b	dB
TECQ (max)	3.6ª	TBD ^b	dB
TDECQ - TECQ (max)	2.5ª	TBD ^b	dB
Average launch power of OFF transmitter, each lane (max)	-1	-15	
Extinction ratio, each lane, (min)	3	3.5	
Transmitter transition time (max)		8	
Transmitter over/under-shoot (max)	2	22	
RIN _x OMA (max)	-1	-139	
Optical return loss tolerance (max)	17	17.1	
Transmitter reflectance (max)	-2	-26	

^a Measured with FFETBD reference equalizer with SER = 4.8e-4

^b Measured with FFETBD reference equalizer with SER = TBD

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Signaling rate, each lane (range)	106.25 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PAN	PAM4	
Lane wavelengths (range)	1264.5 to	1264.5 to 1277.5	
	1284.5 to	1284.5 to 1297.5	
Lane wavelengths (range)	1304.5 to	1304.5 to 1317.5	
	1324.5 to	1324.5 to 1337.5	
Damage threshold, each lane	5.9	5.9	
Average receive power, each lane (max)	4.9	4.9	
Average receive power, each lane (min)	-5.	-5.6	
Receive power, each lane (OMA _{outer}) (max)	4.8	4.8	
Receiver reflectance (max)	-2	-26	
Receiver sensitivity (OMA _{outer}), each lane (max)			
for TECQ < 1.4 dB	-3.	-3.2	
for 1.4 dB ≤ TECQ ≤ SECQ	-4.6 +	-4.6 + TECQ	
Stressed receiver sensitivity (OMA _{outer}), each lane (max)	-1.1	TBD	dBm
Conditions of stressed receiver sensitivity test:			
SECQ	3.6ª	TBD ^b	dB
OMA _{outer} of each aggressor lane	1.9	1.9	
a Management with FFFTDD with CFD = 4.90.4	•		•

^a Measured with FFETBD with SER = 4.8e-4

b Measured with FFETBD with SER = TBD

Proposed Link Budget

Description	800GBASE-FR4 RS(544,514) +Hamming(128,120)		Unit
Power budget (for max TDECQ)	8	TBD	dB
Operating distance	2000		m
Channel insertion loss	4		dB
Maximum discrete reflectance	-35		dB
Allocation for penalties (for max TDECQ)	3.6	TBD	dB
Additional insertion loss allowed	0		dB

Summary

- A Baseline proposal for 800GBASE-FR4 with FEC bypass has been presented.
- Proposal contain requirements for operation with inner FEC bypassed or enabled.
- For inner FEC enabled operation parameters derived from a target SER (including TDECQ, TECQ, SECQ, and SRS) have been indicated as TBD