Enablement of multiple FEC modes for 200 Gb/s per lane 500 m and 2 km PMDs

Eric Bernier (Huawei)

Jonathan Ingham (Huawei)

Overview

- There is a clear desire for an option to support 500 m and 2 km optical PMDs that operate without the Hamming(128, 120) inner code
  - Principal motivation is to support low latency applications by avoiding convolutional interleaver required by the inner FEC
  - See Motion #9 at the July meeting
    - Motion passed to add “an option to support only RS544 FEC (aka Bypass Inner FEC) for the single wavelength 500m and 2km optical PMDs“
- However, there are significant concerns about how this support should be achieved by the Task Force
- This presentation provides a summary of possibilities and makes a recommendation

Goals to consider

- Robust interoperability
- Simplicity for the majority of end users
- Preserve the broad market potential
- Low latency support for sophisticated end users

Definitions

- **Mode_FECo**: Optical link runs with RS(544,514) FEC protection

- **Mode_FECi**: Optical link runs with RS(544,514) FEC protection operating as an outer code, supplemented by Hamming(128,120) FEC protection operating as an inner code

Option 1: Define single PMD (“combined specification” approach)

- Combined specifications
  - Specifications for Mode_FECo and Mode_FECi combined
  - Transmitter is **allowed** to comply to **either** Mode_FECo or Mode_FECi operating condition
  - Receiver is **required** to comply to **both** Mode_FECo and Mode_FECi operation conditions
- Pros
  - Low latency is supported by one PMD
  - No objective changes required
- Cons
  - Potentially confusing for some end users
  - Receiver must support two modes
  - Testing may be more costly

Option 2: Define separate PMDs (“discrete specification” approach)

- Discrete specifications
  - Specifications for Mode_FECo and Mode_FECi provided separately
  - Transmitter is **allowed** to comply to **either** Mode_FECo or Mode_FECi operating condition
  - Receiver is **required** to comply to **either** Mode_FECo or Mode_FECi operation conditions
- Pros
  - Low latency is supported by one PMD
  - Link specification is set by IEEE
- Cons
  - Potentially confusing for end users
  - Requires modification of objectives
    - No support for this change (see recent motion)

Option 3: Define single PMD while allowing for engineered link

- Single simplified specification
  - A single PMD based on Mode_FECi is defined
  - Links using **Mode_FECo** are possible; sophisticated end users work with engineered link guidance, similar in spirit to 40GBASE-ER4, 100GBASE-ER4, 200GBASE-ER4 and others
  - Interoperability on the standard is guaranteed on the **Mode_FECi** and best effort on **Mode_FECo**
- Pros
  - No ambiguity that the standard requires the Hamming(128, 120) inner code
  - However, sophisticated end users are able to use the same chipsets and technology base to achieve links without use of the inner code
  - Sophisticated end users are provided with guidance on how to achieve operation without the inner code
  - No objective changes required
- Cons
  - No significant cons, merely a small amount of additional work to include the engineered link tables

Recommendation

- Option 3 is recommended
- This approach meets the desire to support an option for low latency applications, via additional engineered link guidance
- However, the vast majority of end users benefit from a clear single specification, based around use of the inner code, with robust interoperability
- Shared technology base amongst end users and industries

Example Specification

Proposed Transmitter Specifications

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	113.4375 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	30	dB
Average launch power, each lane (max)	4	4	dBm
Average launch power, each lane (min)	-2.8	-2.1	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(max)	4.2	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(min) for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ TDECQ (max)	 0.2 -1.2 + TDECQ	 0.9 -0.5 + TDECQ	 dBm dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	TBD[a]	TBD[a]	dB
TECQ (max)	TBD[a]	TBD[a]	dB
|TDECQ - TECQ| (max)	TBD[a]	TBD[a]	dB
Average launch power of OFF transmitter, each lane (max)	-15	-15	dBm
Extinction ratio, each lane, (min)	3.5	3.5	dB
Transmitter transition time (max)	8	8	ps
Transmitter over/under-shoot (max)	22	22	%
RIN_xOMA (max)	-139	-139	dB/Hz
Optical return loss tolerance (max)	21.4 (15.5 for DR1)	21.4 (17.1 for FR1)	dB
Transmitter reflectance (max)	-26	-26	dB

[a] Measured with FFETBD reference equalizer with SER = 6e-3

Proposed Receiver Specifications

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	113.4375 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Damage threshold, each lane	5	5	dBm
Average receive power, each lane (max)	4	4	dBm
Average receive power, each lane (min)	-5.8	-6.1	dBm
Receive power, each lane (OMA_{outer}) (max)	4.2	4.2	dBm
Receiver reflectance (max)	-26	-26	dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ SECQ	 -2.9 -4.3 + TECQ	 -3.5 -4.9 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	TBD[a]	TBD[a]	dBm
Conditions of stressed receiver sensitivity test:			
SECQ	TBD[a]	TBD[a]	dB
OMA_{outer} of each aggressor lane[b]	4.2	4.2	dBm

[a] Measured with FFETBD reference equalizer with SER = 6e-3
[b] No aggressors needed for 200GBASE-DR1 or 200GBASE-FR1

Proposed Link Budget

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Power budget (for max TDECQ)	TBD	TBD	dB
Operating distance	500	2000	m
Channel insertion loss	3	4	dB
Maximum discrete reflectance	-35	-35	dB
Allocation for penalties (for max TDECQ)	TBD	TBD	dB
Additional insertion loss allowed	0	0	dB

Example of engineered link guidance

- Transmitter specification guidance to enable Mode_FECo (all other specifications unchanged)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	106.25 ± 50 ppm	106.25 ± 50 ppm	GBd
Transmitter and dispersion eye closure (TDECQ), each lane (max)	3.4[a]	3.4[a]	dB
TECQ (max)	3.4[a]	3.4[a]	dB
|TDECQ - TECQ| (max)	2.5[a]	2.5[a]	dB

[a] Measured with FFETBD reference equalizer with SER = 4.8e-4

Example of engineered link guidance

- Link budget for Mode_FECo

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Power budget (for max TDECQ)	6.5	7.8	dB
Operating distance	500	2000	m
Channel insertion loss	3	4	dB
Maximum discrete reflectance	-35	-35	dB
Allocation for penalties (for max TDECQ)	3.5	3.8	dB
Additional insertion loss allowed	0	0	dB

Example of engineered link guidance

- Receiver specification guidance to enable Mode_FECo (all other specifications unchanged)

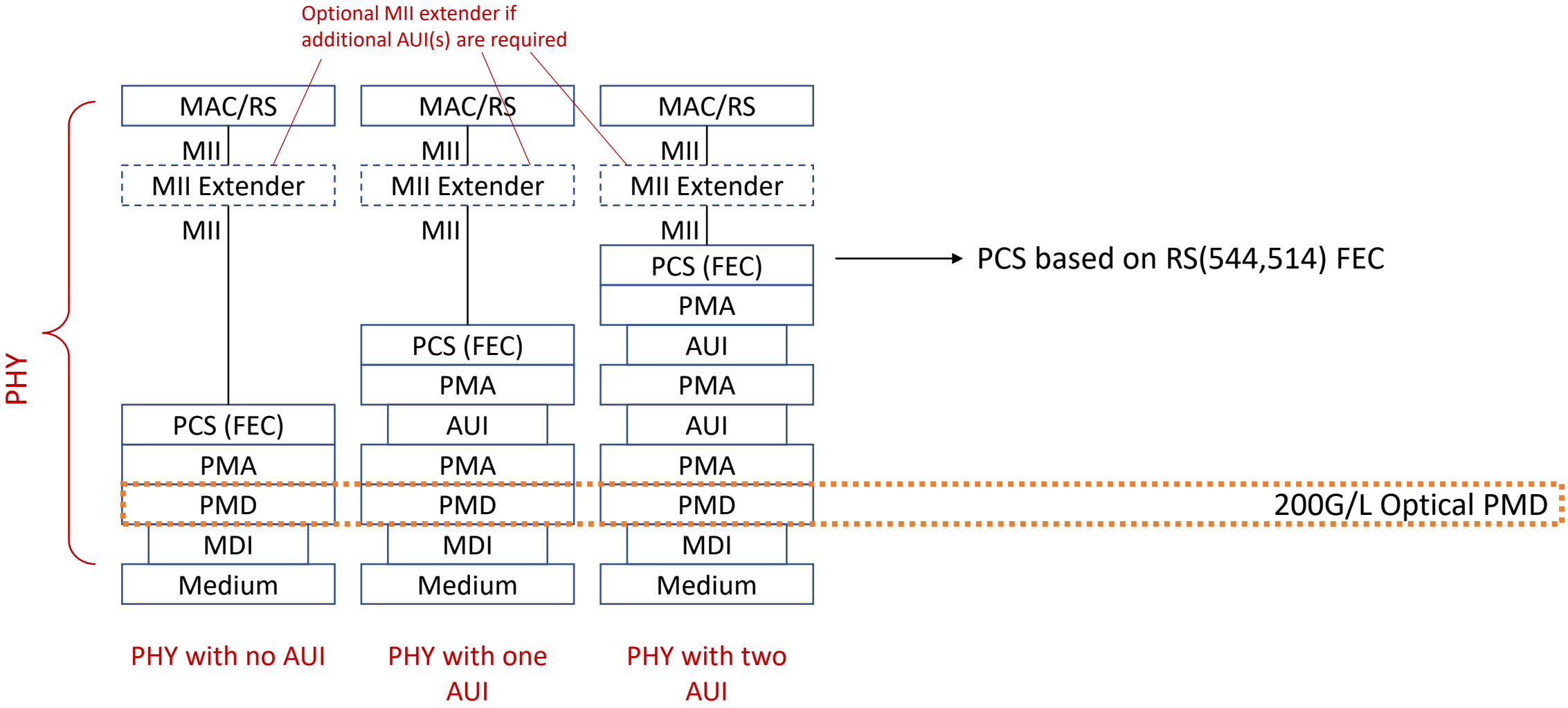
Description	**200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8**	**200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2**	**Unit**
Signaling rate, each lane (range)	106.25 ± 50 ppm	106.25 ± 50 ppm	GBd
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	-0.9[a]	-1.5[a]	dBm
Conditions of stressed receiver sensitivity test:			
SECQ	3.4[a]	3.4[a]	dB

[a] Measured with FFETBD reference equalizer with SER = 4.8e-4

Thank You

& Backup

Location in Ethernet Stack: RS(544,514) only



Location in Ethernet Stack: RS(544,514) + Hamming(128,120)