Toward AUI C2M Baseline Assuming Two Package Classes

Ali Ghiasi – Ghiasi Quantum/Marvell
Henry Wong – Alphawave
David Cassan – Alphawave

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Supporters

- **Matt Brown – Alphawave**
- **Jim Weaver – Arista**
- **Kent Lusted – Intel**
- **Rick Rabinovich –Keysight Technology**
- **Arash Farhoodfar – Marvell**
- **Mike Dudek – Marvell**
- **Tobey Li – MediaTek.**

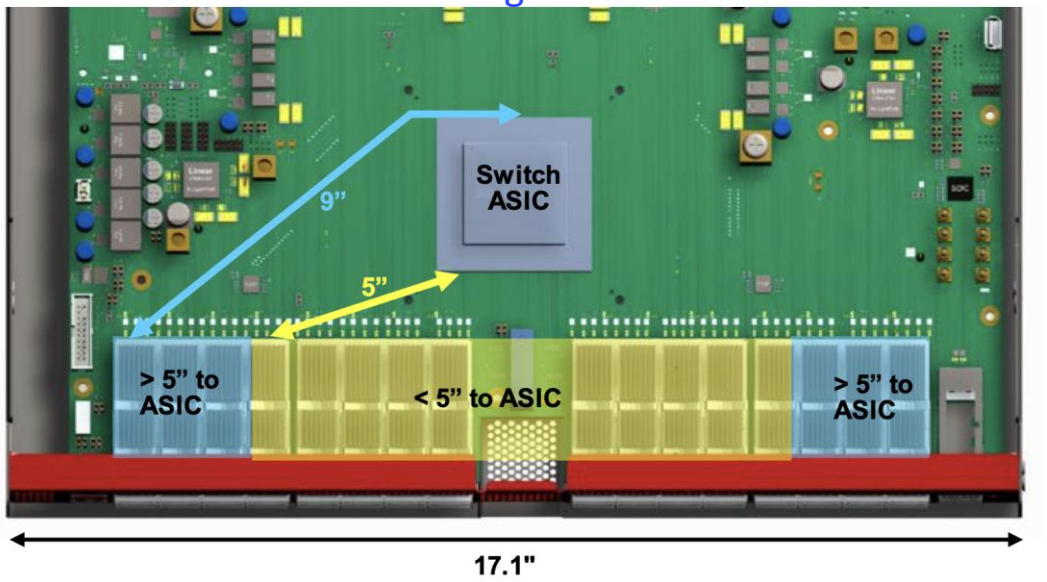
Overview

- C2M reference application model
- Defining two host packages
- C2M hosts loss considering package A and B
- Bottom C2M loss with package A and B
- Increasing C2M loss doesn’t come for free
- Proposed C2M loss budget
- Summary.

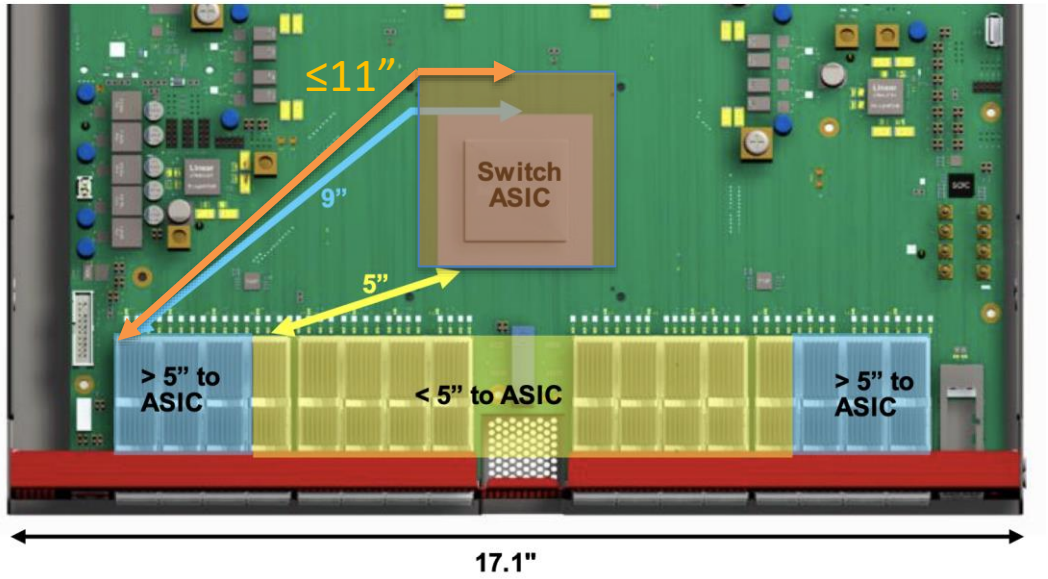
Most Common Switch Implementation

- **In 802.3ck max C2M PCB length assumed was 9” per recommendation stone_3ck_01a_0518**
  - In CL120G max host PCB loss is 11.9 dB based on above recommendation for PCB with loss ~1.2 dB/in
  - weaver_3dj_elec_01_230831 C2M channel go up to 9” and was stated during Q&A the upper limit of 10”
    - Any application needing more than 10” has the option to use cabled host or retimers
  - PCB length 10 to 11” expect to cover common 512 lanes switch implementations!

Stone Hypothetical 256 Lane Switch
Package ~69x69



Hypothetical 512 lane (102T) Switch
Package ~90x90



DJ Direction is to Define Two Difference Host Packages

- **Class A package loss is 0.15 dB/mm @ 90 °C and Class B loss is 0.21 dB/mm @ 90 °C**
  - See lim_3dj_02_2307 and the consensus presentation lusted_3dj_elec_01_230817
    - For consistency package type A and B are replaced with class A and B in lim_3dJ_02_2307.

Comparison of Key Design/Material Characteristics of "Class A" vs "Class B" PKGs

Package	"Class A"	"Class B"
ABF (Ajinomoto build-up film) material	GL107 Like	NA
Cross-section	8-2-8, or 10-2-10	6-2-6, to 9-2-9
Core thickness	~1000 µm	800-1200 µm
Trace routing lengths	33 mm max	30-40 mm max
Surface treatment	CZ8401 Like	NA
BGA ball pitch	0.8 mm	> 1.0 mm
Skip Layer	Yes (x%)	No
Trace line / space	~30 / 60 / 30 µm	27-45-27 µm
Trace line / space (Skip Layer)	~80 / 80 / 80 µm	NA
Impedance	~87.5 ohms	90-92 ohms
ABF height	35 µm	40 µm

Package Trace	Class A Loss (dB)	Class B Loss(dB)
15 mm	2.25	3.15
30 mm	4.5	6.3
45 mm	6.75	9.45

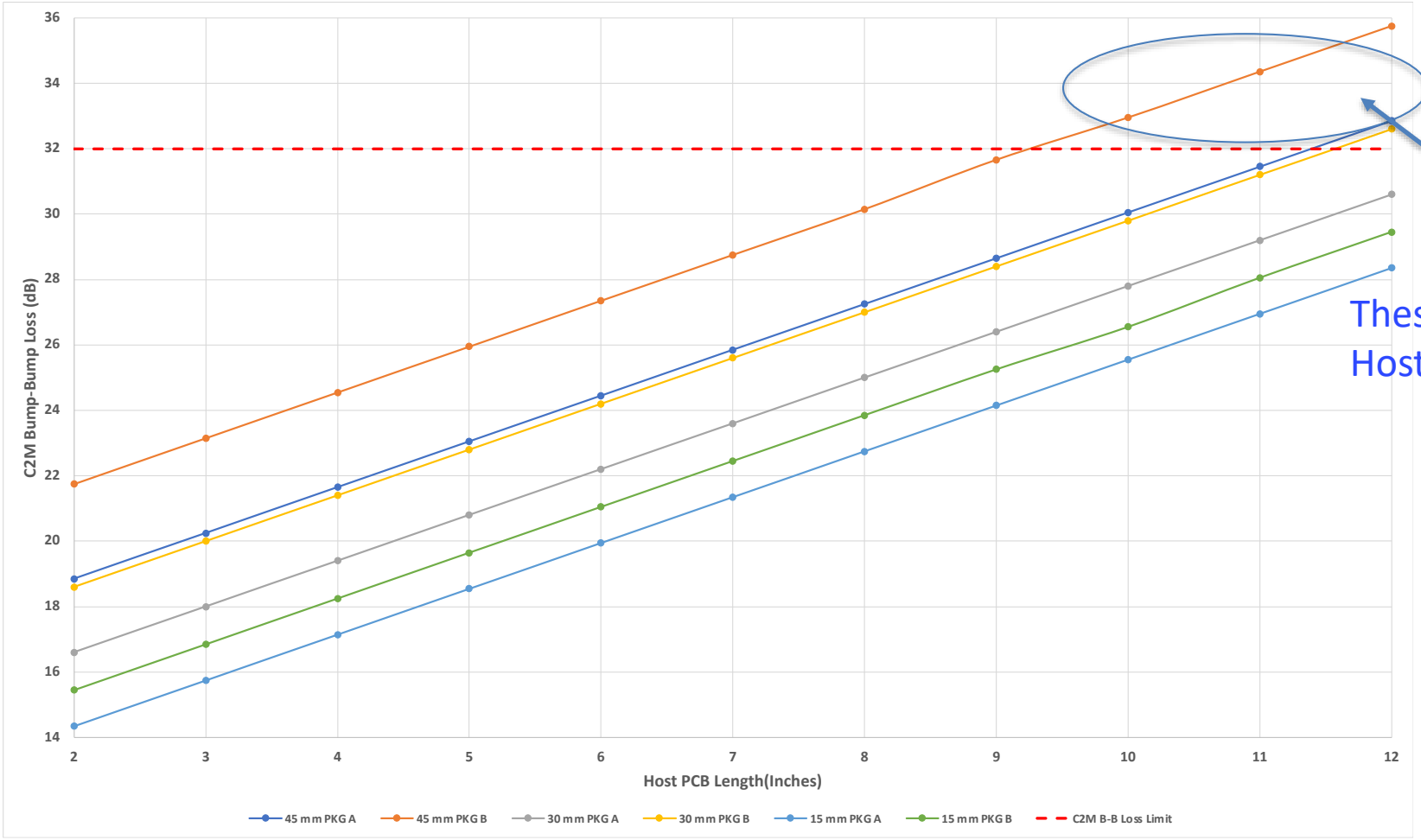
AUI Bottom-Up Analysis with Package Class A and B

- **AUI contribution ghiasi_3dj_02a_2307 bottom-Up analysis now include PKG A (0.15 dB/mm) in addition to the original PKG B (0.21 dB/mm)**
  - 1 dB excess via loss is added on top of weaver_3dj_elec_01_230831 1.4 dB/in channel loss @80 °C for > 3 mm vias
  - 0.8 dB excess loss added for PKG A mode conversion and 1.0 dB for PKG B
  - With 32 dB bump-bump loss PKG A support 11.4" of PCB and PKG B supports 9.3" of PCB
    - With modest planning not connecting PKG(long)-PCB(long) AUI C2M loss can be reduced to 30 dB for potential power saving
  - Proposed common AUI application for all front pluggable TP0b-TP1a loss ≤29.5 dB.

Loss Parameters @ 53 GHz A. Ghiasi - Rev 1.3 9/1/2023	Host1 with PKG A	Host2 with PKG B	Length or # PKG A	Length or # PKG B	AUI Conventional PCB PKG A	AUI Conventional PCB PKG B	AUI Cabled Host PKG A	AUI Cabled Host PKG B
Host PCB Loss (dB/in)	1.4	1.4	11.4	9.3	15.96	13.02	NA	NA
Cabled Host PCB Loss (dB/in)	1.4	1.4	2	2	NA	NA	2.8	2.8
Cable Loss (dB/in)	0.3		18	18	NA	NA	5.4	5.4
Plug Board/PIC/HCB Loss (dB/in)	1.5	1.5	2	2	3	3	3	3
AUI Connector Loss (dB)	2	2	NA	NA	2	2	2	2
Excess Host Via Loss (dB)	1	1	NA	NA	1	1	1	1
Host Package Loss (dB/mm)	0.15	0.21	45	45				
Host PKG Mode Con. Loss (dB)	0.8	1	NA	NA				
CDR Package Loss (dB/mm)	0.21	0.21	10	10				
CDR PKG Mode Con. Loss (dB)	0.4	0.4	NA	NA				
Total Host PKG Loss (dB)					7.55	10.45	7.55	10.45
Total CDR PKG Loss (dB)					2.5	2.5	2.5	2.5
TGA Connector Loss (dB)	0.3	0.3	NA	NA	NA	NA	0.3	0.3
Socket Loss (dB)	0.2	0.2	NA	NA	NA	NA	0.2	0.2
TP0-TP1a Loss (dB)	NA	NA	NA	NA	21.96	19.02	14.7	14.7
Bump-TP1a (dB)	NA	NA	NA	NA	29.51	29.47	22.25	25.15
Bump-Bump Loss (dB)	NA	NA	NA	NA	32.01	31.97	24.75	27.65

AUI C2M at 32 dB Bump-Bump Loss has Greater Reach than CL120G

- **AUI C2M at 32 dB on 45 mm package supports ~11.4” with PKG A and ~9.3” with PKG B**
  - We leverage CR/KR package-PCB pairing then AUI C2M loss can reasonable be reduced to 30 dB.

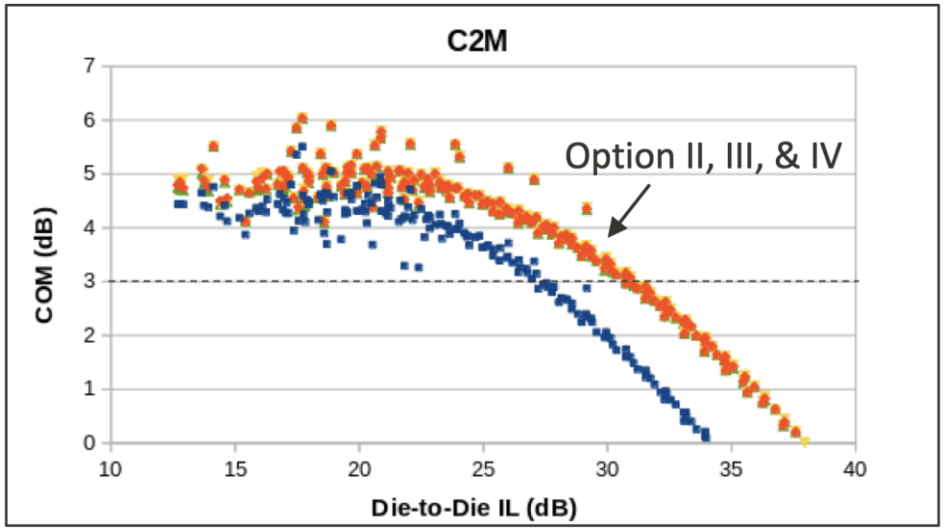


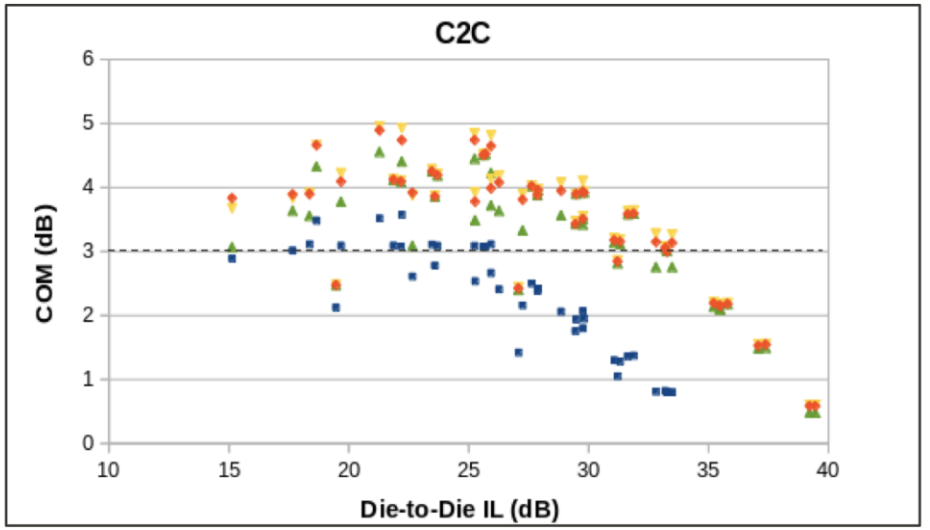
Increasing C2M Loss isn't Free

- **lit_3dj_elec_01a_230817 COM analysis indicates**
  - Steep penalty beyond 30 dB with COM failing
  - Considering thermal limit in optical module the C2M SerDes need to have at least 25% lower power than CR/KR
  - Considering DJ C2M will support greater PCB trace than CK reducing C2M loss to 30 dB can further simplify C2M
    - 9-12" of PCB trace still would be supported if one avoids connecting long PKG with long PCB.

**** Number of post-taps***

Option I	24 fixed DFE tap + 18 floating DFE tap
Option II	1 fixed DFE tap + 24 fixed FFE tap + 18 floating DFE tap
Option III	1 fixed DFE tap + 60 fixed FFE tap
Option IV	1 fixed DFE tap + 24 fixed FFE tap + 18 floating FFE tap



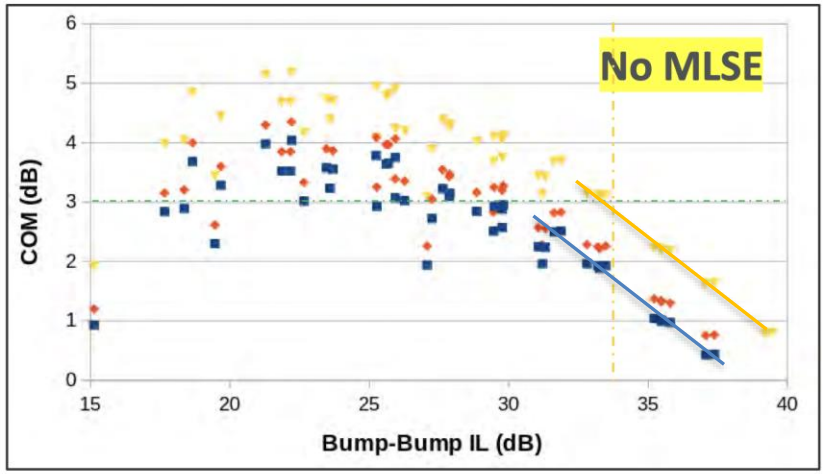


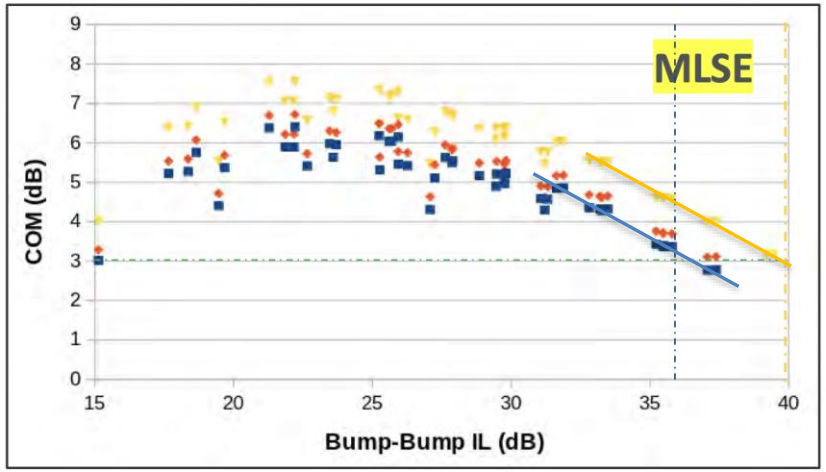
DER0=1.33E-5

Option I
Option II
Option III
Option IV

Increasing C2M AUI BER is Costly

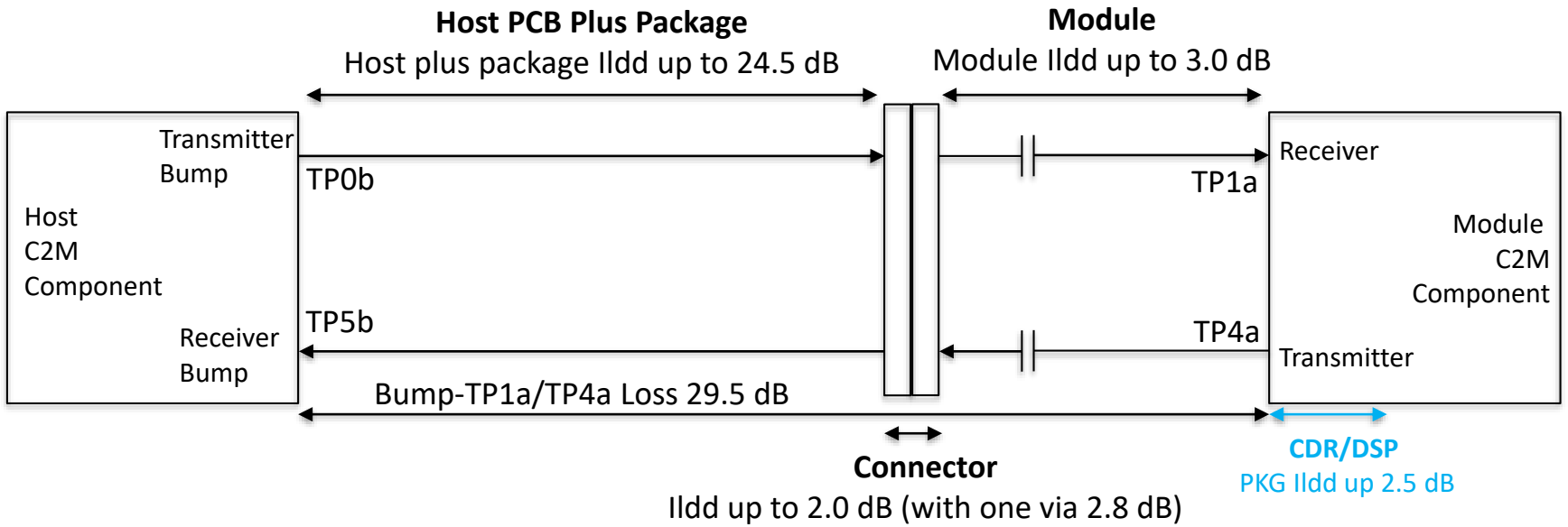
- **lit_3dj_01a_2305 results show a C2M AUI operating at 1E-5 compared to KR link operating at 1E-4 for constant 3 dB require require 3 dB lower loss**
  - If C2M loss is pushed to 36 dB with more strengthen BER then for all practical purposes the C2M SerDes is the same as KR but without FEC termination!





AUI C2M Application Reference Model

- **AUI C2M total loss for DJ proposed to be from TP0b(bump) -TP1a**
  - Recommend to use TP0b for Tx bump
  - Recommend to use TP5b for Rx bump
  - C2M max TP0b -TP1a (TP4a-TP5b) loss ≤ 29.5 dB at 53.125 GHz
  - Max host PCB + package losses including two vias ≤ 24.5 dB
  - C2M AUI bump-bump loss including CDR/DSP package loss would be ≤ 32 dB.



Summary

- **Proposed AUI C2M with max bump-bump loss of 32 dB on 45 mm package trace supports 11.4” of PCB with PKG A and 9.3” with PKG B without needing to avoid pairing long PKG with long PCB**
  - At 32 dB bump-bump the DJ C2M AUI will provide greater PCB length than CK CL 120G
  - AUI C2M at 32 allow increasing PCB traces beyond 11.4”/9.3” with modest pairing of PKG traces with PCB traces
    - With modest pairing of host package with PCB traces the C2M bump-bump loss can be reduced to 30 dB
- **Proposed AUI C2M to have max bump-bump loss of ≤32 dB**
  - Informative C2M loss specifications from TP0b-TP1a and TP4a-TP5b with a loss of ≤29.5 dB
  - Informative host PCB loss + package loss propose to be ≤24.5 dB
- **Pushing the C2M AUI BER to 36 dB with about an order of magnitude lower BER than KR then for all practical purpose the C2M SerDes technology is the same as 40 dB KR**
- **Some thought on AUI C2M BER**
  - AUI C2M is more challenging than C2C channel given the nature of pluggable modules and C2M 200G edge connector must be backward compatible
  - Given the above constrain C2M BER allocation within a PHY should be higher then C2C.