212.5 Gbps-PAM4 CR End-to-End Link COM Analysis and Simulations: Design C

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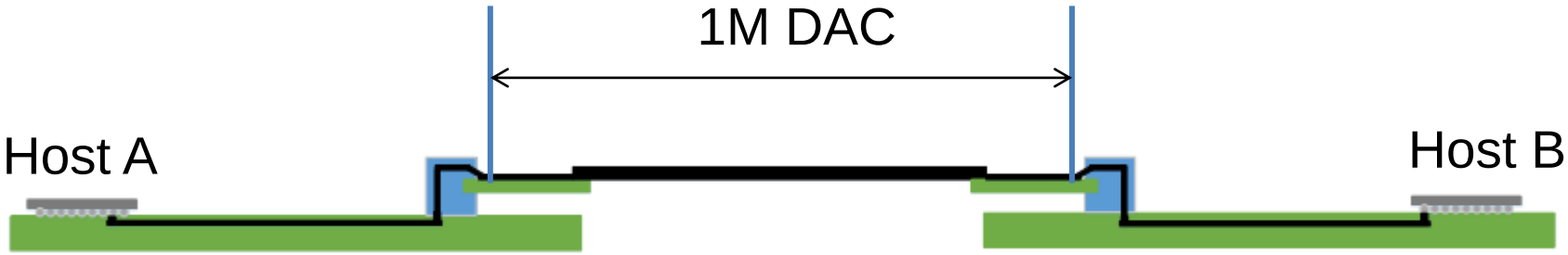
Background and Introduction (I)

- An important use case of 212.5 Gbps-PAM4 is the cable reach (CR) with a 1 Meter DAC.



- We have created a CR channel Design C to support 1 Meter DAC.

Background and Introduction (II)

- We leveraged our established/validated CR/LR simulation/modeling tool-flow-methodology (TFM) (e.g., [1]. [2]), updated reference package ([3]), and reference TX, RX to provide link simulation and analysis with this newly created CR/LR channel Design C.

Preliminary 212.5Gbps PAM4 CR end-to-end COM Analysis

- Proposed CR end-to-end COM configuration
  - DER: 10^{-4}
  - Reference TX
    - Output amplitude (A_v/A_fe/A_ne): 0.413/0.413/0.608
    - RLM = 0.95, SNR_{TX}=33dB, A_DD = 0.02UI_{pk}, RJ = 0.01UI_{RMS}
    - 20%-80% Rise/Fall Time (*T_r*): 4ps
    - TX FIR: 4-pre-, 1-post taps
    - TX Die: (see [1],[2])
    - Termination impedance (R_d): 46.25 ohms
    - TX Package:
      - Z_p = 33mm, Z_{p2} = 1.8mm
      - γ_0, a_1, a_2 *are updated (see [3])*
  - Reference Receiver
    - RX Die: Same as TX die
    - Termination impedance (R_d): 46.25 ohms
    - RX Package:
      - Same as TX, Z_p = 31mm
    - Noise Filter BW *(f_r)* = 0.5 * fb
    - RX EQ
      - CTLE: 2x Scaled from 802.3ck
      - RX FFE: Fixed: 6 pre- + 24 post-taps
      - Floating DFE Taps: 4 groups of 5 consecutive floating taps up to 60 UI
      - RX MLSD: 1 tap, b_{max} = 0.85
    - eta_0: 5x10^{-9} V^2/GHz

212.5G CR end-to-end COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ; 0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[.13 .15 .14; .13 .15 .14]	nH	[TX RX]
C_b	[0.3e-4, 0.3e-4]	nF	[TX RX]
z_p select	[2]		[test cases to run]
z_p (TX)	[12 33; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 33; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 31; 1.8 1.8]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
AC_CM_RMS	0	V	[test cases]
L	4		
M	32		
filter and Eq			
f_r	0.5	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.16]		[min:step:max]
c(-3)	[-0.1:0.02: 0]		[min:step:max]
c(-4)	[0:0.02:0.1]		[min:step:max]
c(-5)	0		[min:step:max]
c(-6)	0		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		
b_min(1)	0.3		
b_min(2..N_b)	[-0.3 -0.2*ones(1,22)]		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
MLSE	1		
ffe_pre_tap_len	6		
ffe_post_tap_len	24		
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	8	dB
DER_0	0.0001	
T_r	0.004	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	5.00E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0.0005 0.00089 0.0002]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	5	taps per group
N_f	60	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	50	(UI) start of tail taps limit
ICN & FOM_ILD parameters		
f_v	0.556	*Fb
f_f	0.556	*Fb
f_n	0.556	*Fb
f_2	80.000	GHz
A_ft	0.600	V
A_nt	**0.600**	V

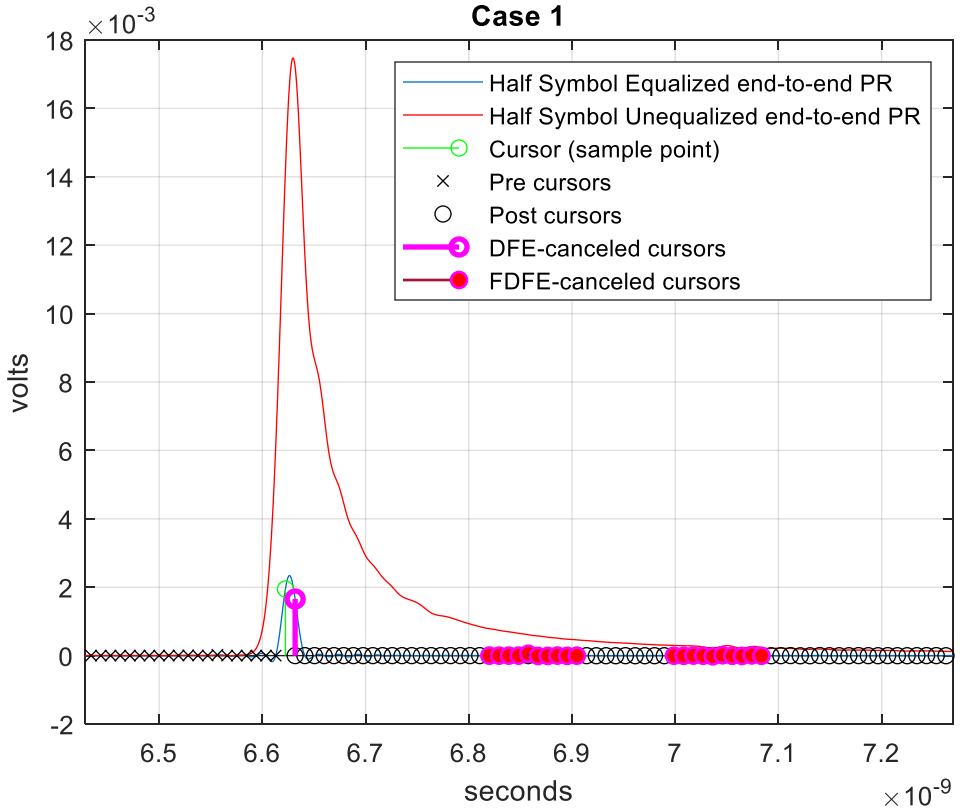
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

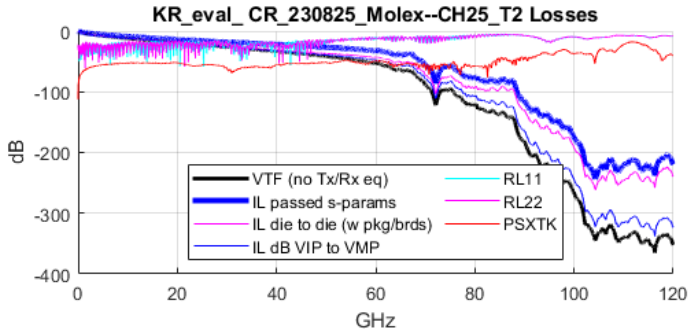
Notes:

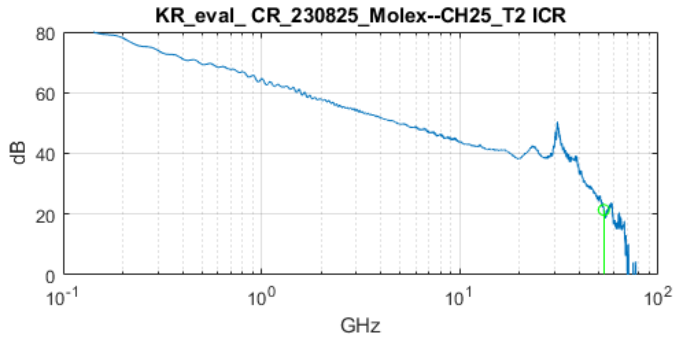
- ***COM v4.0 was used in this study.***

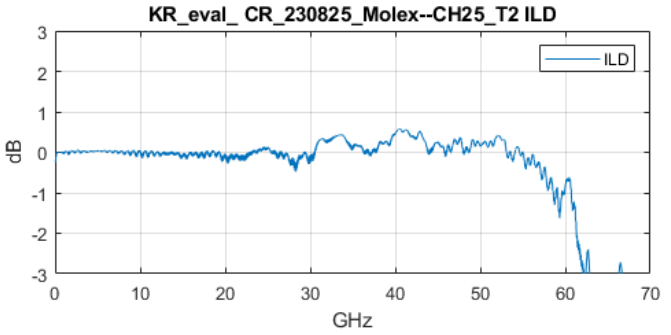
Preliminary 212.5Gbps PAM4 CR end-to-end COM Analysis

CH25

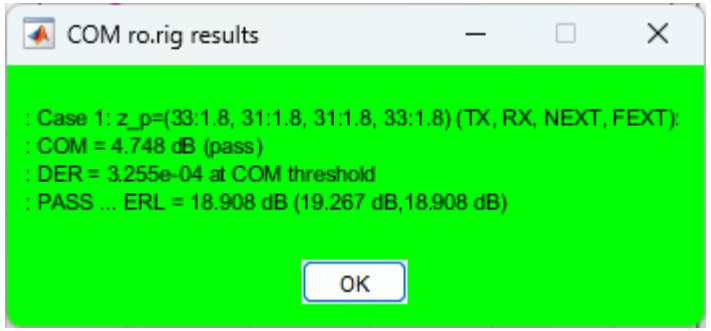








- 2x FEXT + 1 x NEXT
- EQ Taps = FFE(6+M+24) + DFE Float(4x5)
- COM = 4.75 dB
- DER = 1e-4



Conclusion

- This 40 dB (bump-to-bump) CR channel (Design C) can be supported with a COM 4.75 dB, at a DER of 1e-4, with the newly developed ref TX, RX, and PKG
- The newly developed ref TX, RX have the following key characteristics/capabilities:
  - TX FIR: 4-pre-, 1-post taps
  - RX FFE fixed: 6 pre- + 24 post-taps
  - RX DFE floating: 4 groups of 5 consecutive floating taps up to 60 UI
  - RX MLSD: 1 tap, bmax = 0.85

References

[1] https://www.ieee802.org/3/dj/public/23_05/li_3dj_08a_2305.pdf

[2] https://www.ieee802.org/3/dj/public/23_05/li_3dj_10a_2305.pdf

[3] https://www.ieee802.org/3/dj/public/23_0720/lim_3dj_02a_2307.pdf