

Considerations on COM Reference Model

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IEEE P802.3dj Task Force

September, 2023

Outline

- **D** Background and Introduction
- **COM Reference Model**
- **D** Reference CDR
- **G** Floating DFE & FFE
- **D** Summary

Background and Introduction

- Directions of reference receiver taken at the July 2023 Plenary meeting
 - Strong support of directions of RxFFE changes to Annex 93A and RxFFE based reference RX for 200G/lane AUIs, see straw poll #1 & #9, motions_3cwdfdj_2307
 - Various contributions look at different reference receiver architectures
- COM reference model discussion
 - MM + sample sweep CDR introduced in <u>mellitz_3dj_01a_elec_230817</u>
 - Floating-tap DFE/FFE compared in <u>lit_3dj_elec_01a_230817</u>, highly reflective channels showed significant dCOM
- This presentation provides COM analysis and comparison of reference CDR and floating-tap implementation
 - The intention is to advocate adopting a simple and general COM reference model for baseline exploratory and expanding MLSE features
 - NOT a specific baseline receiver proposal

COM Reference Model Proposed in mellitz_3dj_01a_2307

- COM 4.1 functionalities
 - Reference CDR: Mueller-Muller (MM)/sample sweep
 - Floating tap equalization: DFE only



Experimental COM Reference Model

- Experimental COM functionalities for comparison
 - Reference CDR: MM/sample sweep
 - Floating tap equalization: DFE, FFE

- Experimental functions used in this presentation
- NOT supported by COM 4.1



Reference CDR

Reference CDR

- Platform: COM 4.1
- Selected* CR/KR/C2M/C2C channels listed in appendix
- Reference CDR
 - <u>CR/KR/C2M/C2C</u> spreadsheets listed in appendix, except

CDR	ts_anchor	phase_adjustment
ММ	0	[0 0]
Sample sweep**	1	[-16 16]

** See <u>mellitz_3dj_01a_elec_230817</u> for details



- Sample sweep is implementation-specific, performance gain relates to the shapes of
 - 1. Channel response
 - 2. RX front-end response
- This function is time-consuming, simulation takes >1day (>10x run time) for a single channel

Floating Tap Equalization

COM Reference Model – Floating Tap Implementation

- Key change in this presentation: Move the floating taps from DFE to FFE function
- No change to the algorithms for determining FFE coefficients and floating tap locations



Reference Parameter Highlights

- Platform: COM 4.1
- Test channels: all CR/KR/C2M/C2C channels listed in appendix
 - Include new C2M channels and CR/KR channels, as compared to lit_3dj_elec_01a_230817
- Exploratory of reference RX architecture
 - <u>CR/KR/C2M/C2C</u> spreadsheets listed in appendix, except

			COM	4.1	Experiment funct	ion
		Parameter	FFE-Fix + DFE-Float	FFE-Fix	FFE-Fix + FFE-Float	
Fixed Tap -	DFE Fixed Tap	N_b	1	1	1	
	FFF Fixed Ter	ffe_pre_tap_len	4	4	4	
	FFE FIXED Tap	ffe_post_tap_len	24	60	24	
	DFE Floating Tap	N_bg	4***	0	0	
		N_bf	5***	-	-	
-1		N_f	60	-	-	
Floating Tap		ffe_flt_tap_N_bg	NA	NA	4***	Groups
	FFE Floating Tap	ffe_flt_tap_N_bf	NA	NA	5***	Taps per groups
		ffe flt tap N f	NA	NA	60	UI span

Experimental parameters for floating FFE taps, not implemented in COM4.1

*** Changes to lit_3dj_elec_01a_230817

Considerations of FFE-based Receiver

• Receiver architectures for comparison

Option I	1 fixed DFE tap + 24 fixed FFE tap + 20 floating DFE tap
Option II	1 fixed DFE tap + 60 fixed FFE tap
Option III	1 fixed DFE tap + 24 fixed FFE tap + 20 floating FFE tap

- FFE acts through convolution rather than subtraction
 - ISI located beyond EQ coverage may be enhanced
 - Accumulative residual ISI (power sum of equalized pulse response) of a selected channel





Considerations of FFE-based Receiver

- Highly reflective channels show significant dCOM
 - Use long FFE fixed-tap to handle far-end reflections is not reasonable, FFE taps are not cheap
 - Difference between floating DFE and FFE taps will change the pass/fail for reflective channels

Option I	1 fixed DFE tap + 24 fixed FFE tap + 20 floating DFE tap
Option II	1 fixed DFE tap + 60 fixed FFE tap
Option III	1 fixed DFE tap + 24 fixed FFE tap + 20 floating FFE tap





- This presentation continued discussions in the Task Force on COM reference model
 - Reference CDR: MM/sample sweep
 - Floating-tap implementation: DFE/FFE
- Provided a relative comparison for consensus discussion in order to focus baseline proposal development efforts
 - Choice of reference models yields different performance and can change the pass/fail for some channels
 - Reference model should address a reasonable minimal implementation
- Straw Polls requested to TF leadership on the
 - Direction of COM reference CDR
 - Direction of floating-tap implementation in COM



Channel List



Application	Contribution	Application	Contribution		
	rabinovich_3df_01_2209*		shanbhag_3dj_01_2305*		
	rabinovich_3df_02_2209	CD	kocsis_3dj_02_2305*		
	rabinovich_3dj_02_230116*	CR	lim_3dj_03_230629*		
	rabinovich_3dj_03_230116		lim_3dj_04_230629*		
	shanbhag_3dj_03_2305*		mellitz_3dj_02_elec_230504*		
C214	akinwale_3dj_02_2307	KD	weaver_3dj_02_2305		
CZIVI	akinwale_3dj_03_2307* [1 5 9 11] in	KK	shanbhag_3dj_02_2305*		
	akinwale_3dj_04_2307		weaver_3dj_elec_01_230622*		
	lim_3dj_01_230629*				
	lim_3dj_02_230629*		* Selected channels for reference CDR simulatior		
	weaver_3dj_elec_02_230831 (TP0-TP1)*[High Temp]				
	kareti_3dj_02_2309*				
C2C	mellitz 3di elec 01 230504*				

Example COM Configuration for 200Gbps/Lane CR/KR

Table 93A-1 parameters				I/O control				Table 93A-3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical		Parameter	Setting	Units
fb	106.25	GBd		DISPLAY WINDOW	0	logical		package ti gamma0 a1 a2	10 0.0008455 0.0003402251	
 f min	0.05	GHz		CSV REPORT	0	logical		package ti tau	0.00644805	ns/mm
Delta f	0.01	GHz		RESULT DIR	\results\CAKR {date}			package Z c	[92 92 : 70 70: 80 80: 100 100]	Ohm
Cd	[0.4e-4 0.9e-4 1.1e-4:0.4e-4 0.9e-4 1.1e-4]	nF	ITX RX1	SAVE FIGURES	0	logical		P	,	
15	[0.130.150.14:0.130.150.14]	nH	ITX RX1	Port Order	[1324]			Parameter	Setting	
Ch	[0.3e.4.0.3e.4.]	nE	[TX RX]	RUNTAG	CAKE BCos eval			board ti gamma0 a1 a2	10.6.44084e-4.3.6036e-051	1.5 db/in @ 56G
z n select	[12]		[test cases to run]	COM CONTRIBUTION	0	logical		board ti tau	5.790E-03	ns/mm
7 p (TX)	[12 31 1 1 1 1 0 5 0 5]	mm	[test cases]	Operational	5			board 7 c	100	Ohm
z p (NEXT)	[12 29:11:11:0.50.5]	mm	[test cases]	FRI Pass threshold	9.7	dB		z hn (TX)	125	mm
z_p (FEXT)	[1231:11:11:0505]	mm	[test cases]	COM Pass threshold	3	db		z bp (NEXT)	0	mm
7 p (BX)	[12 29:11:11:0505]	mm	[test cases]	DER 0	1.00F-04			z hp (FEXT)	125	mm
PKG Tx FFE preset	0		[rest cuses]	Tr	4.00E-03	ns		z_bp (BX)	0	mm
Cn	10 5e.4 0 5e.41	nF	ITX RX1	FORCE TR	1	logical		C 0	10 20-4 01	nF
P	50	Ohm	[Intiot]	PMD type	C2C	rogrean		C1	[0.2e + 0]	nF
R_0	[50 50]	Ohm	ITX RX1	FW	1		-	Include PCB	0	logical
Av	0.413	V	vn/d=	TDP and FPL ontions	-	logical		include Feb	· · ·	logical
 	0.413	v	vp/vi-	 TOP		logical				
A. no.	0.415	v	vp/vi-	 IDK EDI	1	logical		Seletions (rectangle, gaussian dual, rayleigh triangle		
	6.45			ERL	1	logical	-	Histogram Window Weight	mussion	coloction
M	22			TR TOR	0.01	115	-	Histogram_window_weight	gaussian	selection
filter and Eq.	52			IN_IDK	3500	logical	-	4	0.02	01
f.r.	0.75	*fb		 TDP Puttopworth	3300	logical	-			
-(0)	0.75	10	min	http://worth	1			ICN parameters		
c(0)	0.34		[minutonumaw]	Deta_X	0.619			f v	0.594	Eb
-(2)	[0: 02:0 12]		[min:step:max]		0.010	111	-	1_V f f	0.574	FD
c(-2)	[0.02:0:12]		[min:step:max]	 N by	0			fn	0.574	Eb
C(-3)	[0: 02:0 02]		[min:step:max]	 IN_DX fixture delay/time	[0.0.1		-	<u>[]</u>	79.699	FD CHr
c(-+)	[0.1:0.02:0.02]		[min:step:max]	 Tukey Window	1		-	1_2 A #	0.450	
N b	1		[mm.step.max]	 Noise litter	1		-	Ant	0.450	v
h max(1)	0.85	01	Ac/dffo1	 ridise, jittei	0.01	111	-	<u></u>	0.450	· · ·
h max(2 N h)	(0.2.0.3tener(1.22))		As/dio2_N_h	 signia_io	0.01		-	Electing Tap Control		
b_min(1)	[0.3 0.2 offes(1,22)]		As/dffo1	 A_DD	E 00E 09	VA2/CH-	-	N hg	4	0.1.2 or 2 groups
h min(2 N h)	(0.2.0.2tener(1.22))		As/die2 N h	 eta_0	33002-07	40	-	N bf		tens per groups
a DC	[12:1:0]	dB	[minutonimax]	 P IM	0.95	ub		N É	60	LII span for floating tans
<u>g_</u> DC	[-13.1.0] 43 E	CH-	[mm.step.max]	K_LIVI -	0.75			hmaya	0.3	max DEE value for floating taps
1_2	42.5	CHa		Federate Councilla		-	-	billang	0.2	max bite value for noacing caps
1_p1	106.25	CH ₂		Enforce causality	trend to DC		-	MCC	1	logical
	100.25	GHZ	[minut enum mi]	5-parameter magnitude extrapolation policy	trend_to_bc	-		MILSE		logical
g_DC_HP f UD_D7	[-0.1.0]	CHa	[mm.step:max]	Ciltor: DyECF			-	Deceiver testing		
Dutterunath	1.328125	Invial	include in fe	filter, RAFFE	4			PX CALIDRATION	0	Indian
Butterworth Raised Cosine	1	logical	include in fr	fie_pre_tap_ien				Sigma BBN stop	E 00E 03	logical
Raised_Cosilie	6 705:10	logical	mclude in n	fie_post_tap_ten	24	0		sigilia BBN scep	5.00E-03	*
RC_Start	0.70E+10	nz	start freq for RCos	ne_tap_step_size	07					
KC_end	7.97E+10	HZ	end freq for KCos	me_main_cursor_min	0.7					
annals adjustes ant	10.01	abase		me_pre_tap1_max	0.7		-			
sample_adjustment	[00]	pnase		 me_post_tap1_max	0.7		-			
ts_anchor	U			 rre_tapn_max	0.7					
				 rie_backoff	0	012-2				
				 rre_rit_tap_N_bg	0	012 or 3	groups			
				 fe_ft_tap_N_bf	5	taps per g	oup			
				 TTE_TIT_TAP_IN_I	00	u spari to	noating ta	ihz		
		-		 ne_aig_opt	0	logical				

Example COM Configuration for 200Gbps/Lane C2M

Table 93A-1 parameters				 I/O control		1		Table 93A-3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical	1	Parameter	Setting	Units
f_b	106.25	GBd		DISPLAY_WINDOW	0	logical		package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
f min	0.05	GHz		CSV REPORT	0	logical	1	package ti tau	0.00644805	ns/mm
Delta f	0.01	GHz		RESULT DIR	.\results\CAKR {date}\	-		package Z c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]	SAVE_FIGURES	0	logical				
Ls	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]	Port Order	[1324]	-	1	Parameter	Setting	
Cb	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	CAKR_RCos_eval_			board ti gamma0 a1 a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G
z_p select	[12]		[test cases to run]	COM CONTRIBUTION	0	logical		board_tl_tau	5.790E-03	ns/mm
z_p (TX)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]	Operational		_		board_Z_c	100	Ohm
z_p (NEXT)	[888;000;000;000]	mm	[test cases]	ERL Pass threshold	9.7	dB		z_bp (TX)	125	mm
z_p (FEXT)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]	COM Pass threshold	3	db		z_bp (NEXT)	0	mm
z_p (RX)	[888;000;000;000]	mm	[test cases]	DER_0	1.33E-05			z_bp (FEXT)	125	mm
PKG_Tx_FFE_preset	0			Tjr	4.00E-03	ns		z_bp (RX)	0	mm
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]	FORCE_TR	1	logical		C_0	[0.2e-4 0]	nF
R_0	50	Ohm		PMD_type	C2C			C_1	[0.2e-4 0]	nF
R_d	[50 50]	Ohm	[TX RX]	EW	1			Include PCB	0	logical
A_v	0.413	V	vp/vf=	TDR and ERL options		logical	1			-
A_fe	0.413	V	vp/vf=	TDR	1	logical				
A_ne	0.45	V		ERL	1	logical		Seletions (rectangle, gaussian, dual_rayleigh, triangle		
L	4			ERL_ONLY	0	ns		Histogram_Window_Weight	gaussian	selection
M	32			TR_TDR	0.01			Qr	0.02	UI
filter and Eq				N	2000	logical				
f_r •	0.75	*fb		TDR_Butterworth	1					
c(0)	0.54		min	beta_x	0			ICN parameters		
c(-1)	[-0.4:0.02:0]		[min:step:max]	rho_x	0.618			f_v	0.594	Fb
c(-2)	[0:.02:0.2]		[min:step:max]	TDR_W_TXPKG	0	UI		ff	0.594	Fb
c(-3)	[-0.04:.02:0]		[min:step:max]	N_bx	0			f_n	0.594	Fb
c(-4)	[0:.02:0.02]		[min:step:max]	fixture delay time	[00]			f_2	79.688	GHz
c(1)	[-0.12:0.02:0.04]		[min:step:max]	Tukey_Window	1			A_ft	0.450	V
N_b	1	UI		Noise, jitter				A_nt	0.450	V
b_max(1)	0.85		As/dffe1	sigma_RJ	0.01	UI				
b_max(2N_b)	[0.3 0.2*ones(1,22)]		As/dfe2N_b	A_DD	0.02	UI		Floating Tap Control		
b_min(1)	0		As/dffe1	eta_0	1.25E-08	V^2/GHz		N_bg	4	0 1 2 or 3 groups
b_min(2N_b) 🗧	[-0.2 -0.2*ones(1,22)]		As/dfe2N_b	SNR_TX	33	dB		N_bf	5	taps per group
g_DC	[-20:1:0]	dB	[min:step:max]	R_LM	0.95			N_f	60	UI span for floating taps
f_z	42.5	GHz						bmaxg	0.2	max DFE value for floating taps
f_p1 🗧	42.5	GHz		Enforce Causality	1					
f_p2	106.25	GHz		S-parameter magnitude extrapolation policy	trend_to_DC			MLSE	0	logical
g_DC_HP	[-6:1:0]		[min:step:max]							
f_HP_PZ	1.328125	GHz		Filter: RxFFE				Receiver testing		
Butterworth	1	logical	include in fr	ffe_pre_tap_len	4	UI		RX_CALIBRATION	0	logical
Raised_Cosine	0	logical	include in fr	ffe_post_tap_len	24	UI		Sigma BBN step	5.00E-03	v
RC_Start	6.70E+10	Hz	start freq for RCos	ffe_tap_step_size	0					
RC_end	7.97E+10	Hz	end freq for RCos	ffe_main_cursor_min	0.7					
				ffe_pre_tap1_max	0.7					
sample_adjustment	[0 0]	phase		ffe_post_tap1_max	0.7					
ts_anchor	0			ffe_tapn_max	0.7					
				ffe_backoff	0					
				ffe_flt_tap_N_bg	0	0 1 2 or 3	groups			
				ffe_flt_tap_N_bf	5	taps per gr	oup			
				ffe_flt_tap_N_f	60	UI span for	floating ta	aps		
				ffe_alg_opt	0	logical				





Example COM Configuration for 200Gbps/Lane C2C

Table 93A-1 parameters		1			I/O control			İ	Table 93A-3 parameters		
Parameter	Setting	Units	Information		DIAGNOSTICS	0	logical		Parameter	Setting	Units
fb	106.25	GBd			DISPLAY WINDOW	0	logical		package ti gamma0 a1 a2	[0 0.0008455 0.000340225]	
 f min	0.05	GHz			CSV REPORT	0	logical		package ti tau	0.00644805	ns/mm
Delta f	0.01	GHz			RESULT DIR	\results\CAKR {date}			package Z c	[92 92 : 70 70: 80 80: 100 100]	Ohm
Cd	[0.4e-4 0.9e-4 1.1e-4:0.4e-4 0.9e-4 1.1e-4]	nE	ITX RX1		SAVE FIGURES	0	logical		1 011		
Ls	[0.130.150.14:0.130.150.14]	nH	ITX RX1		Port Order	[1324]			Parameter	Setting	
Cb	[0.3e-4 0.3e-4]	nE	ITX RX1		RUNTAG	CAKR RCos eval			board ti gamma0 a1 a2	10.6.44084e-4.3.6036e-051	1.5 db/in @ 56G
z p select	[12]		[test cases to run]		COM CONTRIBUTION	0	logical		board ti tau	5.790E-03	ns/mm
z p (TX)	[13 31:11:11:0.5 0.5]	mm	[test cases]		Operational	-			board Z c	100	Ohm
z p (NEXT)	[11 29: 1 1: 1 1: 0.5 0.5]	mm	[test cases]		ERL Pass threshold	9.7	dB		z bp (TX)	125	mm
z p (FEXT)	[13 31:11:11:0.50.5]	mm	[test cases]		COM Pass threshold	3	db		z bp (NEXT)	0	mm
z p (RX)	[11 29: 1 1 : 1 1 : 0.5 0.5]	mm	[test cases]		DER 0	1.33E-05			z bp (FEXT)	125	mm
PKG Tx FFE preset	0		()		Tr	4.00E-03	ns		z bp (RX)	0	mm
C n	[0.5e-4 0.5e-4]	nE	ITX RX1		FORCE TR	1	logical		C Q	[0.2e-4.0]	nE
R O	50	Ohm	[]		PMD type	C2C			C 1	[0.2e-4 0]	nF
R d	[50 50]	Ohm	ITX RX1		FW	1			Include PCB	0	ogica
Av	0.413	V	vp/vf=		TDR and ERL options	-	logical	-		-	
A fe	0.413	v	vp/vf=		TDR	1	logical				
A ne	0.45	V			FRI	1	logical		Seletions (rectangle, gaussian, dual, rayleigh, triangle		
ī	4				ERL ONLY	0	ns		Histogram Window Weight	gaussian	selection
M	32				TR TDR	0.01			Or	0.02	UI
filter and Eq					N	2000	logical				
fr.	0.75	۴ß			TDR Butterworth	1					
c(0)	0.54		min		beta x	0			ICN parameters		
c(-1)	[-0.4:0.02:0]		[min:step:max]		rho x	0.618			fv	0.594	Fb
c(-2)	[0:.02:0.2]		[min:step:max]		TDR W TXPKG	0	UI		ff	0.594	Fb
c(-3)	[-0.04:.02:0]		[min:step:max]		N bx	0			fn	0.594	Fb
c(-4)	[0:.02:0.02]		[min:step:max]		fixture delay time	[00]			f 2	79.688	GHz
c(1)	[-0.12:0.02:0.04]		[min:step:max]		Tukey Window	1			Aft	0.450	v
N_b	1	UI			Noise, jitter				A_nt	0.450	V
b_max(1)	0.85		As/dffe1		sigma_RJ	0.01	UI				
b_max(2N_b)	[0.3 0.2*ones(1,22)]		As/dfe2N_b	1	A_DD ·	0.02	UI		Floating Tap Control		
b_min(1)	0		As/dffe1		eta_0	1.25E-08	V^2/GHz		N_bg	4	0 1 2 or 3 groups
b min(2N b)	[-0.2 -0.2*ones(1,22)]		As/dfe2N b	l l	SNR TX	33	dB		N bf	5	taps per group
g_DC	[-20:1:0]	dB	[min:step:max]		R_LM	0.95			N_f	60	UI span for floating taps
f_z I	42.5	GHz							bmaxg	0.2	max DFE value for floating taps
f_p1	42.5	GHz			Enforce Causality	1					
f_p2	106.25	GHz			S-parameter magnitude extrapolation policy	trend_to_DC			MLSE	0	logical
g_DC_HP	[-6:1:0]		[min:step:max]								
f_HP_PZ	1.328125	GHz			Filter: RxFFE				Receiver testing		
Butterworth	1	logical	include in fr		ffe_pre_tap_len	4	UI		RX_CALIBRATION	0	logical
Raised_Cosine	0	logical	include in fr		ffe_post_tap_len	24	UI		Sigma BBN step	5.00E-03	V
RC_Start	6.70E+10	Hz	start freq for RCos		ffe_tap_step_size	0					
RC_end	7.97E+10	Hz	end freq for RCos		ffe_main_cursor_min	0.7					
					ffe_pre_tap1_max	0.7					
sample_adjustment	[0 0]	phase			ffe_post_tap1_max	0.7					
ts_anchor	0				ffe_tapn_max	0.7					
					ffe_backoff	0					
					ffe_flt_tap_N_bg	0	0 1 2 or 3	groups			
					ffe_flt_tap_N_bf	5	taps per g	oup			
					ffe_flt_tap_N_f	60	UI span fo	floating ta	ps		
					ffe_alg_opt	0	logical				
1											

Thank you Questions and Discussions