Considerations on COM Reference Model

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IEEE P802.3dj Task Force

September, 2023

Outline

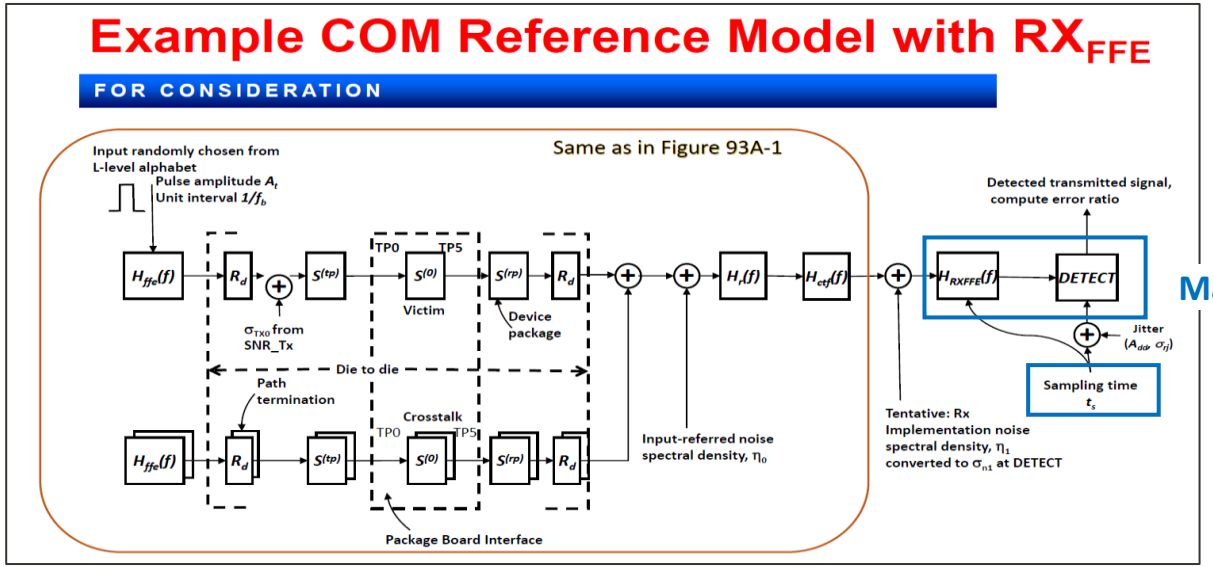
- Background and Introduction
- COM Reference Model
- Reference CDR
- Floating DFE & FFE
- Summary

Background and Introduction

- Directions of reference receiver taken at the July 2023 Plenary meeting
  - Strong support of directions of RxFFE changes to Annex 93A and RxFFE based reference RX for 200G/lane AUIs, see straw poll #1 & #9, motions_3cwdfdj_2307
  - Various contributions look at different reference receiver architectures
- COM reference model discussion
  - MM + sample sweep CDR introduced in mellitz_3dj_01a_elec_230817
  - Floating-tap DFE/FFE compared in lit_3dj_elec_01a_230817, highly reflective channels showed significant dCOM
- This presentation provides COM analysis and comparison of reference CDR and floating-tap implementation
  - The intention is to advocate adopting a simple and general COM reference model for baseline exploratory and expanding MLSE features
  - NOT a specific baseline receiver proposal

COM Reference Model Proposed in mellitz_3dj_01a_2307

- **COM 4.1 functionalities**
  - Reference CDR: Mueller-Muller (MM)/sample sweep
  - Floating tap equalization: DFE only

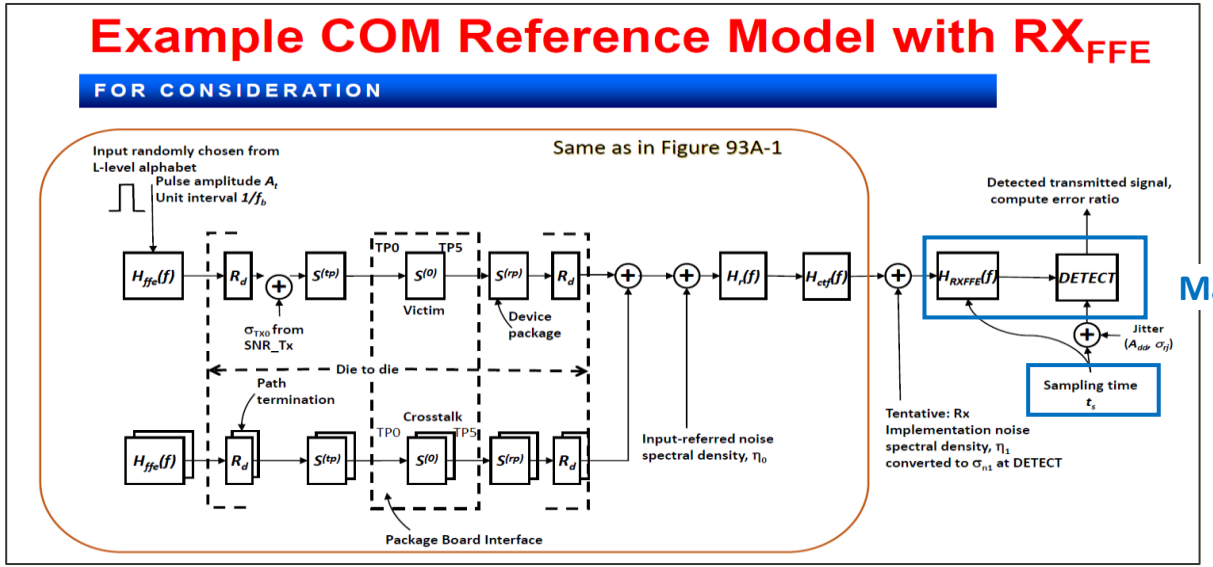


Main focus of this presentation

Experimental COM Reference Model

- **Experimental COM functionalities for comparison**
  - **Reference CDR: MM/sample sweep**
  - **Floating tap equalization: DFE, FFE**

- *Experimental functions used in this presentation*
- *NOT supported by COM 4.1*



Main focus of this presentation

Reference CDR

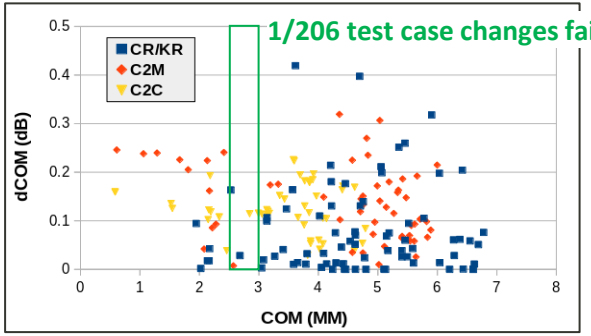
Reference CDR

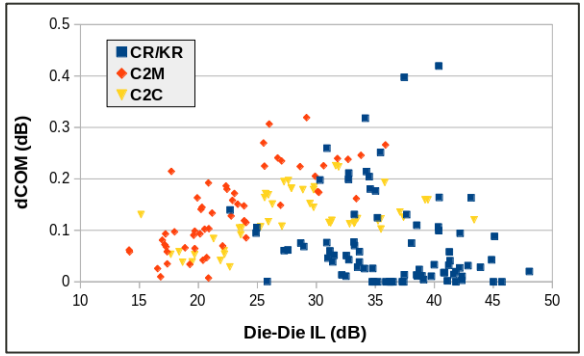
- Platform: COM 4.1
- Selected* CR/KR/C2M/C2C channels listed in appendix
- Reference CDR
  - CR/KR/C2M/C2C spreadsheets listed in appendix, except

CDR	ts_anchor	phase_adjustment
MM	0	[0 0]
Sample sweep**	1	[-16 16]

** *See mellitz_3dj_01a_elec_230817 for details*

COM (Sample Sweep) – COM (MM)



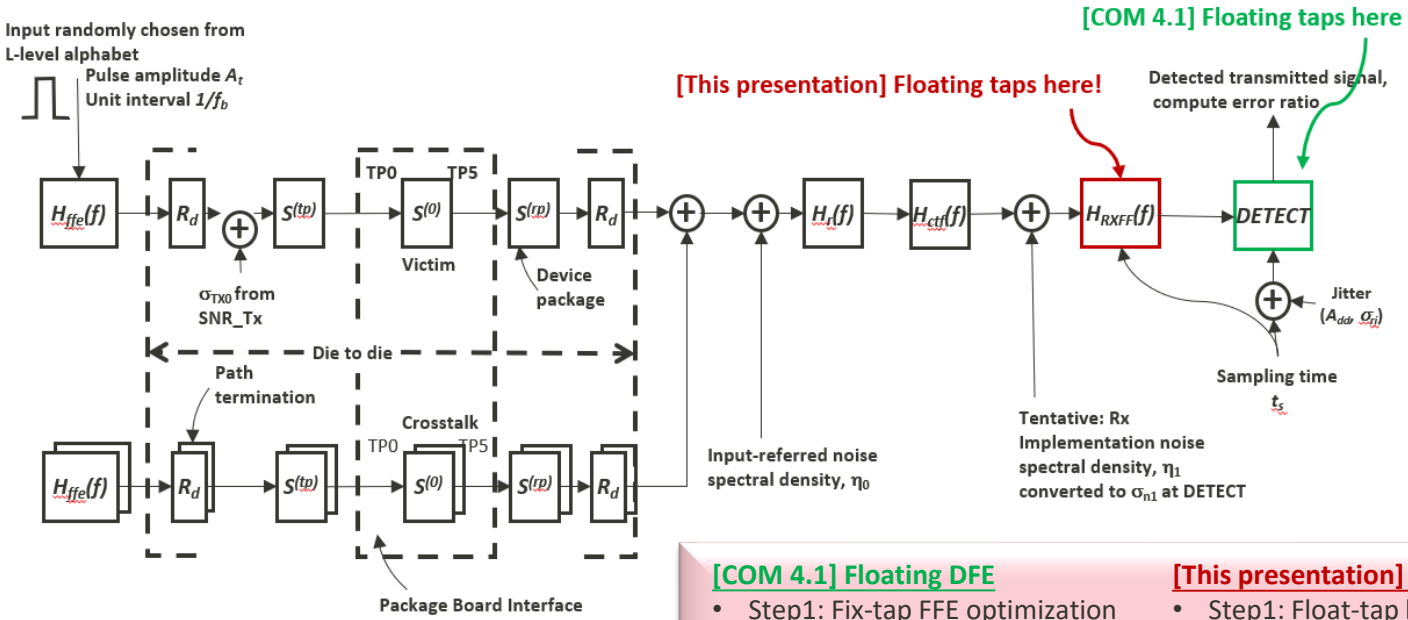


- Sample sweep is implementation-specific, performance gain relates to the shapes of
  1. Channel response
  2. RX front-end response
- This function is time-consuming, simulation takes >1day (>10x run time) for a single channel

Floating Tap Equalization

COM Reference Model – Floating Tap Implementation

- Key change in this presentation: Move the floating taps from DFE to FFE function
- No change to the algorithms for determining FFE coefficients and floating tap locations



[COM 4.1] Floating DFE

- Step1: Fix-tap FFE optimization
- Step2: Float-tap location search
- Step3: DFE

[This presentation] Floating FFE

- Step1: Float-tap location search
- Step2: Fix- & float-tap FFE optimization
- Step3: DFE

Reference Parameter Highlights

- **Platform: COM 4.1**
- **Test channels: all CR/KR/C2M/C2C channels listed in appendix**
  - **Include new C2M channels and CR/KR channels, as compared to lit_3dj_elec_01a_230817**
- **Exploratory of reference RX architecture**
  - **CR/KR/C2M/C2C spreadsheets listed in appendix, except**

		Parameter	COM 4.1 FFE-Fix + DFE-Float	COM 4.1 FFE-Fix	Experiment function FFE-Fix + FFE-Float	
Fixed Tap	DFE Fixed Tap	N_b	1	1	1	
	FFE Fixed Tap	ffe_pre_tap_len	4	4	4	
		ffe_post_tap_len	24	60	24	
Floating Tap	DFE Floating Tap	N_bg	4***	0	0	
		N_bf	5***	-	-	
		N_f	60	-	-	
	FFE Floating Tap	ffe_flt_tap_N_bg	NA	NA	4***	Groups
		ffe_flt_tap_N_bf	NA	NA	5***	Taps per groups
		ffe_flt_tap_N_f	NA	NA	60	UI span

Experimental parameters for floating FFE taps, not implemented in COM4.1

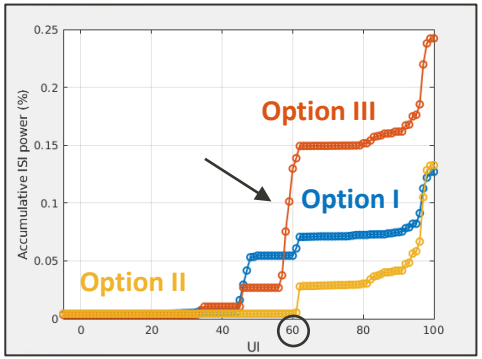
****** Changes to lit_3dj_elec_01a_230817***

Considerations of FFE-based Receiver

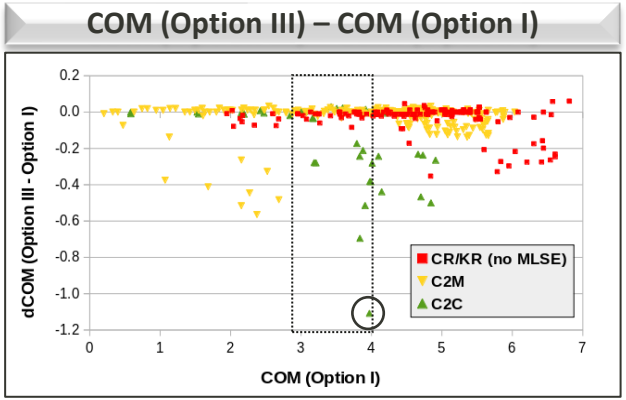
- Receiver architectures for comparison

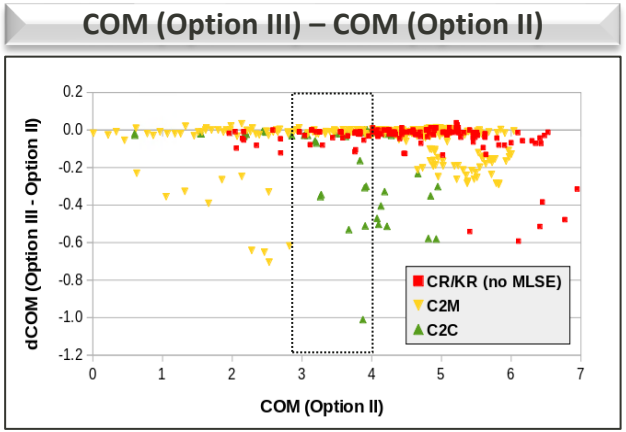
Option I	1 fixed DFE tap + 24 fixed FFE tap + 20 floating DFE tap
Option II	1 fixed DFE tap + 60 fixed FFE tap
Option III	1 fixed DFE tap + 24 fixed FFE tap + 20 floating FFE tap

- FFE acts through convolution rather than subtraction
  - ISI located beyond EQ coverage may be enhanced
  - Accumulative residual ISI (power sum of equalized pulse response) of a selected channel



EQ span



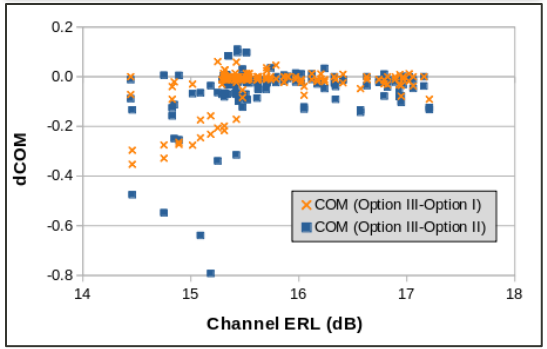


Considerations of FFE-based Receiver

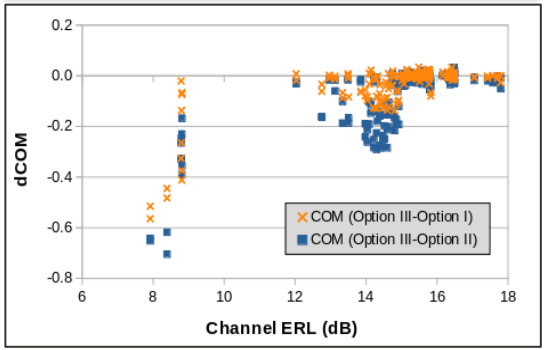
- **Highly reflective channels show significant dCOM**
  - **Use long FFE fixed-tap to handle far-end reflections is not reasonable, FFE taps are not cheap**
  - **Difference between floating DFE and FFE taps will change the pass/fail for reflective channels**

Option I	1 fixed DFE tap + 24 fixed FFE tap + 20 floating DFE tap
Option II	1 fixed DFE tap + 60 fixed FFE tap
Option III	1 fixed DFE tap + 24 fixed FFE tap + 20 floating FFE tap

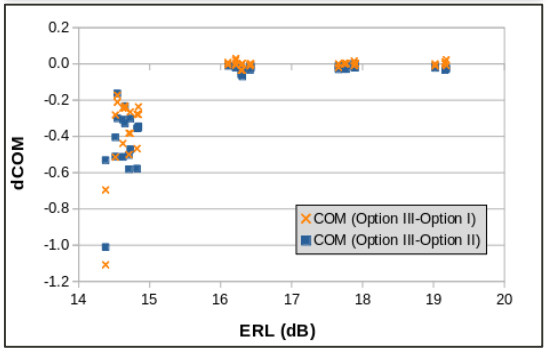
CR/KR



C2M



C2C



Summary

- This presentation continued discussions in the Task Force on COM reference model
  - Reference CDR: MM/sample sweep
  - Floating-tap implementation: DFE/FFE
- Provided a relative comparison for consensus discussion in order to focus baseline proposal development efforts
  - Choice of reference models yields different performance and can change the pass/fail for some channels
  - Reference model should address a reasonable minimal implementation
- Straw Polls requested to TF leadership on the
  - Direction of COM reference CDR
  - Direction of floating-tap implementation in COM

Appendix

Channel List

Application	Contribution
C2M	rabinovich_3df_01_2209*
	rabinovich_3df_02_2209
	rabinovich_3dj_02_230116*
	rabinovich_3dj_03_230116
	shanbhag_3dj_03_2305*
	akinwale_3dj_02_2307
	akinwale_3dj_03_2307*[1 5 9 11] in
	akinwale_3dj_04_2307
	lim_3dj_01_230629*
	lim_3dj_02_230629*
	weaver_3dj_elec_02_230831 (TP0-TP1)*[High Temp]
	kareti_3dj_02_2309*
C2C	mellitz_3dj_elec_01_230504*

Application	Contribution
CR	shanbhag_3dj_01_2305*
	kocsis_3dj_02_2305*
	lim_3dj_03_230629*
	lim_3dj_04_230629*
KR	mellitz_3dj_02_elec_230504*
	weaver_3dj_02_2305
	shanbhag_3dj_02_2305*
	weaver_3dj_elec_01_230622*

** Selected channels for reference CDR simulation*

Example COM Configuration for 200Gbps/Lane CR/KR

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[12 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[12 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (RX)	[12 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.12]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.1:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-13:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos
sample_adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval_	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.00E-04	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	3500	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	5.00E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
Enforce Causality	1	
S-parameter magnitude extrapolation policy	trend_to_DC	
Filter: RxFFE		
ffe_pre_tap_len	4	UI
ffe_post_tap_len	24	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	
ffe_flt_tap_N_bg	0	0 1 2 or 3 groups
ffe_flt_tap_N_bf	5	taps per group
ffe_flt_tap_N_f	60	UI span for floating taps
ffe_alg_opt	0	logical

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	*0*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI
ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	5	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
MLSE	1	logical
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Example COM Configuration for 200Gbps/Lane C2M

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[8 8 8; 0 0 0; 0 0 0 ; 0 0 0]	mm	[test cases]
z_p (FEXT)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 8 8; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos
sample_adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval_	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.25E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
Enforce Causality	1	
S-parameter magnitude extrapolation policy	trend_to_DC	
Filter: RxFFE		
ffe_pre_tap_len	4	UI
ffe_post_tap_len	24	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	
ffe_flt_tap_N_bg	0	0 1 2 or 3 groups
ffe_flt_tap_N_bf	5	taps per group
ffe_flt_tap_N_f	60	UI span for floating taps
ffe_alg_opt	0	logical

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	*0*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI
ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	5	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
MLSE	0	logical
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Example COM Configuration for 200Gbps/Lane C2C

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (RX)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos
sample_adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval_	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.25E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	
Enforce Causality	1	
S-parameter magnitude extrapolation policy	trend_to_DC	
Filter: RxFFE		
ffe_pre_tap_len	4	UI
ffe_post_tap_len	24	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	
ffe_flt_tap_N_bg	0	0 1 2 or 3 groups
ffe_flt_tap_N_bf	5	taps per group
ffe_flt_tap_N_f	60	UI span for floating taps
ffe_alg_opt	0	logical

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	*0*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI
ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	5	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
MLSE	0	logical
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Thank you

Questions and Discussions