IEEE P802.3dj Package Status Update & Next Steps

Kent Lusted, Intel
Liav Ben-Artsi, Marvell
Matt Brown, Alphawave Semi
Ali Ghiasi, Ghiasi Quantum / Marvell
Adam Healey, Broadcom
Mike Li, Intel
Rich Mellitz, Samtec
Adee Ran, Cisco

1p0

Supporters and Contributions

Supporters

- Jim Weaver, Arista
- Rick Rabinovich, Keysight
- Jason Chan, Arista
- Howard Heck, Intel
- Tobey P.-R. Li, MediaTek

Problem Statement

- Device packages are projected to consume a considerably larger portion of the die-to-die loss budget at 200 Gbps/lane
- There still is no consensus on the loss allocation for device packages after ~1.5 years of contributions, discussions, debates, etc.
- Two different (opposing) approaches:
  - **Loss optimized**: Concerns that a channel loss budget based on worst-case allocations for package losses overly constrains system design
    - E.g. https://www.ieee802.org/3/dj/public/23_0720/lim_3dj_02a_2307.pdf
  - **Radix optimized**: Concerns that low allocations for package loss overly constrain package design
    - E.g. https://www.ieee802.org/3/dj/public/23_07/benartsi_3dj_02_2307.pdf
- The lack of consensus on the package is holding up the baseline proposal development of electrical interfaces

Proposed Path

- Define two classes of packages
  - Both the Class A “loss optimized” and Class B “radix optimized” approaches are supported
- Create two sets of transmitter and receiver specifications, one for each package class
  - TX Class A (common die model + Class A package)
  - TX Class B (common die model + Class B package)
  - RX Class A (common die model + Class A package)
  - RX Class B (common die model + Class B package)
  - Choose the reference package model that is applicable
- Package-to-Package (TP0-TP5) channel compliance using COM with a specific reference package on each end
- Apply to backplane PHYs, AUI C2C interfaces
  - Look at CR and C2M later

Transmitter and Receiver Compliance Direction

- Define multiple reference package models differentiated *at first order* by a maximum insertion loss allocation e.g., ...

Transmitter or receiver	Maximum package IL allocation [1], dB
Class A (e.g. “loss optimized”)	TBD = 6
Class B (e.g. “radix optimized”)	TBD = 9

[1] From TP0d to TP0 for transmitters and from TP5 to TP5d for receivers.

- All transmitters and receivers must meet Class B requirements. Some may meet Class A requirements.
- TX/RX compliance to Class A and/or Class B is demonstrated using existing compliance test methods with the reference package model that reflects the corresponding limit on insertion loss

Note: values in magenta are placeholders, not a baseline proposal

Some Future Work Items

- Test cases of different trace lengths for each package needs consideration
- A separate minimum package loss test case may also be included
- Package-to-package channel classification, if needed
- Parameters and values for Class A and Class B packages
- Consider package choices for CR and C2M interfaces

Example KR Channel Matrix (IL <= 40 dB die-die)

Example compliance test requirements

Reference package models for COM		KR Channel IL (ball-ball)
Transmitter	Receiver	
Class A (6 dB)	Class A (6 dB)	28 dB
Class A (6 dB)	Class B (9 dB)	25 dB
Class B (9 dB)	Class A (6 dB)	
Class B (9 dB)	Class B (9 dB)	22 dB

Co-design of channel with targeted package and vice versa

*C2C channel class loss will be adjusted after agreement on max bump-bump loss.

Example compatibility matrix

KR Channel IL (ball-ball)		Receiver class	
		Class A	Class B
Transmitter class	Class A	28, 25, 22 dB	25, 22 dB
	Class B	25, 22 dB	22 dB

Note: values in magenta are placeholders, not a baseline proposal

Summary

- To unblock progress towards baseline proposals on the electrical interfaces, we should go in the direction of:
  - Specifying two package classes
    - Each package class is optimized for a different approach
  - Creating two sets of transmitter and receiver specifications for backplane and AUI C2C, one for each package class
    - Choose the reference package model that is applicable
  - Channel compliance using COM with a specific reference package on each end
  - Apply to backplane PHYs, AUI C2C interfaces

- A straw poll and motion was requested

BACKUP

Reference: Proposed direction of CR TP0d-TP2/TP3

$TP0_d$-TP2/TP3 Insertion Loss (informative Annex)

- Partition loss budget allocation for device package + host
- No change to test point reference TP2/TP3 i.e., testing of normative TX/RX

Annex 162A
(informative)

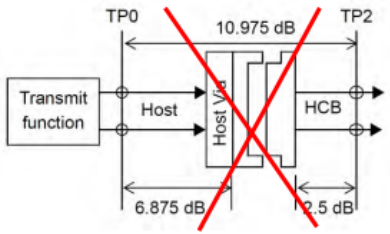
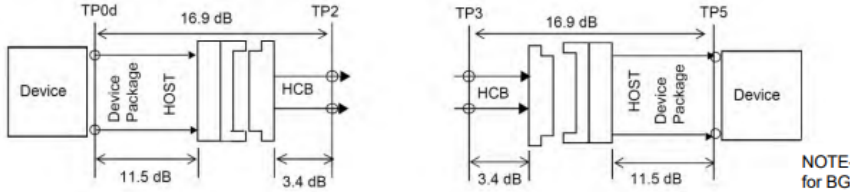


Table XXX–X—Test points

Test points	Description
$TP0_d$ to $TP5_d$	The channel including the device package, the host transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance PCB insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure xxx-x. The cable assembly test fixture of Annex xxxx, or its equivalent, is required for measuring the cable assembly specifications in xxx.x at TP1 and TP4.
$TP0_d$ to TP2 TP3 to $TP5_d$	A mated connector pair has been included in both the transmitter and receiver specifications defined in xxx.x and xxx.x. The recommended maximum insertion loss from $TP0_d$ to TP2 or from TP3 to $TP5_d$ including the test fixture is provided in xxx.x.
TP2	Unless specified otherwise, all transmitter measurements defined in xxx.x are made at TP2 utilizing the test fixture specified in Annex xxxx.
TP3	Unless specified otherwise, all receiver measurements and tests defined in xxxx are made at TP3 utilizing the test fixture specified in Annex xxxx.



NOTE—The 11.5 dB ILdd includes allowance for BGA and connector footprint vias.
NOTE—Device package not including bump capacitance

Figure XXXA–X—$TP0_d$-TP2/TP3 Insertion loss at 53.125 GHz

8

802.3dj Task Force

https://www.ieee802.org/3/dj/public/23_07/diminico_3dj_01b_2307.pdf