Pad insertion with 8:1 Hamming Interleaver for Inner FEC

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Background

- The inner FEC in patra_3dj_01b_2303 with FEC lane rate, convolutional interleaver details in he_3dj_01_2307 was adopted in the P802.3dj March 2023 and July 2023 Plenary meetings, respectively.
  - The adopted padding block size is 384 bits (3x Inner FEC CWs) without Hamming interleaver protection
- rechtman_3dj_01a_2305 examined the value of using 8x128b padding block protected by Hamming interleaver
- he_3dj_03b_2307 suggested Inner Codeword Self-sync method which can also benefit from the 8x128b + Hamming interleaver structure.
- Several proposals to use the padding bits for backchannel: ghiasi_3dj_01a_2307 and dudek_3dj_optx_01_230629
  - Would benefit with improving pad protection scheme.

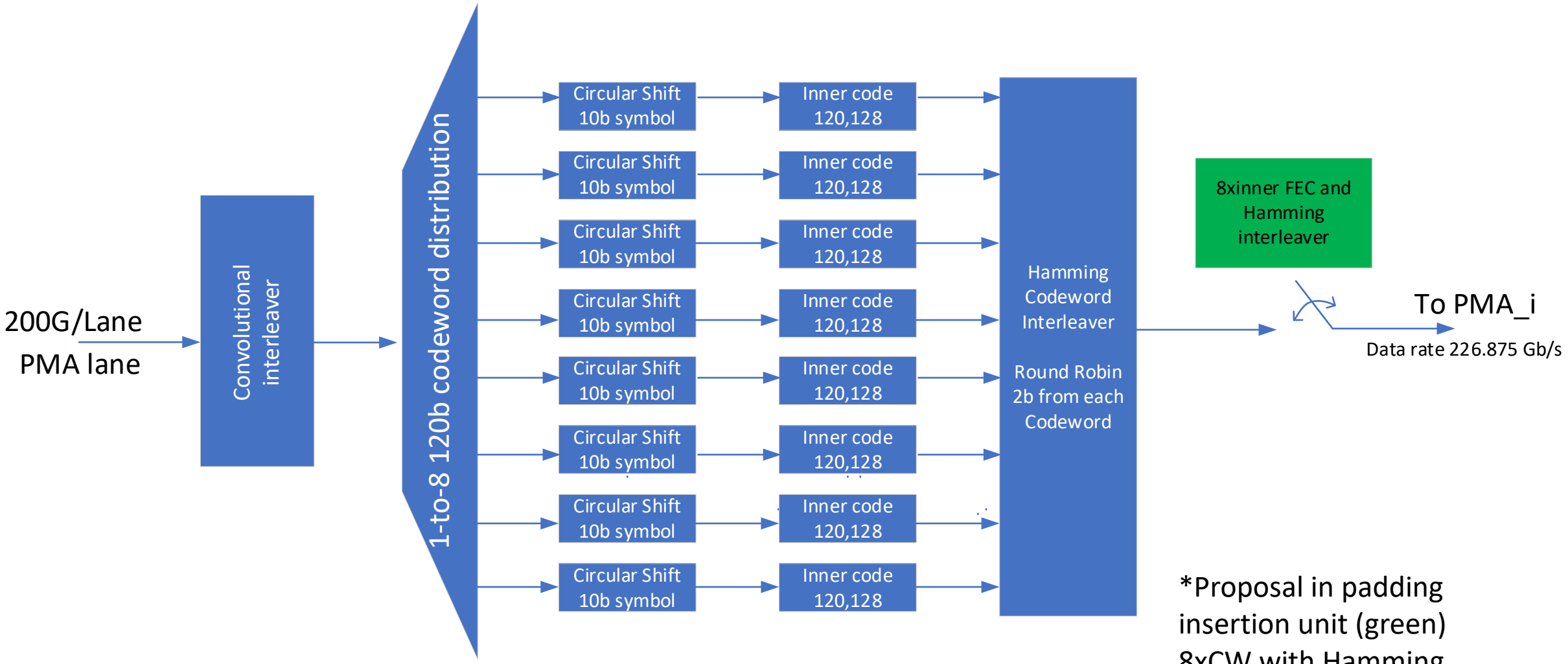
This presentation

- Provides more details on the pad insertion with 8:1 Hamming Interleaver.
- Revisits the advantages of the proposed pad insertion.

Pad insertion proposal - 1024 bits/8 CWs with Hamming interleaver

- Inserted every 8704 inner FEC CWs $(106.25Gbd * \frac{128}{120} * \frac{8704+8}{8704} = 113.4375Gbd)$
  - No change in the singnaling rate of 113.4375 Gbd
- **8-way Hamming interleaver "protection" on padding bits**
- Enable definition of RX synchronization using Framing Sequence (FS)
- Enable self synchronization implementation (Search & Test synchronization) as suggested in he_3dj_03b_2307
- Allow implementation with minimal number of inner-FEC encoders/decoders.
- Consistent Datapath stream of Hamming Interleaved PAM4 bit-pairs on the PMD lane.
- Padding latency (~4.5 nsec)
  - PTP is not affected because Tx and Rx timestamp differences are cancelled.
  - For comparison Clause 172 (800G PCS) AM size is 4,112 bits total.
- Time between pad blocks ~4.91usec

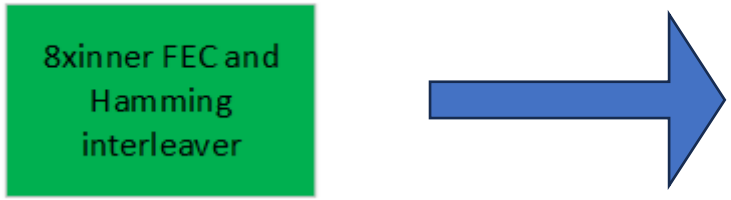
8xCWs (1024 bit) and Hamming interleaver as shown in [he_3dj_01_2307.pdf]

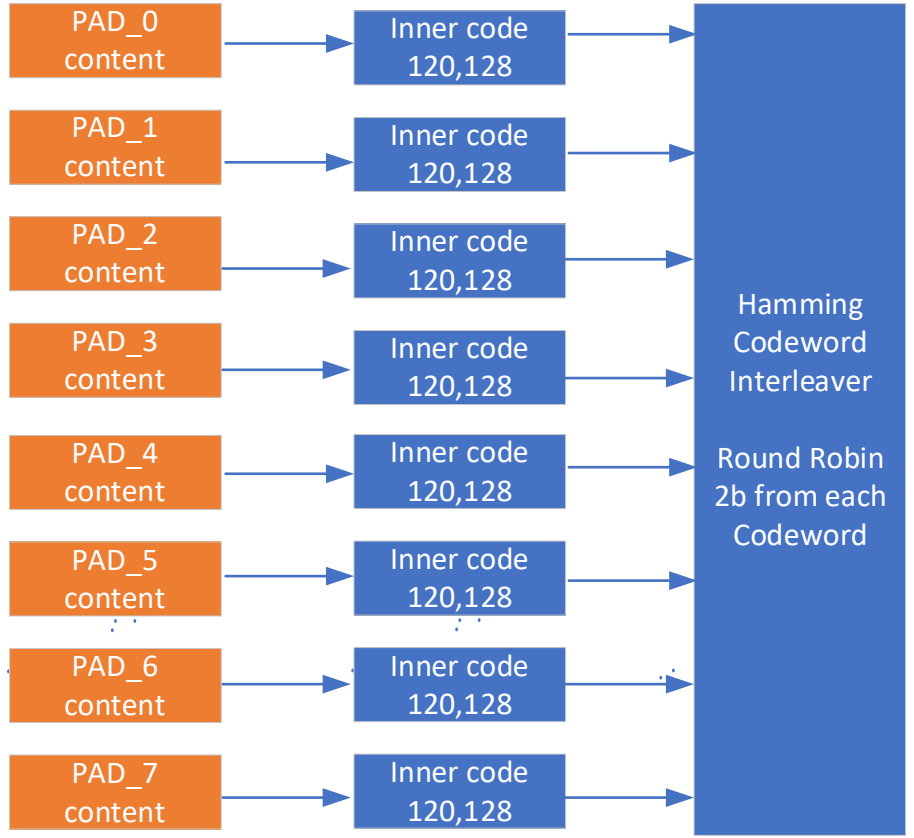


*Proposal in padding insertion unit (green) 8xCW with Hamming interleaver.

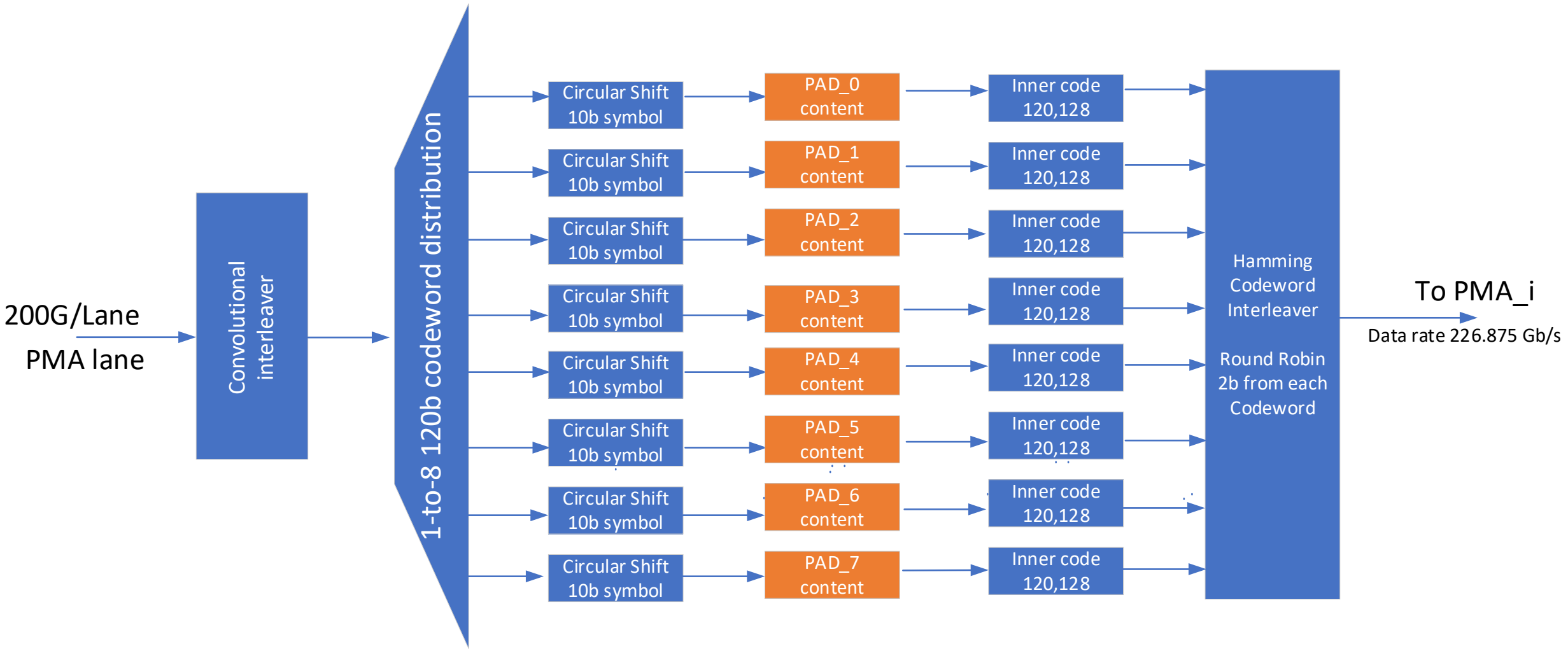
What the pad insertion process contains

- This diagram represent the padding insertion unit (green unit from previous slide):
- Allows the reuse of same inner code and Hamming interleaver
- PAD_i structure description on following slides





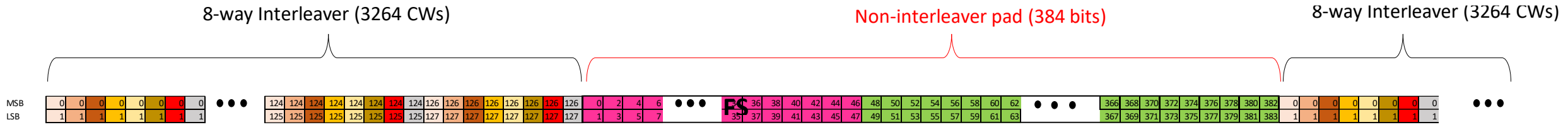
Equivalent representation of the proposed change



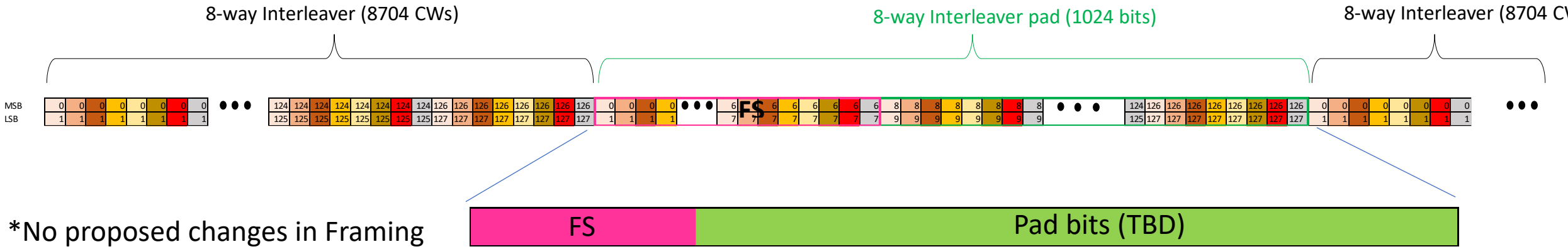
* Each of PAD_i contain 120 bits

Simple data stream on PMD

- From <u>two types</u> of streams:



- To <u>single type</u> of stream:



*No proposed changes in Framing Sequence (FS) size (48 bit) and content on the PMA_i lane

Pad structure (prior to encoding function)

- Pad is 960 bits (prior to 128,120 encoder)
  - 48 bits for the Frame Sequence (FS)
  - 912 bits as padding bits (e.g. backchannel)
- 120-bit PAD_i bits per encoder (i.e. exactly inner-FEC CW)

  In figure to right:
  - 2-bit symbols (Hamming interleaver is 2 bits).
  - Symbols 0-2 on each PAD_i are defined Frame Sequence (FS)
  - Symbols 3-59 on each PAD_i contain the rest of the padding bits that can be used for backchanneling

	2-bit PAM4 symbol index																	
PAD_i	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	..	58	59
0	FS[0:1]	FS[16:17]	FS[32:33]							..	..					..		
1	FS[2:3]	FS[18:19]	FS[34:35]							..	..					..		
2	FS[4:5]	FS[20:21]	FS[36:37]							..	..					..		
3	FS[6:7]	FS[22:23]	FS[38:39]							..	..					..		
4	FS[8:9]	FS[24:25]	FS[40:41]							..	..					..		
5	FS[10:11]	FS[26:27]	FS[42:43]							..	..					..		
6	FS[12:13]	FS[28:29]	FS[44:45]							..	..					..		
7	FS[14:15]	FS[30:31]	FS[46:47]							..	..					..		

FS[0:47]=01011001 01010010 01100100 10100110 10101101 10011011

FS (48 bits)
PAD bits (912 bits)

- PAD_0[0:5]= 01 01 10
- PAD_1[0:5]= 01 10 10
- PAD_2[0:5]= 10 01 11
- PAD_3[0:5]= 01 00 01
- PAD_4[0:5]= 01 10 10
- PAD_5[0:5]= 01 10 01
- PAD_6[0:5]= 00 01 10
- PAD_7[0:5]= 10 10 11

Frame sequence vs self synchronization

- Frame sequence bits are needed to identify and remove the pad bits
  - Identification can be done before (FS sync) or after (self-sync) 128,120 decoder.
- From he_3dj_01_2307:

The following table shows the performance comparison based on numbers above.

	CL119 AM	(128,120) Self-sync	Notes
Mean time to lock, **µs**	100	<1	Mean time to find the codeword boundary on a bit stream. Lower is better.
Mean time to false-lock, **yrs**	6×10^{22}	3×10^{23}	Mean time that it locks to a wrong position. Higher is better. **Should never happen.**
Mean time to false-unlock, **yrs**	6×10^{16}	4×10^{18}	Mean time that the lock breaks during normal operation. Higher is better. **Should never happen.**
Mean time to unlock, **µs**	400	<1	Mean time to drop sync when needs to. Lower is better.

Self-sync performs better in every aspect.

- **The proposed padding insertion (8xCWs) is appropriate to both synchronization methods.**

Utilization improvement under burst errors

- Using 8xCWs improves the ratio of backchannel payload / total pad length
  - From (360-48-8)/360 = 84.4% to (960-48-8)/960 = 94.16%
- ramesh_3dj_01b_2303 showed how repetitions with plurality voting (PV) could improve the MTTFPA of messages sent in padding codewords.
  - The recommendation was to repeat each message 15 times, which reduces the equivalent bandwidth to 1/15.
  - With burst errors, more repetitions may be needed to lower the failure rate (where PV cannot be resolved due to too many uncorrectable codewords), which will further lower the usable bandwidth.

Burst Factor "a"	Failure rate (cannot resolve PV) @ 4E-3 BER		Equivalent Bandwidth, Mbps	
	3xCWs, SD 6/15 PV	8xCW Interleaved SD, 6/10 PV	3xCWs, SD 6/15 PV	8xCW Interleaved SD, 6/10 PV
0	2.9E-17	<1E-4	10.995	18.390
0.1	1.1E-10	<1E-4	10.995	
0.375	9.8E-4	<1E-4	10.984	
0.5	**3.0E-2**	<1E-4	10.665	
0.75	**7.4E-1**	<1E-4	2.834	

Summary

- Proposal: change the pad block from 384 bits to 1024 bits (8 Inner FEC CWs) and insertion period from 3264 CWs to 8704 CWs, including 8:1 Hamming interleaver protection for pad.
- It is recommended to define PV (Plurality Voting) of x/10 with x>=5 to meet MTTFPA and effective BW goals.
- Content of the bits for backchannel (message field) should be addressed separately

Backup

Comparison table

	384 bits (patra_3dj_01b_2303.pdf)	1024 bits (proposed)
Baud rate	113.4375 GBd	113.4375 GBd
Hamming Interleaver “protection”	No	Yes
Similar to existing 802.3 BASE-R AMs/CWMs insertion process	No	Yes
Time/CWs between pad bits	1.8 usec/3264 CWs	4.91 usec/8704 CWs
Pad latency	1.7ns	4.5ns
FS lock	Yes	Yes
Possible S&T synchronization method	No	Yes
Number of encoder/decoder Power/Area	Additional inner-FEC encoders/decoders required for the pad bits	Can be optimal (reuse of inner FEC and interleaver)

Pad structure (prior to encoding function)

- Second option based on [huang_3dj_01_2307](#) proposal
- Pad is 960 bits (prior to 128,120 encoder)
  - 24 bits for the Frame Sequence (FS) + 8 bits for message index + 24 bit for Frame Sequence + 8 bits for Message type
  - 896 bits as padding bits (e.g. backchannel)
- 120-bit PAD_i bits per encoder (i.e. entire inner-FEC CW)

  In figure to right:
  - 2-bit symbols (Hamming interleaver is 2 bits).
  - Symbols 0-3 on each PAD_i are defined Frame Sequence and the Message control
  - Symbols 4-59 on each PAD_i contain the rest of the padding bits
- Mimic the organization of the common marker (CM) portion of 200G/400G/800G PCS AM for hardware reuse purpose

	2-bit PAM4 symbol index																		
PAD_i	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	..	58	59
0	FS[0:1]	FS[16:17]	FS[24:25]	FS[40:41]						..	..					..		
1	FS[2:3]	FS[18:19]	FS[26:27]	FS[42:43]						..	..					..		
2	FS[4:5]	FS[20:21]	FS[28:29]	FS[44:45]						..	..					..		
3	FS[6:7]	FS[22:23]	FS[30:31]	FS[46:47]						..	..					..		
4	FS[8:9]		FS[32:33]							..	..					..		
5	FS[10:11]		FS[34:35]							..	..					..		
6	FS[12:13]		FS[36:37]							..	..					..		
7	FS[14:15]		FS[38:39]							..	..					..		

FS[0:47]=01011001 01010010 01100100 10100110 10101101 10011011

FS (48 bits)
PAD bits (192 bits)
Message index
Message type

- PAD_0[0:7]=01 01 10 10
- PAD_1[0:7]= 01 10 10 01
- PAD_2[0:7]= 10 01 01 10
- PAD_3[0:7]= 01 00 10 11
- PAD_4[0:7]= 01 xx 10 xx
- PAD_5[0:7]= 01 xx 10 xx
- PAD_6[0:7]= 00 xx 11 xx
- PAD_7[0:7]= 10 xx 01 xx
- Here, x means bit (0 or 1) for message index and Message type